SCSI signal modeling study group (SSM)
September 01, 1999
Colorado Springs, NH

Subject: Draft minutes for the SSM study group

This was the third meeting to address the general subject of modeling
for parallel SCSI. Dean Wallace of QLogic led the meeting. Bill Ham of
Compaq took these minutes. There was a good attendance from a broad
spectrum of the industry. LSI Logic (Larry Barnes) hosted the meeting.

Last minutes: 99-236r1.

1. Introduction

Dean Wallace opened the meeting and conducted the introductions and
reviewed the meeting purpose.

2. Attendance

The following folks were present:

Dean Wallace, Qlogic, d_wallace@qlc.com
Martin Ogbuokiri, Molex, mobuokiri@molex.com

Larry Barnes, LSI Logic, larry.barnes@lsil.com
Johnathan Fasig, Western Digital, johnthan.L.Fasig@wdc.com
Tariq Abou-Jeyab, Adaptec, tajayab@corp.adaptec.com
Paul Aloisi, Unitrode, aloisi@unitrode.com
Richard Uber, Quantun, Richard.Uber@ quantum.com
Bill Ham, Compaq, bill_ham@ix.netcom.com
Andrew Bishop, Quantum, andrew.bishop@quantum.com
Craig Clewell, FCI Electronics, cwc@ieee.org
Nicholaos Limberapoulas, C&M, Nlimbeeropoulos@cm-corp.com
Matt Schumacher, Compaq, Matt.Schumacher@compaq.com
John Lohmeyer, LSI Logic, lohmeyer@t10.org
Frank Gasparik, LSI Logic, frank.gasparik@lsil.com

3. Agenda development

The agenda shown was that used.

4. Approval of previous minutes

Confusion about the formats for distributing the minutes caused two
separate versions to be created one for the reflector and one for the
web site. It was decided that the reflector format was too limiting and
cumbersome and that a notice of the minutes being posted to the T10 web
site would be all that is done on the reflector. The minutes may
contain graphics and other formatting that the .pdf format handles very
well.

This strategy enables a much more efficient creation, tracking,
modifying, and approval process.

The minutes of the July meeting were approved with slight modifications
and Ham will post them with the corrections.

5. SSM Project proposal - Ham

Bill Ham requested that the group develop an SD-3 (more correctly a
project proposal) to focus the modeling work for the group. This
subject was extensively discussed with the merits of technical report vs
standard and other issues. After all the points were considered the
group decided unanimously that the SCSI signal modeling group would
pursue a standard.

Using a project proposal template supplied by John Lohmeyer the group
edited the content, including the candidates for technical content.
Bill Ham uploaded this project proposal as document T10/99-243r0 to the
T10 web site for further consideration at the SCSI working group in
September.

The sections containing the work content candidates was:

        The SCSI Signal Modeling standard (SSM) is a collection of
        requirements on methodologies to be used to simulate SCSI signals.

These methodologies support the current family of SCSI standards
and are designed to work at the data rates expected to be
specified through 2006.

the following items may be considered for inclusion in SSM

1. methodologies and models for all the types of components that
   exist in a SCSI signal path
2. simulation tools
3. benchmark data patterns;
4. benchmark test configurations;
5. output types and formats;
6. output evaluation schemes;
7. evaluation of signaling methodologies (encoding, ISI compensation,
   etc.);
8. physical measurement / simulation correlation;
9. definitions for terms and concepts of signal integrity (SNR,
   random and deterministic jitter);
10. translation between component manufacturing control parameters and
    simulation input parameters
11. other capabilities that may fit within the general application
    scope of the this project.

Larry Barnes of LSI Logic is the technical editor.

It was the sense of the group that without a standardized methodology
that accurate interpretation of simulation results would be (and is)
problematic.

6. Presentations

6.1 IBIS modeling: Tariq Abou-Jeyab, Adaptec

Tariq reviewed an example of a National LVDS driver used with the IBIS
methodology. This produced a number of excellent discussions.e Tariqs
presentation is included as an annex to these minutes.

6.2 IBIS framework: Dean Wallace, QLogic

Dean went thru a somewhat detailed explanation of how IBIS works. This
is somewhat captured below:
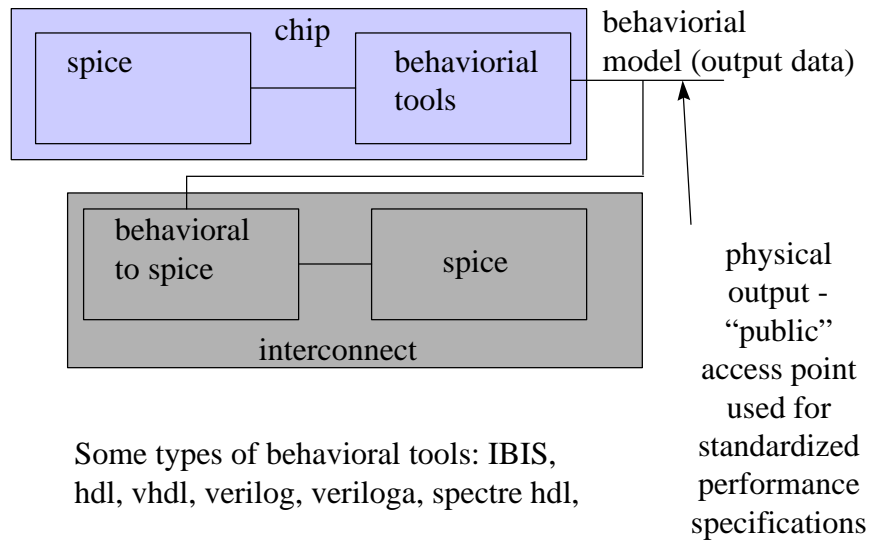
TRANSCEIVER CONFIGURATION

chip

spice | behaviorial tools

behaviorial model (output data)

behavioral to spice | spice

interconnect

physical output - "public" access point used for standardized performance specifications

Some types of behavioral tools: IBIS, hdl, vhdl, verilog, veriloga, spectre hdl,
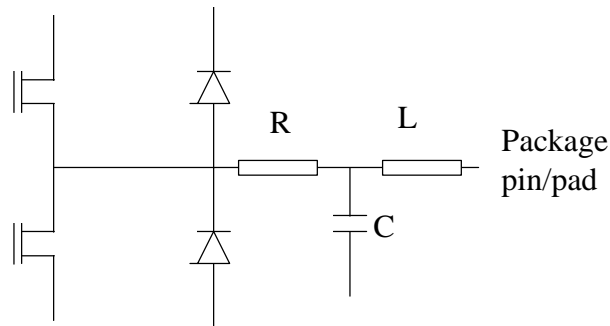
Figure 1 - Chip / interconnect modeling relationships

Typical IBIS output configuration

R   L

Package pin/pad

C

Output is the values of the R, L, C components, the IV curves for the transistors and diodes, simple rise and fall times

Figure 2 - Example of an IBIS output style

The present definition of IBIS models do not allow for multilevel logic or for schemes where the intensity or shape of the signal is purposefully adjusted (for emphasis / ISI management or feedback slewrate control for example). This was viewed as a serious limitation of the presently available IBIS specification and as a serious mandate to improve on the capabilities of behavioral tools for SCSI applications.

7. Model data base strategy

A need for a way to archive the specific models that are developed was extensively discussed. John Lohmeyer noted that he did not want to be directly responsible for maintaining the model data base. Therefore, another approach was developed:

- John agreed to help the owner set up the web site for the data base.

- Dean Wallace agreed to be the owner.

- Dean will create a proposal for using this web site.

8. Output of group

The effort will produce three types of output: (1) reports to the SCSI working group through minutes, reports, and other means, (2) a new standard document containing the technical details, and (3) a web based repository for specific models.

9. SFF backplane

Bill H noted this activity is still planned but not yet started.

10. SSM document organization - Barnes

Larry Barnes reviewed a proposal for the document organization. The details will be visible in the first draft when it becomes available after the project proposal is approved.

11. Matrix development for SSM - Ham/Wallace

A matrix was developed that captures the architectural relationships between the components in a SCSI point to point connection. The relationships for multidrop connections will follow a similar pattern but were not attempted at this meeting.

For the point to point connections the general relationships are shown in Figure 3.
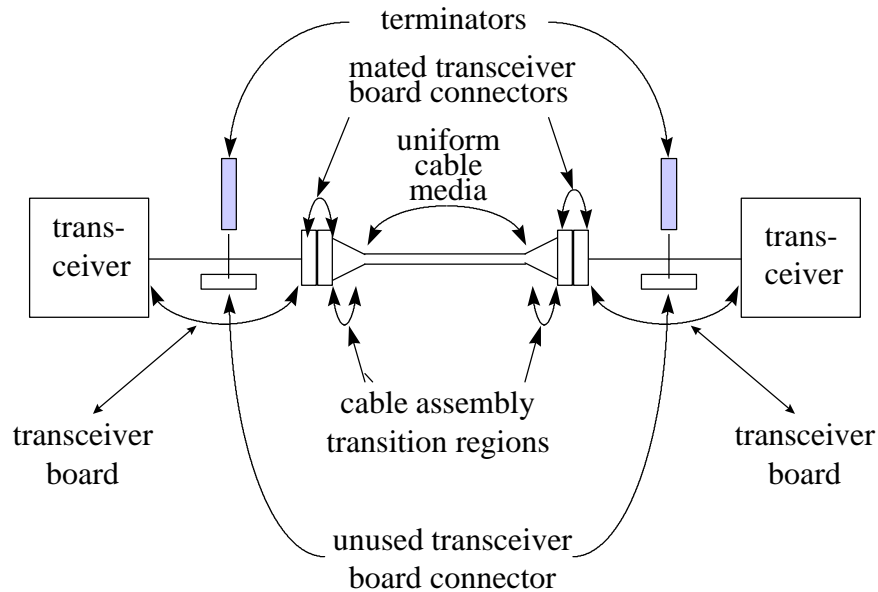
Figure 3 - Relationship of point to point SCSI connection components

Each component labeled in Figure 3 is to be modeled according to a set of attributes that are appropriate to the behavior and interfaces for the component. A start at capturing these attributes was made and the results are presented next:

11.1 Transceiver chips: owner, Dean Wallace

Interface is at packaging pins
Model types: Spice, IBIS, HDL, table spice – details TBD
Data patterns: TBD
ISI compensation: TBD
Single line / Multiline: TBD

11.2 Bus segment termination: owner, Paul Aloisi

Interface is at package pins
Model types: Spice, IBIS details TBD
Terminator type: multimode
Single line, multiline TBDE

11.3 Transceiver board: owners, Tariq Abou-Jeyab and Matt Schumacher

Interface is at transceiver board connectors, transceiver chip pins, terminator chip pins

Model types: Spice, Maxwell coefficients
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

11.4 Transceiver board connector: owner, Martin Ogbuokiri

Interface is at transceiver board and the cable assembly transition region
Model types: Spice, Maxwell coefficients
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,
single line, multiline

11.5 Cable assembly transition region: owner, Dave Chapman?

Interfaces are at the connector termination and the uniform media
Model types: Spice
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multiline

11.6 Uniform cable media: owner, Jie Fan

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: Spice, Maxwell coefficients
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

12. Simulation integration strategy

Further discussion pending progress on the component level simulation work.

13. System configurations

Not discussed

14. Data patterns

Not discussed

15. Data rate

Not discussed

16. Definitions:

Not discussed

17. Tools:

This topic refers to identification and properties of specific modeling
tools. It was not discussed at this meeting.

18. Next meetings

Sept 29, 1999 Lisle IL (Holiday Inn
October 27, 1999 Huntington Beach, CA
Dec 01, 1999 Rochester, MN

19. Action Items:

Martin O. to supply a block diagram of the simulation process used to do
the simulation for TDR.
Status: carried over

Jonathan Fasig to send the lists of reference material electronically to
Bill Ham for posting on the web site.
Status: done

Martin O. to supply an RGL transmission line matrix (circuit type of
specification) for VHDCI, SCA-2,and HD68 connectors.
Status: carried over

Dean to provide a target board model.
Status: carried over

Larry Barnes to create a document framework.
Status: done and ongoing

Larry Barnes to do an overview presentation of the IBIS transceiver
model specification.
Status: handouts provided but presentation still needed

Tariq to provide an IBIS transceiver model
Status: done

Ham to post the draft minutes (after review by Dean) of the July meeting
Status: carried over pending establishment of the new draft/approval
minutes process – will be posted as approved minutes

Han to post the draft minutes of the September 01 meeting after review by Dean
Status: new

20. Annex: presentations

ibis.ppt

Further details are available from Tariq.