T10/99-262 r2

LSI LOGIC®

4420 ArrowsWest Drive
Colorado Springs, CO 80907

02/09/2000

To: T10 Technical Committee
From: William Petty, LSI Logic Corp.
Subj: **SPI-4 REQ/ACK ISI removal via qualified clocking with combined Deskew Training method**

Change Control

Rev.	Date	Description of Change
0	9/9/99	Initial Document
1	10/11/1999	Disallowed gating of ST following ST or DT following DT. Paired ST and DT qualification into single event. Revised waveforms to match text.
2	02/09/2000	Complete rewrite.

1. PROPOSAL SUMMARY

The effects of pattern dependant ISI created when REQ or ACK pause can be removed by utilizing the unused P1 signal line as a qualifier for REQ or ACK from the device that sources data.

1.1 Primary Goals

- To remove one of the two sources of compounding ISI timing errors.
- Establish an ISI free reference clock at the receiver.

1.2 Assumptions

- Must only be used in DT phase after fast-160 negotiations are complete.

2. Waveforms

The following graph illustrates both the free-running clock start-up and the Deskew training pattern.

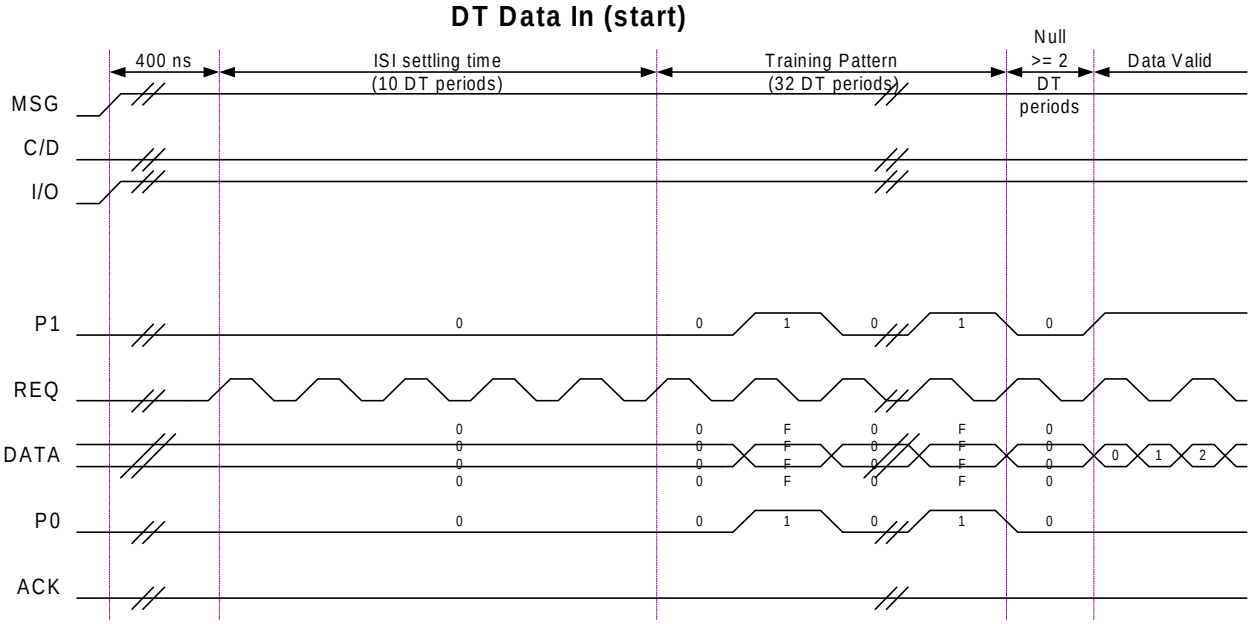

Figure 1

The following graph illustrates both the data clocking and CRC/exit method.

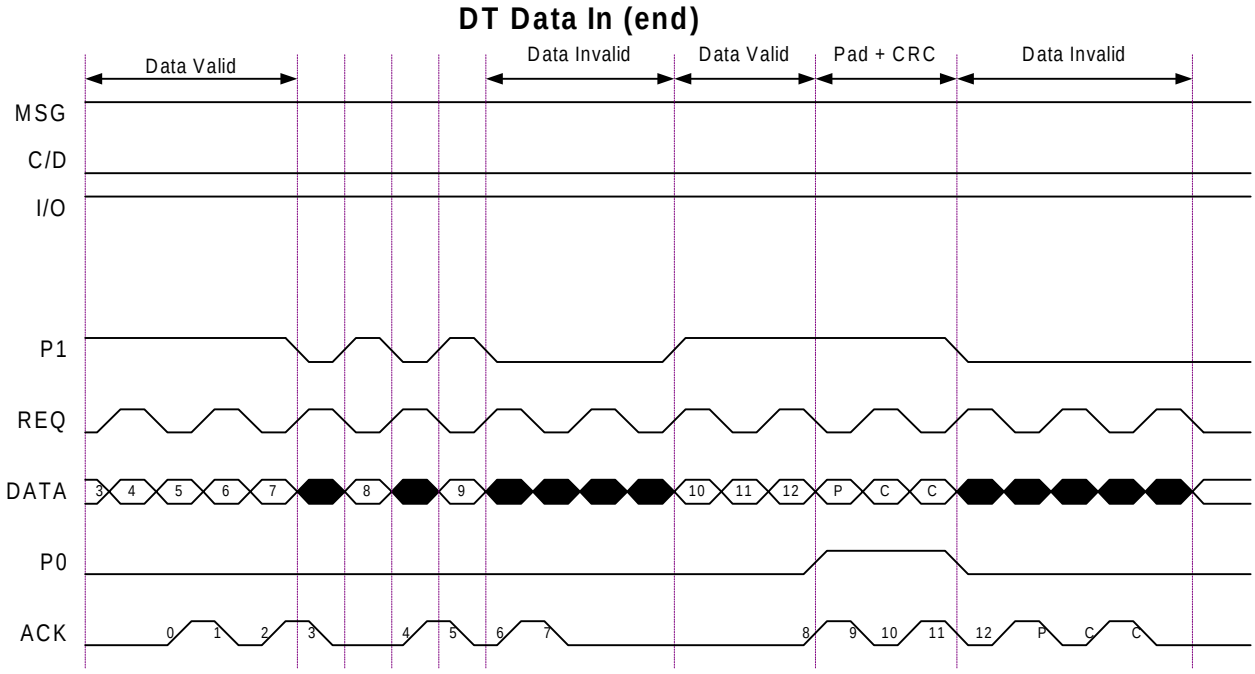

Figure 2

1. The currently unused P1 signal is held negated while the REQ clock begins transitioning at the maximum agreed period for 10 DT periods to ensure that the majority of all ISI components die out. The first REQ assertion is also used to qualify the phase as normal.
2. After counting off the 10 DT edges, deskew training begins and lasts for 32 DT periods. Each "Training Cell" consists of 4 DT periods which represent two complete cycles of the reference clock (REQ) which starts with an asserting edge and one complete cycle of all lines being trained (Data, P1, and P0) which starts with a negated edge or level. The 32 DT periods encompass eight "Training Cells" which allows for a minimum resolution of (Correction Window divided by 256). Assuming a de-skew correction range of +-5nS, this would yield 10nS/256 = 39pS.
3. After counting off the 32 DT edges, all trained signals are negated for a minimum of 2 DT periods. This delay allows internal registering of the final values. All following detected assertions of P1 indicate that the associated data is valid.
4. The P1 signal, which is now de-skewed and has the same timing characteristics as the data lines, shall be transmitted in unison with both the REQ and DATA signals and used as a qualifier to validate the data. P1 is sampled on both the Asserting and Negating edges of REQ, and if sampled active, qualifies the data for the current data cell.
5. The corresponding ACK signal is not time correlated with any other signal lines and thus needs no qualifier. It is counted to maintain proper offset management.

The following graph shows the both the free running clock start-up and the Deskew training pattern.

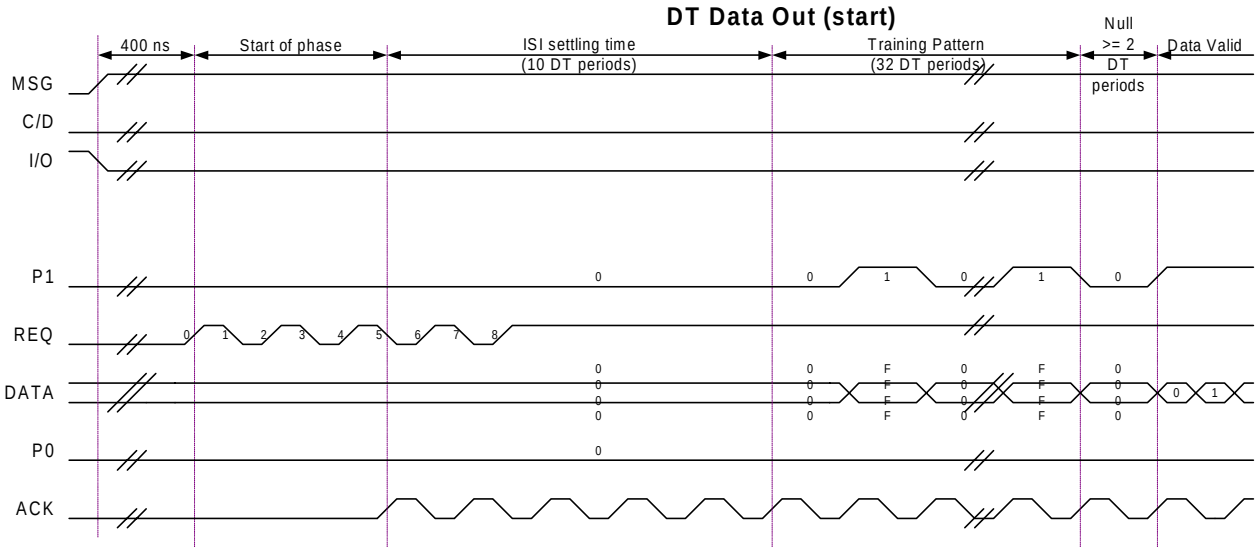

Figure 3

The following graph shows the both the free running clock start-up and the Deskew training pattern.

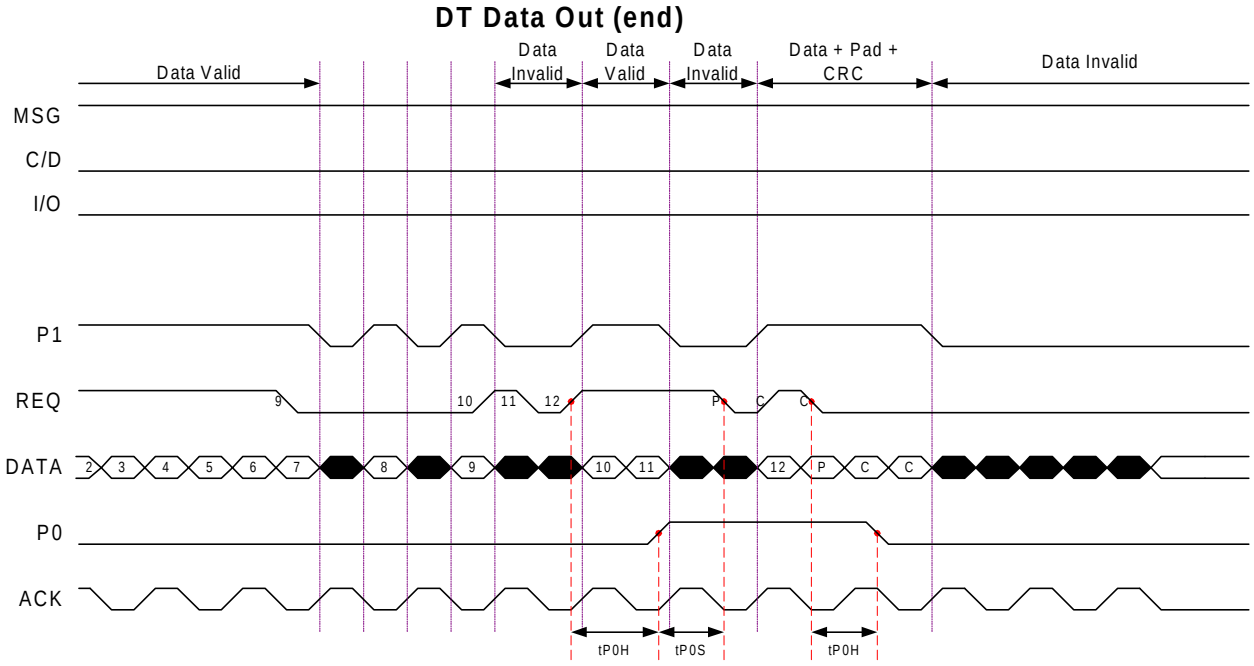

Figure 4

2.1 Implementation Description (DT Data Out)

1. After the phase change settle time, the REQ signal begins building up the offset and its first assertion validates the phase.
2. The currently unused P1 signal is held negated while the ACK clock begins transitioning at the maximum agreed period for 10 DT periods to ensure that the majority of all ISI components die out.
3. After counting off the 10 DT edges, deskew training begins and lasts for 32 DT periods. Each “Training Cell” consists of 4 DT periods which represent two complete cycles of the reference clock (ACK) which starts with an asserting edge and one complete cycle of all lines being trained (Data and P1) which starts with a negated edge or level. The 32 DT periods encompass eight “Training Cells” which allows for a minimum resolution of (Correction Window divided by 256). Assuming that the de-skew correction range is +-5nS, this would yield 10nS/256 = 39pS.
4. After counting off the 32 DT edges, all trained signals are negated for a minimum of 2 DT periods. This delay allows internal registering of the final values. All following detected assertions of P1 indicate that the associated data is valid.
5. The P1 signal, which is now de-skewed and has the same timing characteristics as the data lines, shall be transmitted in unison with both the ACK and DATA signals and used as a qualifier to validate the data. P1 is sampled on both the Asserting and Negating edges of ACK, and if sampled active, qualifies the data for the current data cell.
6. The corresponding REQ signal is not time correlated with any other signal lines and thus needs no qualifier. It is counted to maintain proper offset management.
7. Since P0 is not de-skewed during DT Data Out it requires a minimum of 10nS setup and a minimum of 10nS of hold with respect to REQ.

2.2 When to do Deskew Training

Deskew training is required once per IT nexus (physical connection) for the first DT Data In and/or the first DT Data Out phase and not repeated until a new IT nexus is established.

On subsequent DT Data phases after training is established, the clock REQ/ACK ISI settling time is still required. The deskew training and null periods are not transmitted.