T10/99-261 r0

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09/09/1999

To: T10 Technical Committee
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Subj: **SPI-4 Timing budget utilizing receiver signal deskew method**

Change Control

Rev.	Date	Description of Change
0	9/9/99	Initial Document

1. PROPOSAL SUMMARY

In order to reach 160 mega-transfers per second while maintaining current cable lengths with viable input timing margins, a method of removing a major portion of deterministic system errors is needed. This proposal describes a method of receiver deskew that can remove most of the signal skew caused by static sources such as silicon clock balancing errors, package, board routing, and cable propagation variations. The amount removed is limited only by the resolution and calibration of the deskew hardware itself.

1.1 Primary Goals

- Removal of deterministic skew errors.
- Minimize performance degradation due to calibration overhead.

1.2 Assumptions

- The major sources of skew vary little over time, temperature, and voltage.
- Primary calibration need only be run during bus scan or when requested.
- Secondary calibration cycles can be hidden within the normal phase change delays.
- The use of single or multi-cycle calibration edges are allowed.

2. Supporting Data

		SPI-4 timing budget					
			Fast-160		**Fast-80**		**Fast40**
Period (ns)							
	Basic Period		12.500		25.000		25.000
	DT Period		6.250		12.500		0.000
	Period Tolerance		0.700		0.700		0.700
Deterministic errors							
	Silicon TX Driver Routing Skew		1.000		1.500		1.500
	Package Skew (Initiator)		0.065		0.065		0.065
	PCB Layout Skew (Initiator)		0.200		0.200		0.200
	Cable Skew (@ 25ps/Ft)		2.500		2.500		2.500
	PCB Layout Skew (Target)		0.200		0.200		0.200
	Package Skew (Target)		0.065		0.065		0.065
	Silicon RX Routing Skew		1.000		1.500		1.500
	HL Vs LH Matching		0.500		0.500		0.500
Non-Deterministic errors							
	Low Vt Vs Substrate Noise		0.200		0.100		0.100
	PLL Jitter		0.500		1.000		1.000
	Cross Talk Induced Jitter		0.100		0.100		0.100
	Cable Period Distortion ISI		2.000		2.000		2.000
	Input Slew Rate Dependent Skew		0.200		0.200		0.200
	Receiver Amplitude Dependent Skew		0.200		0.200		0.200
	Self Cal Accuracy (+-100ps)		0.200		0.000		0.000
Data Valid Window			2.000		2.020		14.170
Data Setup/Hold			1.000		1.010		7.085
	NOTE Cable timings based on good quality twisted pair round shielded cable						
	* These values are removed by **Skew Compensation Logic**						
	* Calculated Value						

2.1 Deskew Requirements

The timing diagram in Fig. 2 shows the input Vs output timing waveforms for a typical deskew circuit.

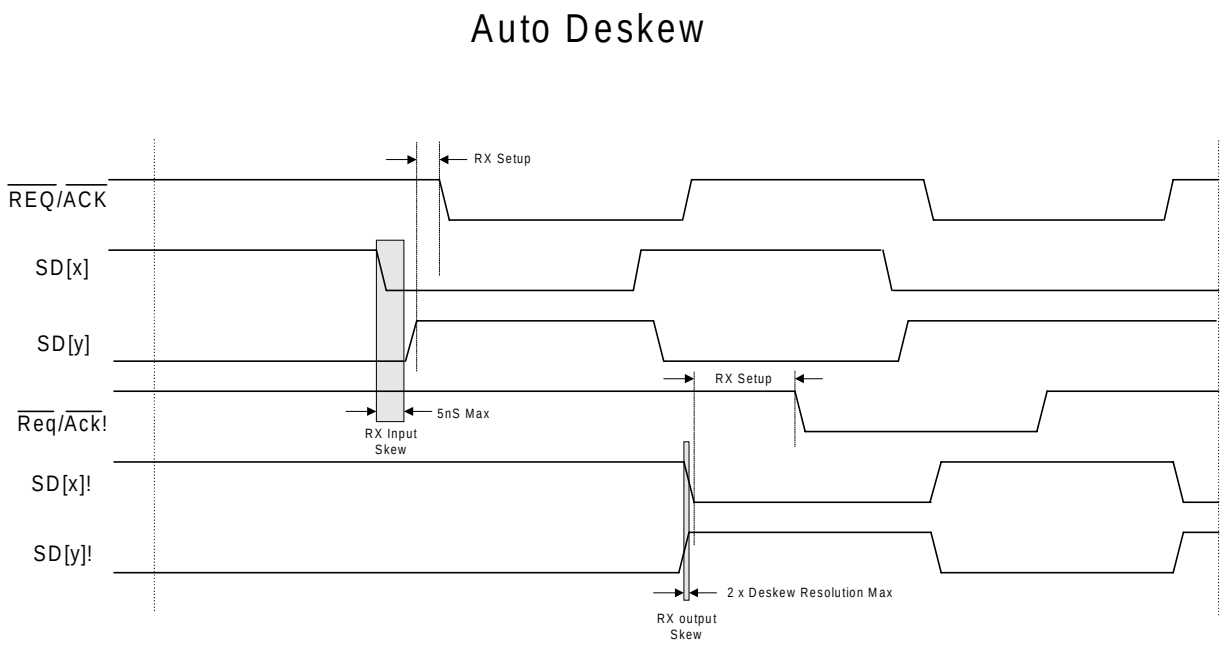

Figure 1

Not only can the deterministic skews be minimized, it is also easy for the internal REQ/ACK! strobe to be positioned to its optimum placement.

By using the current SPI-3 timing budget values plus an allotment for silicon based contributions a minimum of 5nS of absolute skew correction is needed. But, due to the hardware not knowing which signals will be best or worst for any given cable plant, the deskew delay generators must be capable of covering ±5ns for a total of 10ns of timing adjustment over temperature and process. The minimum resolution step in this 10nS delay generator is not yet defined but should be ≤ 100pS due to the small final setup and hold budget.

During calibration, the REQ/ACK delay generator is set to its midpoint – one setup delay and all data/parity signals are adjusted to occur line on line with the output REQ!/ACK!. After calibration is complete, the REQ/ACK delay generator is readjusted to achieve the desired setup/hold of the internal latches. These calibration values for each pin should also be available for storage and retrieval on a per connection basis.

The training patterns presented to the receiver should accommodate both a single edge deskew mechanism similar to HIPPI 6400 as well as Multi-cycle techniques. It must also allow for all ISI interference to die out prior to the actual calibration edge(s). See Fig 2 waveform below.

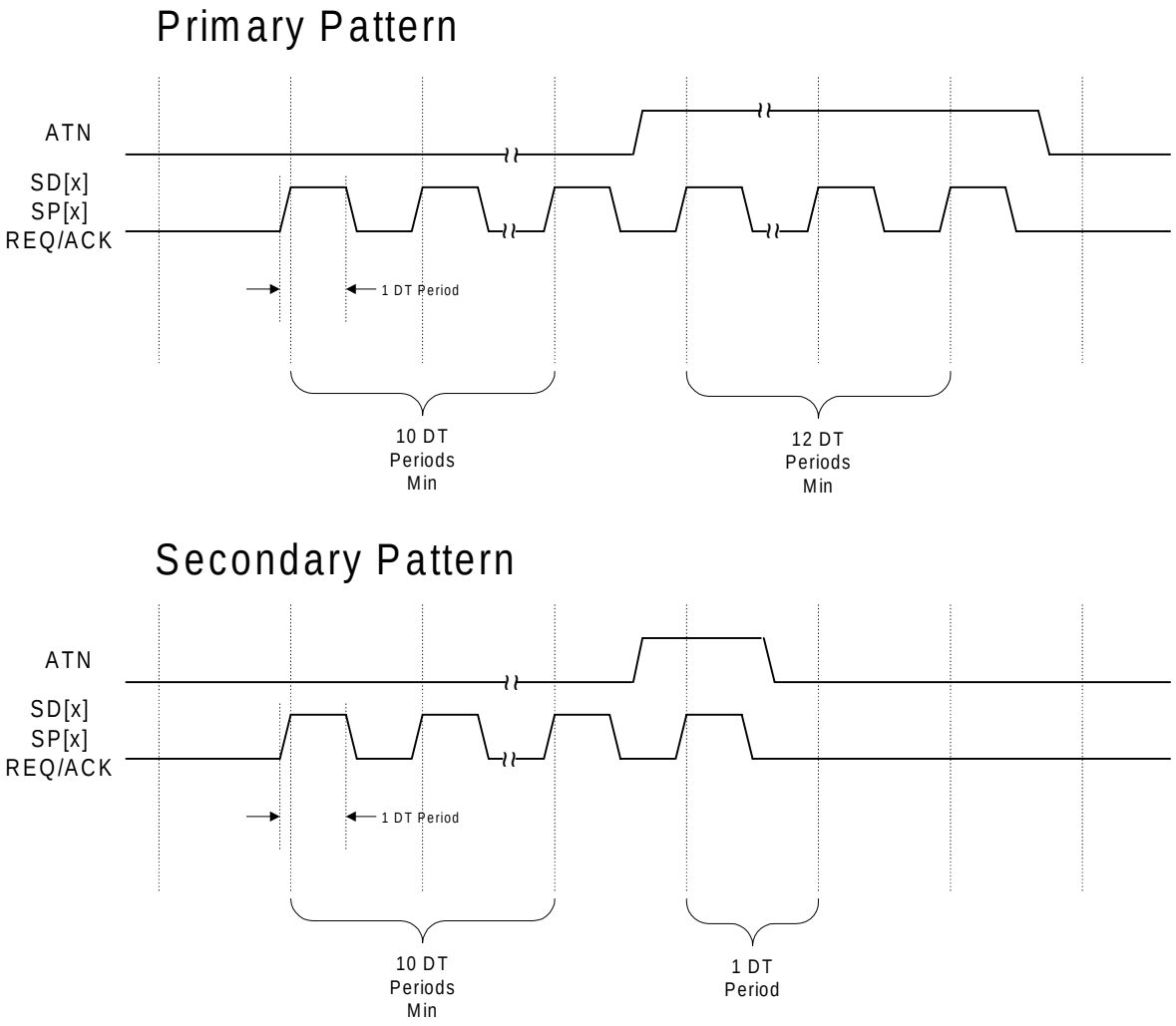

Figure 2

The multi-cycle method also has the additional capability of switching from bit write mode during the primary multi-cycle calibration to increment/decrement mode during secondary calibration cycles. These secondary cycles consist on a single calibration edge only and are used to track any subtle changes in the sources of skew. These secondary cycles should be run on a selection/re-selection basis while primary calibrations would only be run at bus scan time or when requested due to CRC errors.