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GOALS:

DEFINE CHANGES NEEDED TO ACHIEVE AT LEAST 640 MBY/SEC (16 BIT BUS).
DO SO WITH NO CHANGES TO CABLE PLANT.

ISSUES:

1. FREQUENCY RESPONSE OF THE CABLE.
2. DRIVE LEVELS OF THE SIGNALS (GIVEN LOSS IN CABLE).
3. ISI ISSUES OF THE REQ & ACK SIGNALS
4. SKEW OF THE CABLE.
5. ISI ISSUES OF THE DATA SIGNALS.
6. BIAS OF THE RECEIVERS (FAIL SAFE BIAS IS A DC NOISE SOURCE).

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1. FREQUENCY RESPONSE OF THE CABLE

- GOOD SCSI CABLE ROLL OFF OCCURS AROUND 100 MHZ.
- CURRENT 40 MHZ SIGNAL (ULTRA 160/M) HAS THIRD HARMONIC AT 120 MHZ.

DOUBLE CLOCKING (JUST RAISE FREQUENCY).

- THIRD HARMONIC WOULD BE AT 240 MHZ, MOSTLY BEYOND RANGE OF CABLE.
- NRZ CODE HAS RUN LENGTH PROBLEM (COULD TRY TO SCRAMBLER).
- CODES THAT SOLVE RUN LENGTH TEND TO REQUIRE MORE BANDWIDTH (4b5b) AND LOGIC COMPLEXITY DUE TO PACKING AND UNPACKING OF DATA.

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1. FREQUENCY RESPONSE OF THE CABLE

ENCODING

- MULTILEVEL CODE WOULD LOWER FREQUENCY SPECTRUM BUT DETECTION MORE DIFFICULT.
- WOULD WANT RUN LENGTH LIMITED CODE TO REDUCE ISI.
- WOULD WANT CODE WITH NO DC COMPONENT.
- WANT CODE THAT DOES NOT REQUIRE MORE BITS PER BYTE.
- FOR SCSI HALF DUPLEX OPERATION LONG START UP TIMES NEED TO BE AVOIDED. LONG START UP TIMES.

NOTE: POPULAR CODES SUCH AS 4B/5B AND 8B/10BWHICH HAVE RUN LENGTH LIMIT AND NO DC COMPONENT ACTUALLY REQUIRE MORE BITS TO BE SENT SO THE BIT CELL TIME IS ACTUALLY REDUCED AND THE FREQUENCY HAS TO BE HIGHER TO GET EQUIVELENT DATA RATE.

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2. DRIVE LEVEL OF DATA SIGNALS

- GIVEN THE LOSS IN THE CABLE WE COULD INCREASE DRIVE LEVEL OF THE SIGNALS.
- BUT ALREADY AT 800 MV MAX (NOT REALLY LOW VOLTAGE DIFFERENTIAL).
- SHOULD INCREASE TO MAX ALLOWED BY CHIP TECHNOLOGY SUBJECT TO EMI CONSIDERATIONS.

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3. ISI ON REQ AND ACK SIGNALS

- CURRENT SCSI REQ AND ACK SIGNALS USED BOTH AS FLOW CONTROL AND CLOCK.
- CAUSES REQ AND ACK TO START AND STOP CREATING LARGE ISI WHICH DISTORTS TIMING.
- WAY TO ELMINATE IS TO SEPARATE CLOCK AND FLOW CONTROL SIGNALS.
- P1 WILL BE REDEFINED AS FREE RUN CLOCK (SIGNAL NOT USED IN SPI-3).
- FREE RUN CLOCK ALWAYS DRIVEN FROM THE DATA SOURCE (ALLOWS EXPANDERS TO WORK).
- WILL HAVE SOME DELAY TO DATA TRANSFER DUE TO GETTING THE CLOCK GOING (MAY BE ZERO BASED ON PROTOCOL).
- ELIMINATES ISI ON CLOCK AND CREATES STABLE TIMING FOR THE RECEIVER.
- RECEIVER MUST STILL COPE WITH ISI (AND REFLECTIONS) ON THE DATA.

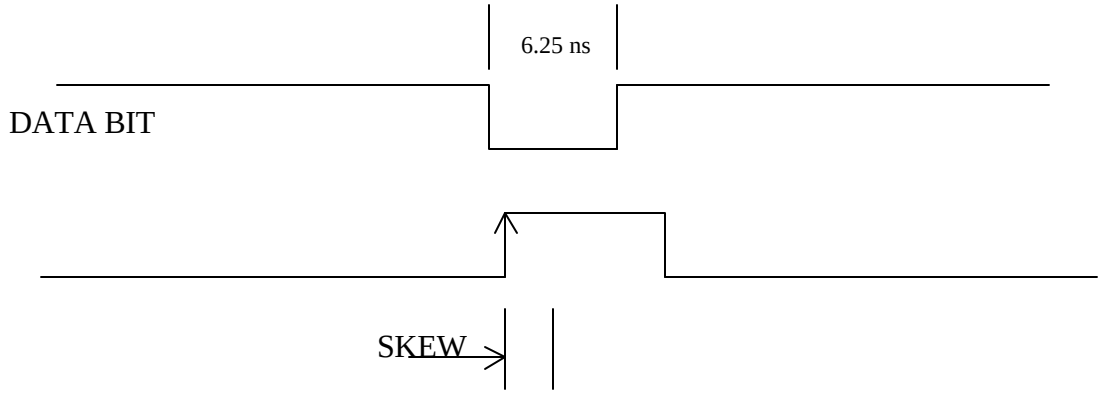
4. CABLE SKEW

SCSI IS PARALLEL TRANSMISSION SO CLOCK IS SENT ON SEPARATE WIRE FROM DATA.

FOR SMALL DATA CELLS DIFFERENCE IN DELAY BETWEEN CLOCK AND DATA CAN RESULT IN STROBE NOT OCCURING IN CENTER OF BIT.

FUNCTION OF DELAY DELTA BETWEEN WIRE PAIRS IN THE CABLE (TYPICAL IS 0.03-0.045 ns/ft OR 3.6 ns IN 25 METER CABLE).

NEED SOME FORM OF SKEW ADJUSTMENT TO ASSURE STROBE OCCURS IN THE CENTER OF THE DATA BITS ON ALL BITS TO ASSURE GOOD SETUP AND HOLD.



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4. CABLE SKEW

- SOLUTION IS TO USE A SKEW ADJUSTMENT CIRCUIT ON ALL LINES THAT CENTERS THE CLOCK FOR EACH DATA BIT.

- WILL REQUIRE A TRAINING SEQUENCE BEFORE THE START OF ANY DATA TRANSFER.

- IDEA OF A MICROPACKET WILL BE INTRODUCED AND IS DETAILED IN THE FOLLOWING SLIDES.

- THIS APPROACH WAS USED IN HIPPI. HIPPI IS A PARALLEL INTERFACE LIKE SCSI WHICH OPERATES MUCH FASTER (POINT TO POINT ONLY).

- THE SKEW ADJUSTMENT CAN BE DONE WITH MOSTLY DIGITAL LOGIC AND SHOULD REQUIRE AT MOST A SINGLE DLL LOOP TO GENERATE THE DIFFERENT CLOCK PHASES.

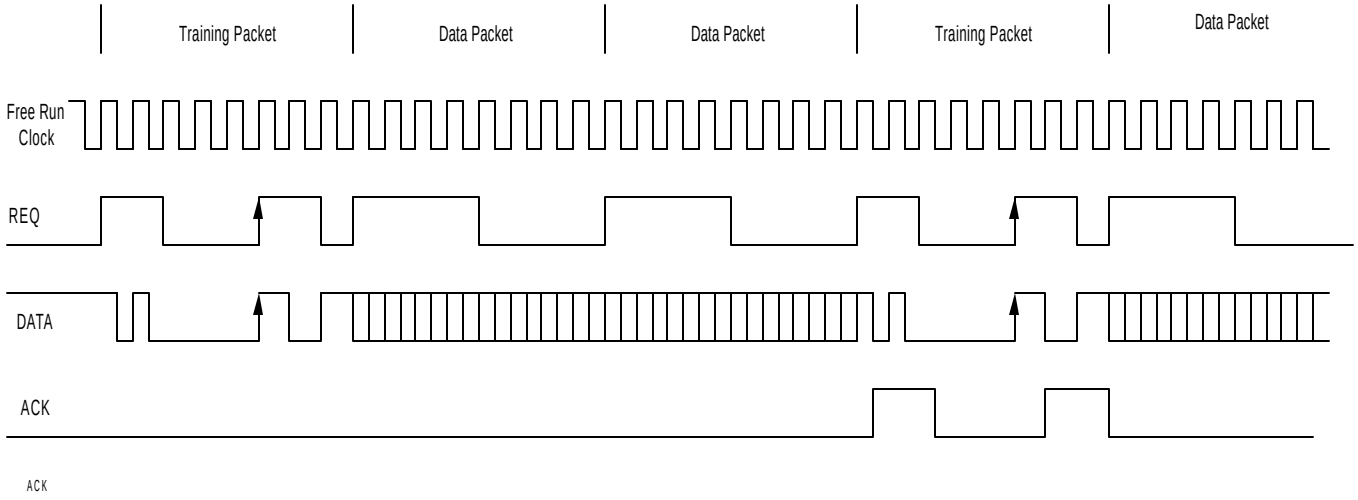
4. CABLE SKEW

MICROPACKETS

- DATA SENT IN 32 BYTE MICRO-PACKETS (16 BIT BUS).
- TRAINING PACKET USED FOR SKEW COMPENSATIION AND TO PAUSE DATA IF NO ACK RECEIVED.
- AT START OF TRANSMISSION TRAINING PACKET SENT BEFORE FIRST DATA PACKET.
- REQ AND ACK SIGNALS OPERATE ON MICRO-PACKETS NOT BYTES OF DATA.
- REQ AND ACK SIGNALS MOVE MUCH SLOWER (SLOWER THAN DATA) SO EASY DETECTION.

4. CABLE SKEW

- DATA TRASMISSION FOR DATA IN
- SKEW COMPENSATION PACKET INDICATED BY REQ SIGNAL (GOES TO ZERO BEFORE CLOCK STROBE 8).
- SKEW COMPENSATION ON CLOCK EDGE 11 OF PACKET.
- REQ AND ACK SIGNALS RUN MUCH SLOWER THAN CLOCK OR DATA SINCE THEY ARE PACKET BASED.
- FREE RUN CLOCK ALWAYS COMES FROM THE FROM DATA SOURCE.
- FREE RUN CLOCK NEEDS SOME TIME TO PHASE OR DELAY LOCK BEFORE TRAINING PACKET SENT.



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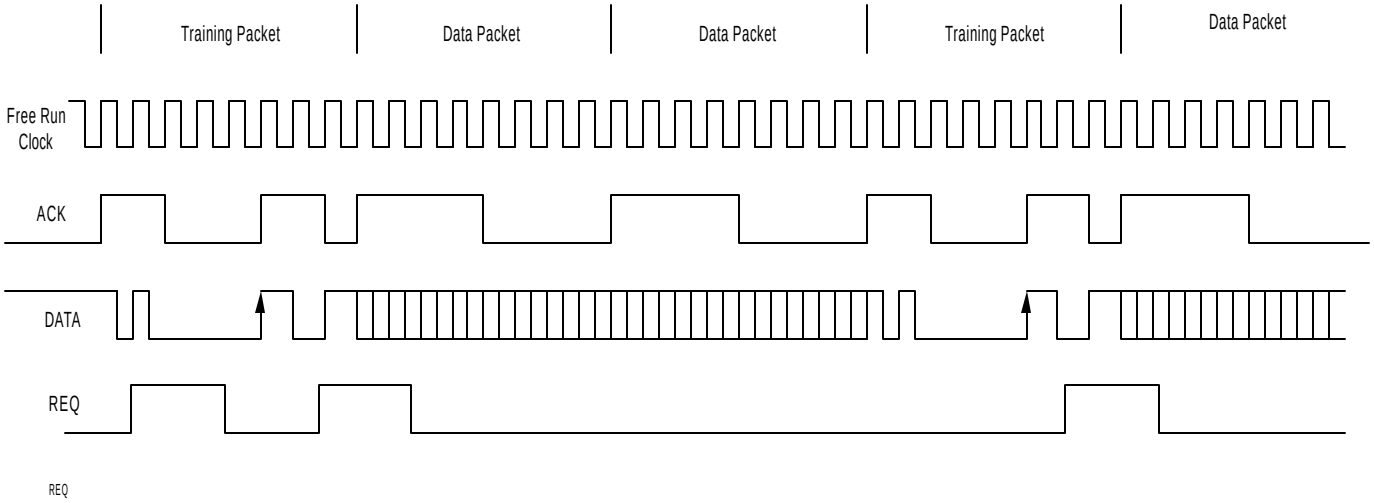
4. CABLE SKEW

- DATA TRASMISSION FOR DATA OUT
- SKEW COMPENSATION PACKET INDICATED BY ACK SIGNAL (GOES TO ZERO BEFORE CLOCK STROBE 8).
- SKEW COMPENSATION ON CLOCK EDGE 11 OF PACKET.
- REQ AND ACK SIGNALS RUN MUCH SLOWER THAN CLOCK OR DATA SINCE THEY ARE PACKET BASED.
- FREE RUN CLOCK ALWAYS COMES FROM THE FROM DATA SOURCE.
- FREE RUN CLOCK NEEDS SOME TIME TO PHASE OR DELAY LOCK BEFORE TRAINING PACKET SENT.



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5. ISI ON DATA SIGNALS

- ISI ON DATA AND ISSUE SINCE BIT N SUFFERS DISTORTION FROM PRIOR BITS.
- REQ AND ACK ARE NO LONGER FORCED TO TOGGLE AT DATA RATE SO NO ISSUE.

WAYS TO REDUCE ISI

NARROW BANDWIDTH OF DATA SIGNAL USING RUN LENGTH LIMITED ENCODING.
REDUCES DELAY DISTORTION SINCE BW OF THE SIGNAL IS CONTAINED.

BUT

INCREASES THE FREQUENCY OF THE BIT RATE FOR A GIVEN DATA RATE.

5. ISI ON DATA SIGNALS

WAYS TO REDUCE ISI

USE EQUALIZATION

EQUALIZATION CAN BE DONE IN MANY WAYS, AND CAN BE DONE AT THE TRANSMITTER, RECEIVER OR BOTH. EQUALIZATION REDUCES THE LOW FREQUENCIES AMPLITUDE TO COMPLEMENT THE CABLE OR LINE CHARACTERISTIC.

TRANSMITTER PRECOMP REDUCES THE DRIVE LEVEL IF THE SIGNAL STAYS AT A CONSTANT STATE. CAN RANGE FROM VERY COMPLEX TO VERY SIMPLE DEPENDING ON THE NUMBER OF CUTBACKS OF THE SIGNAL.

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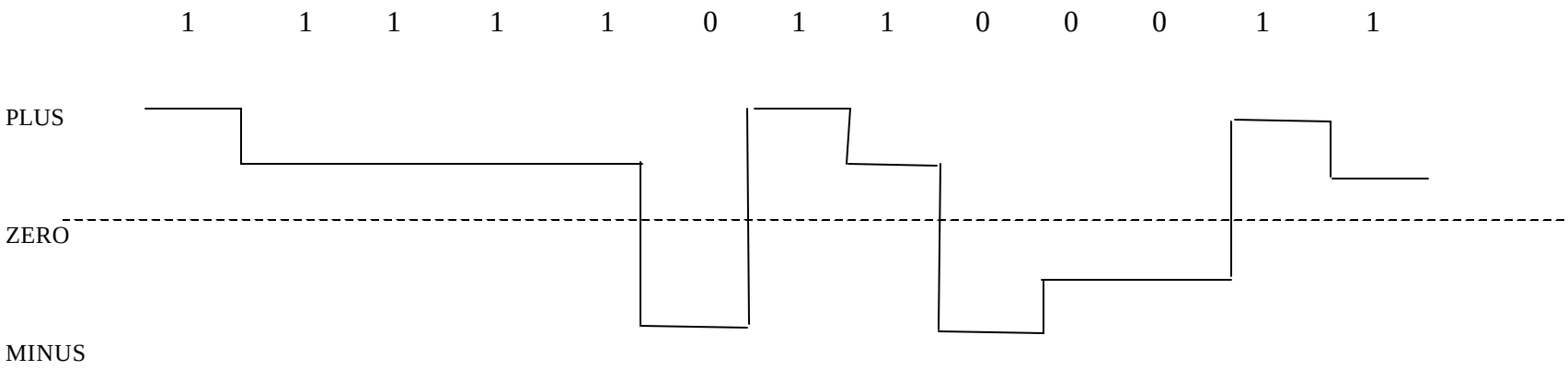
5. ISI ON DATA SIGNALS

WAYS TO REDUCE ISI (TRANSMITTER EQUALIZATION).



•ABOVE SHOWS A SIMPLE ONE STAGE CUTBACK OF THE DRIVE SIGNAL WHEN THE LEVEL STAYS THE SAME. THIS CAN BE EXPANDED TO A MULTISTAGE CUTBACK.

•THIS IS EASY WAY TO MITIGATE THE ISI PROBLEM AS DESCRIBED IN MANY PAPERS.

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5. ISI ON DATA SIGNALS

RISE TIME CONSIDERATIONS

- SOME PAPERS SUGGEST THE RISE TIME SHOULD BE NO LESS THAN 1/2 THE BIT WIDTH.
- IN OUR CASE WOULD BE A 3ns RISE TIME FOR 6.25 ns BIT CELL.
- FROM NEXT SLIDES THERE APPEARS TO BE SOME EYE IMPROVEMENT WITH LARGER RISE TIME.
- PROBLEM IS THE EYE IS MORE ROUNDED BUT IF SKEW COMPENSATION PUTS THE STROBE IN THE CENTER OF THE BIT THIS SHOULD NOT BE AN ISSUE.
- ALSO MAY MITIGATE EMI PROBLEMS.

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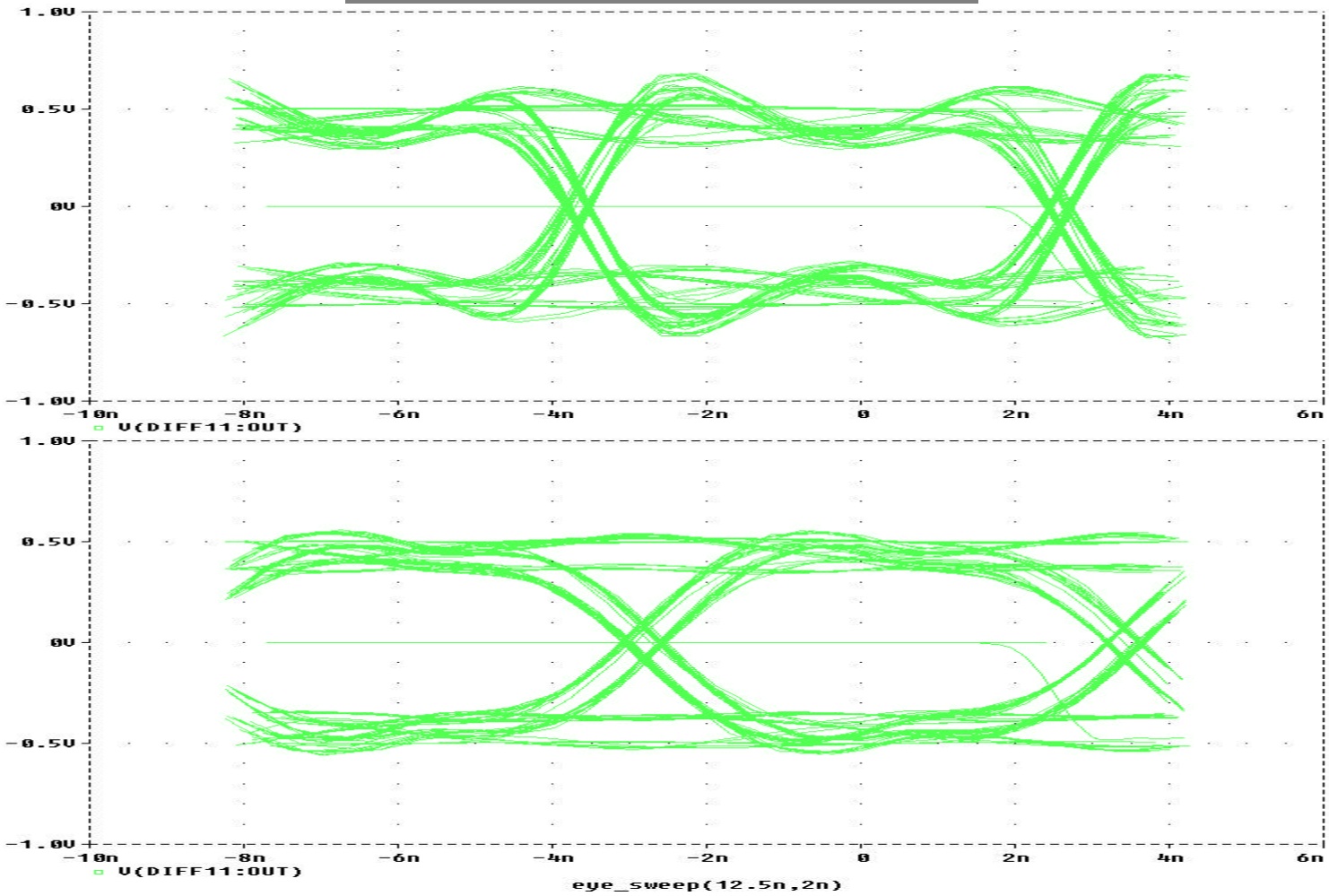
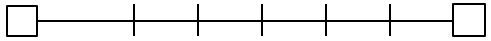


5 ft cable, 5 loads (10” spacing), random pattern ---------- $R_{T(beginning)} = R_{T(end)} = 60$ ohm,



eye at L1 (a) rise = 1.25 ns, (b) rise = 3 ns

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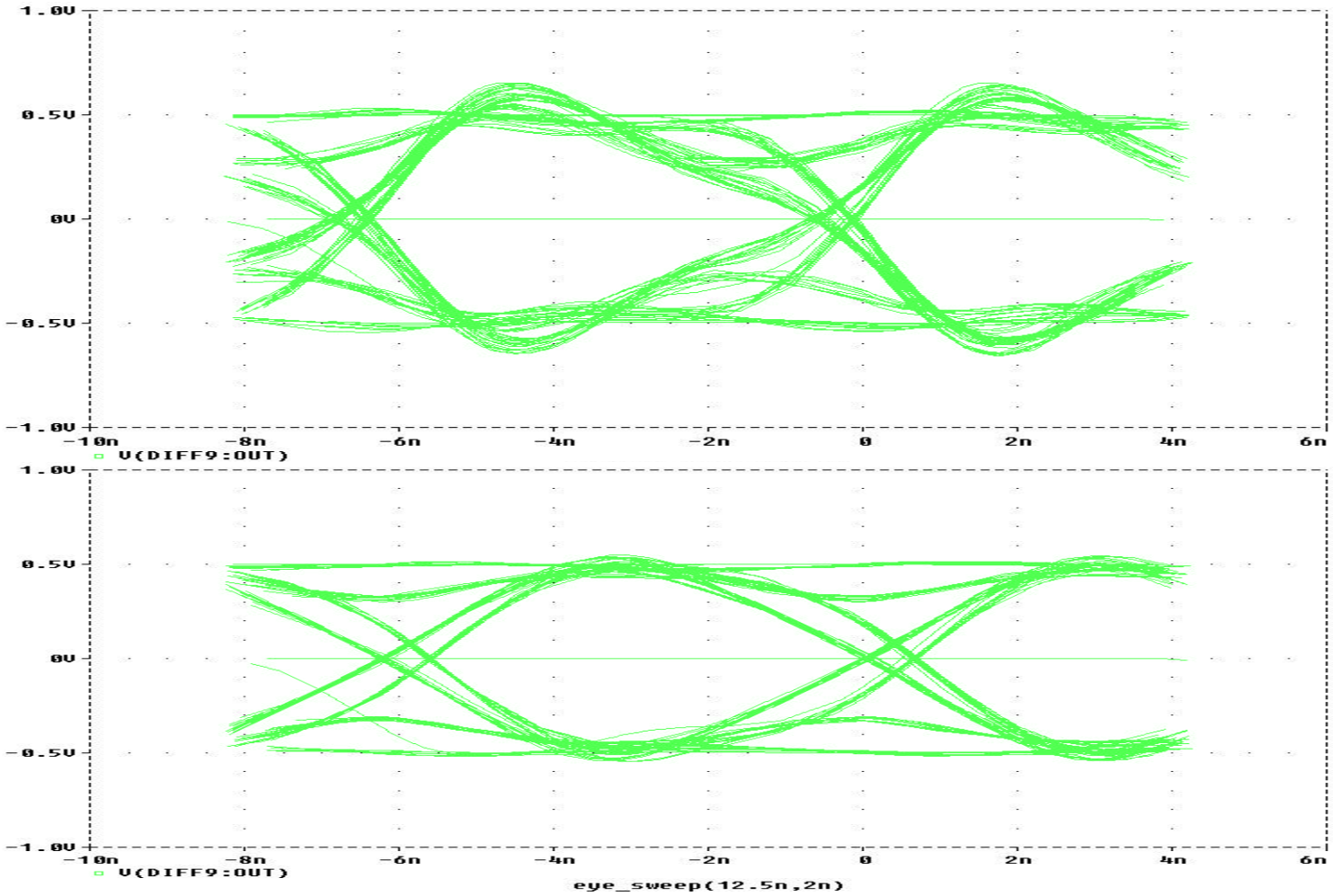
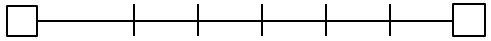


5 ft cable, 5 loads (10” spacing), random pattern ---------- $R_{T(beginning)} = R_{T(end)} = 60$ ohm,



eye at L3 (a) rise = 1.25 ns, (b) rise = 3 ns

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6. BIAS OF RECEIVER (FAIL SAFE BIAS).

PROBLEM

•SCSI NEEDS FAIL SAFE BIAS TO ASSURE WHEN NO ONE DRIVES THE DATA BUS RECEIVERS DETECT A NON ASSERTED STATE.

•THIS REPRESENTS A DC NOISE SOURCE TO THE DATA AND TIMING SIGNALS.

•COMPENSATED IN PRESENT SCSI BY USE OF EITHER AN ASYMETRIC DRIVE.

•THIS IS AN OPEN LOOP COMPENSATION AND IS NOT ACCURATE GIVEN TERMINATOR DIFFERENCES AND DRIVER ACCURACY. ALSO THE CANCELLATION IS DONE AT THE TRANSMITTER AND IF SIGNIFICANT CABLE RESISTANCE WILL NOT BE CORRECT.

•NEED A RECEIVER CLOSE LOOP COMPENSATION SCHEME.

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SUMMARY

•STRAW PROPOSAL:

USE FREE RUN CLOCK.
IMPLEMENT MICROPACKET WITH SKEW COMPENSATION.
IMPLEMENT TRANSMITTER PRE-COMPENSATION.
USE LONGER RISETIME WITH SKEW COMPENSATION.
IMPLEMENT RECEIVER DC BIAS COMPENSATION.
CONTINUE INVESTIGATION ON ENCODING.