The second meeting of the SCSI signal modeling study group was held in Manchester NH July 29.

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1. Introduction

Paul Aloisi of Unitrode opened the meeting and conducted the introductions and reviewed the meeting purpose. Paul also thanked Hitachi cable for hosting the meeting.

2. Attendance

The following people were in attendance:

Tariq Abou-Jeyab	Adaptec
Bill Ham	Compaq
Nicholaos Limberapoulas	C&M
John Ellis	FCI/BERG
Jackie Sylvia	Hitachi Cable
Larry Barnes	LSI Logic
Jie Fan	Madison Cable
Martin Ogbuokiri	Molex
Farbod Falakfarsa	Quantum
Andrew Bishop	Quantum
Ivan Chan	Quantum
Ken Plourde	Tempflex
Paul Aloisi	Unitrode
Johnathan Fasig	Western Digital

3. Agenda development

The agenda shown was used.

4.1 Host bus adapter model (Tariq Abou-Jeyab, Adaptec)

The following material was presented, internal connector, external connector, ASIC chip, terminator, and board construction. A discussion followed on the basic purpose of the simulation effort and the definitions of terms and concepts.

One area of consideration is the definition of the term "IBIS". IBIS is a behavioral model that is used to specify IO buffers inputs and outputs and can be used for termination also. Connector models are also being considered for an IBIS model. IBIS models do not include transmission lines or PCB's. For behavioral specifications the SCSI modeling study group will use only IBIS specification methodology for chip input, output, and terminator. For circuit type specifications no specific position was taken but it was generally agreed that something like "spice" will be used.

Tariq suggested that the microstrip and stripline constructions be considered as the basic options within the PCB. The details of these models are a primary part of the simulation requirements.

4.2 References useful for modeling and simulation (Jonathan Fasig, Western Digital)

Jonathan produced three useful lists of references, signal integrity publications, on-line bookstores and publishers, and other related on-line services. Jonathan took an action item to send the lists electronically to Bill Ham for posting.

4.3 Difference between simulated and measured TDR traces (Martin Ogbuokiri, Molex)

Martin presented real data from a connector and an attempt to simulate the same measurement using a discrete lumped circuit model. There was approximately a 3x difference between the measured and calculated results in terms of the time extent of the connector. The amplitude features however agreed within 4% (peak to peak only).

The recommendations are, use only peak to peak results to validate the simulated results. Ignore the timing features of the results. Do not use the average impedance (over time) values. Better agreement could be obtained if the multiple reflection due to the discontinuities in the test fixture and the connector were included in the model. Presently it requires special expertise to use the spice tool for simulating multiple reflections due to the need to input many details of the physical test environment.

Martin has an action item to supply a block diagram of the simulation process used to do the simulation.

4.4 Transmission line coupling parameters (Larry Barnes, LSI Logic)

Larry presented the results of a comprehensive simulation relating to the intensity of backwards crosstalk as a function of distance from a conductor. This models was a first cut at understanding the issue. Two items that need to be added to this approach are using differential signals and including ground lines where they exist in SCSI. One major result of this work was a very rapidly decreasing coupling with spacing. Another possible result was an extended residual inductive coupling. This is probably due to the way the ground returns were specified in the model. If the extended residual inductive coupling is truly significant it could indicate more crosstalk but that conclusion needs to be validated.

5. Output of the group

The effort will produce three types of output: (1) reports to the SCSI working group, (2) a document containing the technical details, exact type of document TBD and, (3) a web based repository for specific models.

Larry Barnes volunteered to be the editor for the document.

6. SFF backplane

Bill Ham noted this activity is still planned but not yet started.

7. Components to be modeled

7.1 Cable assemblies

The cable assembly consists of : media, connectors, and transition region between pure media and connector termination.

7.1.1 Cable media (bulk cable)

Discussed at June meeting.

7.1.2 Connectors (on cable assemblies)

A model similar to that used for cable media was suggested. A more general version is required for an actual SCSI connector having many contacts. This model would have the same general form as the model for the cable media. The discussion focused on the circuit model approach. A behavioral model may also be attractive but no direction was taken at this meeting. The integration of connector, chip, media, into a single simulation is a major point of interest for this group.

7.1.3 Transition region

The transition region is that part of the cable assembly that is between the connector itself and the undisturbed cable media. This region has not been modeled previously and no models or approaches are currently available. It was agreed that people who do the cable assembly design and manufacturing should be the source of the simulation parameters for this part of the interconnect.

7.2 PCB's

Dean Wallace to provide a target board model. Suggested that the following items be added: vias, discontinuities, signal over discontinuities.

7.3 Connectors for non-cable applications

At this point there is no difference between these connectors and connectors used for cable applications. Molex will supply RGL transmission line matrix for VHDCI, SCA-2, and HD68 connectors.

7.4 Termination

Addressed in the June meeting.

7.5 Transceivers

Due to the proprietary nature of transceiver design only behavioral models will be attempted.

7.5.1 Chip packages

Not discussed at this meeting.

7.5.2 Access to actual measurement points

Not discussed at this meeting.

8. Simulation integration strategy

Significant discussion on how to integrate the simulations from the different interconnect and chip elements since different simulation specification types are used for the different elements. The common approach seems to be a circuit specification approach.

This requires behavioral specifications to be converted into a circuit model. The simulation strategy currently is: IBIS models for the IO buffers and SCSI terminators and a spice model for the cable media, connectors, PCB, and cable assembly transition regions. It is possible to create circuit models from some behavioral tools and vice versa, this allows tailoring the specific simulations to the nature of the specific problem.

An important goal and output for this work is a set of building blocks that everyone can use. For example, transceiver cells, package leads and bond wires etc., connectors, cable media, terminators, PCB's and the like. The integration of these building blocks into a simulation strategy for several parts of the SCSI bus is a second phase for the effort. The third phase is to ensure commonality between simulation input needs and the parameters available from the component suppliers. The reverse is also important: going from simulated performance needs to parameters controllable by the component supplier. The specific action is to agree on a way to translate between needed parameters for simulation and the parameters available from physical measurement methods and specifications.

9. System configurations

Not discussed at this meeting.

10. Data Patterns

Not discussed at this meeting.

11. Data Rate

Not discussed at this meeting.

12.1 Physical measurement points

Not discussed at this meeting.

13. Definitions

Not discussed at this meeting.

14. Tools

   Not discussed at this meeting

   14.1 Behavioral

      Not discussed at this meeting.

   14.2 Circuit
      Not discussed at this meeting.

The future meeting schedule is:

Sept 01, 1999 Colorado Springs (Embassy Suites)
Sept 29, 1999 Chicago (Lisle) at Molex plant.

Regards Dean Wallace Qlogic Corporation