Date: July 13, 1999
To: T10 Committee
From: Richard Moore (QLogic Corporation)
Subject: Release Glitch Management for QAS (99-191r1)

1. Background

At the May SPI-3 Working Group meeting it was pointed out that Table 23 in SPI-3 rev 5, which describes release glitch management, does not provide for glitch management during QAS. (In fact, April's Working Group pointed out that the table was not applicable to QAS but it was not certain whether glitch management was covered in the QAS protocol. It is now ascertained that QAS will require release glitch management).

The phase control lines (MSG, C/D, and I/O) already contain release glitch management measures. The first measure is the requirement for the disconnecting target to release these lines within a QAS release delay (200 ns) of detecting SEL true, ensuring that the release glitches on these signals will be gone within 800 ns of the assertion of SEL. The second measure is the requirement for the winning device to wait a QAS arbitration delay (1000 ns) after asserting SEL, before changing any other bits (including asserting the ID of the device it wants to select). This ensures that the selected device doesn't see the release glitch on I/O as an indicator of a reselection when a selection is intended. However, Table 23 does not take these existing measures into account and should be made compatible with QAS.

10.2.2.1 (SPI-3 rev 7) calls for the target to release REQ directly from the asserted state. This is implied in item c in the list under "procedure for a target to indicate it wants to release the bus". The intention is to have the target actively negate REQ at the end of the QAS message. This section will need to be changed to state this requirement and release glitch management for REQ during QAS will need to be defined. This proposal provides release glitch management for ACK and ATN.

2. Proposal

This proposal adds release glitch management for ACK, ATN, and REQ, and provides additional clarifications.

1. Change the caption of Table 23 from "Non-QAS glitch management requirements for SCSI devices using LVD drivers" to "Glitch management requirements for SCSI devices using LVD drivers". Delete the Editor's Note at the bottom of the table.

2. Change "ACK, ATN" in the first column of Table 23 to "ACK, ATN during transitions to BUS FREE".

3. Add this row after the "ACK, ATN during transitions to BUS FREE" row in Table 23:

ACK, ATN during QAS	I	R	The initiator shall wait until two system deskew delays after it detects C/D, I/O, and MSG false before releasing the ACK and ATN signals from the actively negated state.	Starting no later than two system deskew delays after negating C/D, I/O, and MSG, the target shall ignore the ACK and ATN signals until a subsequent connection.

4. Change "REQ" in the first column of Table 23 to "REQ during transitions to BUS FREE".

5. Add this row after the “REQ during transitions to BUS FREE” row in Table 23:

REQ during QAS	T	R	The target shall wait two system deskew delays after negating C/D, I/O, and MSG before releasing the REQ signal from the actively negated state.	Starting no later than two system deskew delays after detecting C/D, I/O, and MSG false, the initiator shall ignore the REQ signal until a subsequent connection.

6. Change “C/D, I/O, MSG” in the first column of Table 23 to “C/D, I/O, MSG except during SELECTION and RESELECTION phases of QAS”.

7. Add this row after the “C/D, I/O, MSG except during SELECTION and RESELECTION phases of QAS” row in Table 23:

C/D, I/O, MSG during SELECTION and RESELECTION phases of QAS	T	P	After detecting SEL true following QAS arbitration, the target shall release these signals within a QAS release delay.	No glitch management required.

8. Make the following changes in 10.2.2.1, “QAS phase” under “The procedure for a target to indicate it wants to release the bus”:
   a. Change item (c) as follows: “After detection of the last ACK signal being true and if there is no attention condition, the target shall negate REQ. After detection of the last ACK signal being false, the target shall release all SCSI signals except the BSY, MSG, C/D, I/O, and REQ signals and shall negate the MSG, C/D, and I/O signals within two system deskew delays. The target shall wait two system deskew delays after negating the C/D, I/O, and MSG signals before releasing the REQ signal.”
   b. Add the following note after item (f): “NOTE 32 - The release of MSG, C/D, and I/O may cause release glitches; this requirement ensures these glitches occur at a time when no connection is established on the bus so that they do not interfere with proper operation.”
   c. Editorial change: Change “asserted” to “true” in both places in item (f). Also, change “delay, if” in this item to “delay. If”.
9. Editorial change: Under “The procedure for an SCSI device to obtain control of the SCSI bus” in 10.2.2.1, in item (C) of the list under item (d), change “asserted” to “true”.