SPI-3, rev 7, Section 7 Table and Figure Clarification

- **Table 15 appears to be the extreme cases whenever a device is not included in the subclauses of section 7. Is this statement clear enough?**
  The statement says:
  > **"In addition to the device electrical requirements defined in the remaining subclauses of this clause, devices shall meet the requirements specified in table 15 and table 16 at the device connector."**

  To give it more emphasis, it should say:
  > ***"Devices that do not meet the electrical requirements defined in the remaining subclauses of this clause shall not violate the extreme conditions shown in Table 15 and Table 16 at the device connector."***

  This better indicates that Tables 15 and 16 are the absolute boundary conditions expected. Does this also mean *Anywhere* on the bus? Then state it.

- **The note in Table 15 and Table 25 states: "LVD/MSE SCSI devices may be damaged by the DIFFSENS voltage from HVD devices". How? If LVD/MSE devices clamp their inputs above Vdd, then worst case current into the clamping device would be 5.5V ÷ 1000 ohms, or 5.5mA. Is the HVD device expected to generate 15V transients on the DIFFSENS line that last long enough to cause catastrophic amounts of clamping energy?**

Table 15 - Electrical input requirements at the device connector

Mode	Minimum	Maximum	Notes
SE (passive negation) input voltage	-0,5 V D.C.	5,5 V D.C.	Absolute maximum at all operating conditions, SCSI devices meeting the passive negation requirements in table 17.
SE (active negation) input voltage	-0,5 V D.C.	4,1 V D.C.	Absolute maximum at all operating conditions, for SCSI devices meeting the active negation requirements in table 17.
LVD/MSE input voltage (D.C. V + or - signal to local ground)	-0,5 V D.C.	4,1 V D.C.	Absolute maximum at all operating conditions all signals except DIFFSENS.
DIFFSENS for LVD/MSE input voltage	-0,5 V D.C.	4,1 V D.C.	Absolute maximum at all operating conditions for the DIFFSENS connection.
Note: LVD/MSE SCSI devices may be damaged by DIFFSENS voltage from HVD devices.			

- **It must be inferred from Table 15 that the maximum any *pin* will see at its input is controlled by the mode of that particular *pin.* Some SE device *pins* could see passive negation and some could see active negation. Is a device expected to continuously clamp a 5.5V line when it is operating with a Vdd of 3.3 volts? If so, then the 99-187 load line needs to consider very high current *sources.* A statement needs to be added to discourage this catastrophic failure mode; either from the perspective of the current source, the current sink, or both.**

- **How is an LVD/MSE device expected to react to a passively negated device on the bus? The assumption is made that a passively negated device sources very little current. Where is this stated?**

- **As 99-187 will change V_{in} to < 3.01V, in Table 16, how is it assumed that MSE devices will have a Vdd of 3.3V or less? Does this statement need to be added somewhere?**

Table 16 - Input current requirements at the device connector for lines not being driven by the device

Value	Maximum	Notes
MSE current magnitude	± 20 µA D.C.	Measured from + or - signal 0 < V_{IN} < 4,1 V to local ground for each signal pin.
LVD current magnitude	± 20 µA D.C.	Measured from + or - signal V_{IN} < 2,5 V to local ground for each signal pin.

- **Table 16 assumes we understand the difference between MSE and SE. A note should state that MSE is different from SE due to technology implementation differences. Otherwise, why isn't SE also shown in Table 16? Where is the reference to SE's leakage current which is comparable to the MSE in Table 16? *(and not what's shown in Table 18 and 19!)***

- **The title of Table 16 should read:**
  "Input leakage current requirements ..."

- **Figure 26 shows a possibility of 7mA between 3.24V and 3.70V. To further encourage designers to not source current above a supply rail of 3.3V, add a statement that says:**
  "It is desirable for LVD/MSE drivers to not source current above a V_{oh} of 3.0 volts."
  (maybe 99-187r1 already makes this clear)

Table 18 - SE input voltage characteristics

Maximum transfer rate	SE input voltage characteristics
Fast-5	a) VIL (low-level input voltage) = 0,0 V D.C. to 0,8 V D.C. (signal true); b) VIH (high-level input voltage) = 2,0 V D.C. to 5,25 V D.C. (signal false) c) IIL (low-level input current) = - 0,4 mA to 0,0 mA at VI = 0,5 V D.C.; d) IIH (high-level input current) = 0,0 mA to 0,1 mA at VI = 2,7 V D.C.; e) Minimum input hysteresis = 0,2 V D.C.
Fast-10	a) VIL (low-level input voltage) = 0,0 V D.C. to 0,8 V D.C. (signal true); b) VIH (high-level input voltage) = 2,0 V D.C. to 5,25 V D.C. (signal false) c) IIL (low-level input current) = ± 20 µA at VI = 0,5 V D.C.; d) IIH (high-level input current) = ± 20 µA at VI = 2,7 V D.C.; e) Minimum input hysteresis = 0,3 V D.C.
Fast-20	a) VIL (low-level input voltage) = 1,0 V D.C. maximum (signal true); b) VIH (high-level input voltage) = 1,9 V D.C. minimum (signal false) c) IIL (low-level input current) = ± 20 µA at VI = 0,5 V D.C.; d) IIH (high-level input current) = ± 20 µA at VI = 2,7 V D.C.; e) Minimum input hysteresis = 0,3 V D.C.
Note: 1 SE input voltage characteristics specified by the maximum transfer rate shall apply even if a slower transfer rate is negotiated. 2 Due to the tighter voltage thresholds for fast-20, the power supply should have a maximum ±5% tolerance of the nominal voltage. 3 All values apply to both active negation and passive negation devices.	

- **In note 2 of Table 18, what is the *nominal* voltage and how does this relate to 3.3V devices?**

- **Combine Table 18 and Table 19 into a unified, SE spec. There is much duplicate information between these two tables. Either combine the information into one table, or change the titles of each table to give more precise understanding as to their separate uniqueness.**

Table 19 - SE input and output electrical characteristics

Maximum transfer rate	SE input and output electrical characteristics
Fast-5	a) Maximum signal capacitance = 25 pF, measured at the beginning of the stub (see figure 4).
Fast-10	a) I_L (Leakage current) = -20 µA to + 20 µA at V_I = 0,0 V D.C. to 5,25 V D.C. (high-impedance state); b) Maximum signal capacitance = 25 pF, measured at the beginning of the stub (see figure 4).
Fast-20	a) I_L (Leakage current) = -20 µA to + 20 µA at V_I = 0,0 V D.C. to 4,1 V D.C. (high-impedance state); b) Maximum signal capacitance = 25 pF, measured at the beginning of the stub (see figure 4).

Note:
1 SE input and output voltage characteristics specified by the maximum transfer rate shall apply even if a slower transfer rate is negotiated.
2 All values apply to both active negation and passive negation devices.

- **The Fast5 voltage/current characteristics should be carried forward from older specs into this new document which is replacing those older references.**

- **7.3.5 should say: “HVD is not defined in this standard. *HVD is no longer supported and could cause damage to LVD and multi-mode devices if connected to the SPI-3 configured SCSI bus.”***

  7.3.5 SE/HVD transmission mode detection
  HVD is not defined in this standard. For information on HVD SCSI device implementation see the SCSI Parallel Interface-2 Standard (X3.302-1998).
  Transmission mode detection by LVD SCSI devices of SE and HVD SCSI devices is accomplished through the use of the DIFFSENS line. Requirements for SCSI devices and terminators for DIFFSENS are not the same as for "signal" lines because DIFFSENS is driven and detected using its own ~~SE~~ transmission and detection scheme.

- **Remove “SE” from the statement in 7.3.5 because it implies that DIFFSENS is somehow part of the SE bus signaling scheme and not a variable, analog voltage. It was probably intended to mean that the line is a non-differential line, but this could prove confusing with all the other “SE” references in the spec.**
  To state it more precisely say: “...because DIFFSENS is *an analog voltage line which uses* its own transmission and detection scheme.”