To: T10 Technical Committee
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Subject: Change CRC timing values

Revision 2: source numbers updated to match spi3r06. Adjusted new Periods per reflector discussions. Addressed tighter pCRC Receive Hold Time issue. Addressed 10 ns extra Transmit Setup Time issue. Addressed ISI issue. Added chapter 10 changes.

The extra 10 ns setup time accorded P_CRCA can cause problems for some expander designs. When P_CRCA is transitioning, the transmitter (the target) is only required to assert REQ for the minimum of:

a) the Transmit Assertion Period or Transmit Negation period (whichever is applicable), or
b) the pCRC Transmit Hold Time plus the pCRC Transmit Setup Time.

With the current pCRC timing numbers, the Hold Time + Setup Time is longer than the Assertion or Negation period. For normal data transfers, the Assertion Period or Negation Period is always longer than the Hold Time + Setup Time. We would like to guarantee some extra assertion or negation time when P_CRCA is transitioning so it works like normal data transfers. This should be compatible with existing implementations (at Fast-80DT and Fast-40DT), because they generate a pause based on an 80 or 160 MHz clock.

99-183r1, Slow DT Timings, did not raise the pCRC Transmit setup and hold times for Fast-10DT, Fast-20DT, and Fast-40DT as it did for the normal Transmit setup and hold times, but did apply the new interconnect budget to them to create new pCRC Receive setup and hold times. One effect was to make the pCRC receive hold time tighter than the normal hold time.

Additionally, the extra 10 ns setup time seems incorrectly documented. Both the Receive and Transmit Setup Times are 10 ns more than normal. This means there is no additional time budgeted for the interconnect. The reason for the extra time is to tolerate the P_CRCA signal having a slower transition time that the DB signals because it is not toggling as often. To accomodate this problem, the transmitter needs to provide extra setup time, but the receiver cannot expect any additional setup time. Since current implementations may have relaxed their Receive Setup Time requirements based on the original specifications, we suggest trimming away only 3 ns for the interconnect, holding the extra Transmit Setup time at 10 ns and reducing the Receive Setup Time to 7 ns.

Option 3 (revision 0 had Options 1 and 2, both abandoned)(original values are from spi3r06)
These changes are suggested:

- Create new minimum assertion and negation periods for REQ when P_CRCA is transitioning. The new numbers for Fast-80DT and Fast-40DT are based on the assumption that a 12.5 ns delay was added. The new numbers for Fast-10DT and Fast-20DT are just slightly increased, due to existing implementations.
- Make the pCRC Receive Hold Time match the Receive Hold Time.
- Restore the “10 ns extra” for pCRCA Transmit Setup vs Transmit Setup.
- Remove 3 ns from the pCRC Receive Setup Time to account for ISI between transmitter and receiver.

Table 32	Fast-10DT	Fast-20DT	Fast-40DT	Fast-80DT
DB and P_CRCA Timing Requirements				
Receive Hold Time	11,6	5,8	2,9	1,45
Receive Setup Time	11,6	5,8	2,9	1,45
algorithm: 2x per speed decrease. Fast-80DT is tightest ASIC timing possible today.				
(receive hold + setup)	*23,2*	*11,6*	*5,8*	*2.9*
Transmit Hold Time	38,4	19,2	9,6	4,8
Transmit Setup Time	38,4	19,2	9,6	4,8
algorithm: 2x per speed decrease. Let interconnect skew eat up budget				
(transmit hold + setup)	*76,8*	*38,4*	*19,2*	*9.6*
Nominal hold + setup time	*100 ns*	*50 ns*	*25 ns*	*12.5 ns*
Nominal 12.5 ns periods (h/s)	*4/4*	*2/2*	*1/1*	*0/0*
Interconnect budget	*26,8 ns*	*13,4 ns*	*6,7 ns*	*3,35 ns*
pCRC Receive Hold Time	~~10,2~~11,6	~~5,1~~5,8	~~2,55~~2,9	1,45
pCRC Receive Setup Time	~~20,2~~18,6	~~15,1~~12,8	~~12,55~~9,9	~~11,45~~8,45
algorithm: hold = Receive time; setup = Receive time + 7 ns change: made pCRC Receive Hold = Receive Hold (previously Transmit Hold - 10) change: made pCRC Receive Setup = Receive Setup + 7 (previously + ~10)				
(pCRC receive hold + setup)	*~~30,4~~30,2*	*~~20,2~~18,6*	*~~14.9~~12,8*	*~~12.9~~9,9*
pCRC Transmit Hold Time	~~37~~38,4	~~18,5~~19,2	~~9,25~~9,6	4,8
pCRC Transmit Setup Time	~~47~~48,4	~~28,5~~29,2	~~19,25~~19,6	14,8
algorithm: hold = Transmit time; setup = transmit time + 10ns change: made pCRC Transmit Hold = Transmit Hold (previously Transmit Setup – 10) change: made pCRC Transmit Setup = Transmit Setup + 10 (previously + ~10)				
(pCRC transmit hold + setup)	*~~84~~86,8*	*~~47~~48,4*	*~~28.5~~29,2*	*19.6*
nominal hold + setup	*100 ns*	*50 ns*	*32.5 ns*	*25 ns*
number of 12.5 ns periods (h/s)	*4 / 5*	*2 / 3*	*1 / 2*	*0 / 2*
Interconnect budget	*26,8 ns*	*13,4 ns*	*6,7 ns*	*3,35 ns*
REQ/ACK Timing Requirements				
Receive Assertion Period	80	40	20	10
Receive Negation Period	80	40	20	10
algorithm: 2x per speed decrease				
Transmit Assertion Period	92	46	23	11,5
Transmit Negation Period	92	46	23	11,5
algorithm: 2x per speed decrease				
Nominal period	*100 ns*	*50 ns*	*25 ns*	*12,5 ns*
Number of 12.5 ns periods	*8*	*4*	*2*	*1*
REQ/ACK Interconnect budget	*12 ns*	*6 ns*	*3 ns*	*1,5 ns*
Receive REQ Assertion Period with P_CRCA transitioning	85,5	~~-~~48	32,5	22.5
Receive REQ Negation Period with P_CRCA transitioning	85,5	48	32,5	22.5
Transmit REQ Assertion Period with P_CRCA transitioning	97,5	54	35,5	24
Transmit REQ Negation Period with P_CRCA transitioning	97,5	54	35,5	24
Nominal period	*112,5 ns*	*62,5 ns*	*37,5 ns*	*25 ns*
Number of 12.5 ns periods	*9*	*5*	*3*	*2*
REQ/ACK Interconnect budget	*12*	*6*	*3*	*1,5*
algorithm: original period + 12.5 ns				

9.2.20 Receive assertion period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.xx Receive REQ assertion period with P_CRCA transitioning

Tthe minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA is transitioning with pCRC protection enabled.

9.2.22 Receive negation period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.xx Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving an REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA is transitioning with pCRC protection enabled.

9.2.34 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

9.2.xx Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

9.2.36 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

9.2.xx Transmit REQ negation period with P_CRCA transitioning

The minimum time that a target shall negate the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

10.5.2.2.2 Data Group data field transfer

If the I/O signal is true (transfer to the initiator), to transfer the data field the target:
1) Shall drive the DB(15-0) signals to their desired values and shall negate the P_CRCA signal;
2) shall wait at least the longer of a pCRC transmit setup time from the negation of P_CRCA or a transmit setup time from DB(15-0) being driven with valid data;
3) shall transition the REQ signal;
4) shall hold the DB(15-0) signals valid for a minimum of a transmit hold time and shall hold the P_CRCA signal for a minimum of a pCRC transmit hold time;
5) may change or release the DB(15-0) and P_CRCA signals; and
6) shall not change the REQ signal for ~~a minimum of~~ at least a transmit assertion period if asserted or a transmit negation period if negated.

If the I/O signal is true (transfer to the initiator), to receive the data field the initiator shall:
1) Read the value on the DB(15-0) ~~and P_CRCA~~ signals within a receive hold time of the transition of the REQ signal; ~~and~~
1.5) Read the value of the P_CRCA signal within a pCRC receive hold time of the transition of the REQ signal; and

2) respond with an ACK transition.

If the I/O signal is false (transfer to the target), to transfer the data field the initiator:
1) Shall after detecting a REQ transition with P_CRCA negated;
2) shall drive the DB(15-0) signals to their desired values;
3) shall delay at least a transmit setup time;
4) shall transition the ACK signal;
5) shall hold the DB(15-0) signals valid for at least a transmit hold time;
6) shall not change the ACK signal for ~~a minimum of~~at least a transmit assertion period if asserted or a transmit negation period if negated; and [also, swap 6 and 7]
7) may then change or release the DB(15-0) signals.

If the I/O signal is false (transfer to the target), to receive the data field the target:
1) Shall read the value of the DB(15-0) signals within a receive hold time of the transition of the ACK.
2) shall not transition the REQ signal when the P_CRCA signal is asserted for the current data group until the initiator has responded with all ACK transitions for the previous data groups.

10.5.2.2.2.1 Data Group Pad field and pCRC field transfer to initiator
The target determines a pad field is required if the I/O signal is true (transfer to the initiator), the target has completed the data field transfer of the current data group, and REQ signal is asserted. In this case the target shall:
1) Wait at least one pCRC transmit hold time since the last REQ assertion to assert P_CRCA;
2) wait at least one transmit hold time since the last REQ assertion to assert the DB(15-0) signals to their desired pad values;
~~2) assert the P_CRCA signal and drive the DB(15-0) signals to their desired pad values;~~
3) wait at least the longer of a ~~one~~ pCRC transmit setup time from the negation of P_CRCA or a transmit setup time from DB(15-0) being driven with valid pad data;
4) wait until the initiator has responded with all ACK transitions for the previous data group;
4.5) wait at least one Transmit REQ Assertion Period with P_CRCA Transitioning since the last REQ assertion;
5) negate the REQ signal;
6) hold the DB(15-0) signals valid for a minimum of one transmit hold time and hold the REQ signal negated for a minimum of a transmit ~~assertion~~ negation period;
7) drive the DB(15-0) signals to their desired pCRC values;
8) wait at least one transmit setup time;
9) assert the REQ signal;
10) hold the DB(15-0) signals for a minimum of one transmit hold time and hold the REQ signal asserted for a minimum of a transmit assertion period;
11) drive the DB(15-0) signals to their desired pCRC values;
12) wait at least one transmit setup time;
13) negate the REQ signal; and
14) hold the DB(15-0) signals for a minimum of one transmit hold time and hold the P_CRCA signal asserted for at least a pCRC transmit hold time.
11) hold the REQ signal negated for at least one Transmit REQ Negation Period with P_CRCA Transitioning since the last REQ negation

If the target determines no pad field is required (i.e., the REQ signal is negated) the target shall:
1) Wait at least one pCRC transmit hold time since the last REQ negation to assert P_CRCA;
2) wait at least one transmit hold time since the last REQ negation to assert the DB(15-0) signals to their desired pCRC values;
~~2) assert the P_CRCA signal and drive the DB(15-0) signals to their desired pCRC values;~~
3) wait at least the longer of ~~one~~ a pCRC transmit setup time from the negation of P_CRCA or a transmit setup time from DB(15-0) being driven with valid pCRC data;;
4) wait until the initiator has responded with all ACK transitions for the previous data group;

4.5) wait at least one Transmit REQ Negation Period with P_CRCA Transitioning since the last REQ negation;
5) assert the REQ signal;
6) hold the DB(15-0) signals for a minimum of one transmit hold time and hold the REQ signal asserted for a minimum of a transmit assertion period;
7) drive the DB(15-0) signals to their desired pCRC values;
8) wait at least one transmit setup time;
9) negate the REQ signal; and
10) hold the DB(15-0) signals for a minimum of one transmit hold time and hold the P_CRCA signal asserted for a minimum of one pCRC transmit hold time.
11) hold the REQ signal negated for at least one Transmit REQ Negation Period with P_CRCA Transitioning since the last REQ negation