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To: T10 Technical Committee
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Subject: Change CRC timing values

The extra 10 ns setup time accorded P_CRCA can cause problems for some expander designs. When P_CRCA is transitioning, the transmitter (the target) is only required to assert REQ for the pCRC Transmit Hold Time plus the pCRC Transmit Setup Time. For normal data transfers, the Transmit Assertion Period or Transmit Negation Period (whichever is applicable) is longer than the combined Transmit Hold and Transmit Setup times. We would like to guarantee some extra assertion or negation time.

Existing implementations probably generate the extra pause as a multiple of the fundamental data period. For Fast-80DT, the pause would be a multiple of 12.5 ns or 25 ns. Requiring 12.5 ns extra shouldn't break any existing implementations.

Option 3 (excerpts are from spi3r05)
Lengthen the minimum assertion and negation periods for REQ when P_CRCA is transitioning.
Note: reapply the algorithm to the latest accepted Slow DT timings.

Table 32	**Fast-10DT**	**Fast-20DT**	**Fast-40DT**	**Fast-80DT**
Receive Hold Time	25	11,5	4,75	1,45
Receive Setup Time	25	11,5	4,75	1,45
(receive hold + setup)	*50*	*23*	*9.5*	*2.9*
Transmit Hold Time	37	18,5	9,25	4,8
Transmit Setup Time	37	18,5	9,25	4,8
(transmit hold + setup)	*74*	*37*	*18.5*	*9.6*
pCRC Receive Hold Time	25	11,5	4,75	1,45
pCRC Receive Setup Time	35	21,5	14,75	11,45
(pCRC receive hold + setup)	*60*	*33*	*19.5*	*12.9*
pCRC Transmit Hold Time	37	18,5	9,25	4,8
pCRC Transmit Setup Time	47	28,5	19,25	14,8
(pCRC transmit hold + setup)	*84*	*47*	*28.5*	*19.6*
Receive Assertion Period	80	40	20	10
Receive Negation Period	80	40	20	10
Transmit Assertion Period	90	45	22,5	11,5
Transmit Negation Period	90	45	22,5	11,5
Receive REQ Assertion Period with P_CRCA transitioning	180	90	45	22.5
Receive REQ Negation Period with P_CRCA transitioning	180	90	45	22.5
Transmit REQ Assertion Period with P_CRCA transitioning	190	95	47,5	24
Transmit REQ Negation Period with P_CRCA transitioning	190	95	47,5	24
(time added)	*+100*	*+50*	*+25*	*+12.5*

9.2.20 Receive assertion period

The minimum time required at an SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at an SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.xx Receive REQ assertion period with P_CRCA transitioning

Tthe minimum time required at an SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers while P_CRCA is transitioning with pCRC protection enabled. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.22 Receive negation period

The minimum time required at an SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at an SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.xx Receive REQ negation period with P_CRCA transitioning

The minimum time required at an SCSI device receiving an REQ signal for the signal to be asserted while using synchronous data transfers while P_CRCA is transitioning with pCRC protection enabled. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 44 and figure 45 for signal measurement points.

9.2.34 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

9.2.xx Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

9.2.36 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

9.2.xx Transmit REQ negation period with P_CRCA transitioning

The minimum time that a target shall negate the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.