Date: April. 12, 1999

To: T10 Committee (SCSI)

From: SPI-3 Working Group

Subject: Annex A Modification

Annex A

(normative)

Additional requirements for LVD SCSI drivers and receivers

A.1 System level requirements

The requirements for LVD drivers and receivers in this annex are based on the system level requirements stated in table A.1. Some of these requirements are specifically called out in other subclauses while others are derived from bus loading conditions and trade-offs between competing parameters.

Table A.1 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V_A (except OR-tied signals)	-1 V	-175 mV	note 1
V_N (except OR-tied signals)	175 mV	1 V	note 1
V_A (OR-tied signals)	-3,6 V	-175 mV	note 1
V_N (OR-tied signals)	100 mV	125 mV	note 1
attenuation (%)		15	note 2
loaded media impedance (ohms)	85	135	note 3
unloaded media impedance (ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (ohms)	100	110	subclause 7.3.1
device leakage (µA)	-20	20	table 16
number of devices	2	16	subclause 4.1.7
ground offset level (mV)	-355	355	note 4

Note:
1 -These limits allow 60 mV base A.C. level and a minimum of 115 mV overdrive
2 -Measured from the driver to the farthest receiver.
3 -Caused by the addition of device capacitive load (see annex F for calculations).
4 -This is the difference in voltage signal commons for devices on the bus (see figure 3).

A.2 Driver requirements

The fundamental requirement for an LVD driver is the generation of a first-step differential output voltage magnitude at the driver connections to the balanced media to achieve required minimum differential signals at every receiver connection to the bus. Other characteristics that affect overall noise margin are the common-mode output voltage, the maximum differential output voltage, the driver output impedance, and the output signal wave shape.

The driver requirements are defined in terms of the voltages and currents depicted in figure 40.

A.2.1 Differential output voltage, V_S

This subclause does not specify requirements for drivers with source impedances less then 1000 ohms.

To assure sufficient voltage to define a valid logic state at any device connection on a fully loaded LVD bus at least a minimum differential output voltage shall be generated. This value shall be large enough that, after allowance for attenuation, reflections, and differential noise coupling, V_S is at least $\pm$175 mV at the device connector to the LVD bus.

The SCSI device shall also comply with the upper limits for the differential output voltages and to the symmetry of the differential output voltage magnitudes between logic states in order to assure a first-step transition to the opposite logic state.

With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V_S, for an asserted state (V_A), shall be greater than or equal to ~~400~~ 375 mV and less than or equal to ~~780~~ 800 mV. For the negated state, the polarity of V_S shall be reversed (V_N) and the differential voltage magnitude shall be greater than or equal to ~~400~~ 375 mV and less than or equal to ~~640~~ 800 mV. The relationship between V_A and V_N specified in table A.2 and shown graphically in figure A.2 shall be maintained.

The assertion drivers and negation drivers require different strengths to achieve the near equality in V_A and V_N shown in figure A.2 because the applied V1 and V2 simulate the effects of the bus termination bias.

Figure A.2 shall only apply to drivers with source impedances greater than 1000 ohms.

Table A.2 - Driver steady-state test limits and conditions

Test parameter	Test conditions (figure A.1)	Minimum (mV)	Maximum (mV)
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted) (note)	V_1 = ~~0,957~~ 1,056 V V_2 = ~~0,535~~ 0,634 V	~~400~~ 375	~~780~~ 800
	V_1 = ~~1,949~~ 1,866 V V_2 = ~~1,527~~ 1,444 V	~~400~~ 375	~~780~~ 800
$\lvert V_N \rvert$ Differential output voltage magnitude (negated) (note)	V_1 = ~~0,957~~ 1,056 V V_2 = ~~0,535~~ 1,444 V	~~400~~ 375	~~640~~ 800
	V_1 = ~~1,949~~ 1,866 V V_2 = ~~1,527~~ 1,444 V	~~400~~ 375	~~640~~ 800
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted)	All four above conditions	0,69 x $\lvert V_N \rvert$ + 50	1,45 x $\lvert V_N \rvert$ - 65
Note: The test circuit (figure A.1) is approximately equivalent to two terminators creating the normal system bias.			

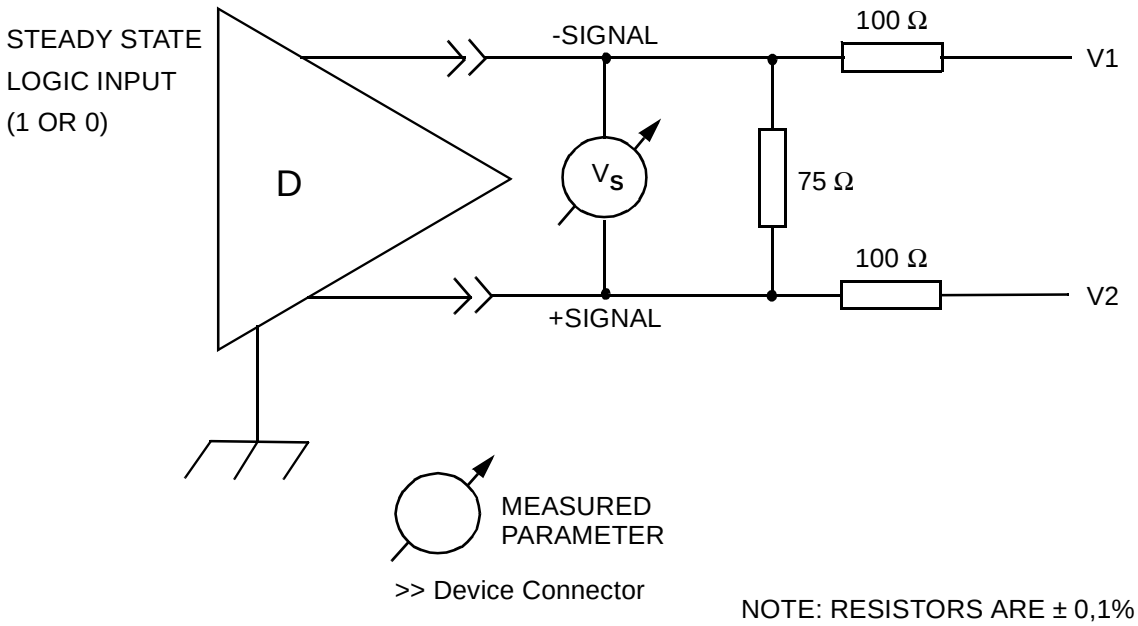


Figure A.1 - Differential steady-state output voltage test circuit

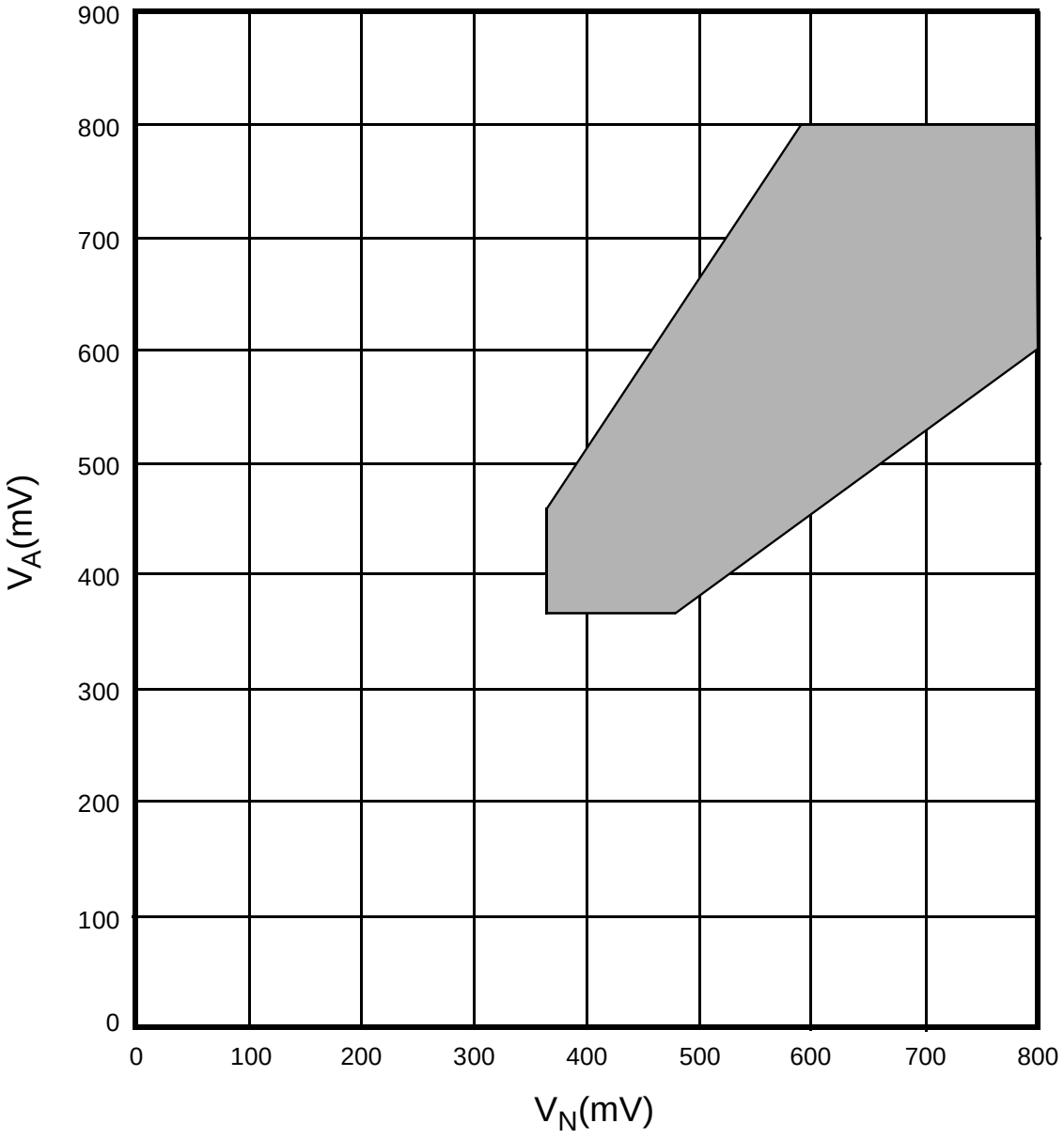


Figure A.2 - Domain for driver assertion and negation levels

A.2.2 Offset (common-mode output) voltage, V_{CM}

The steady-state magnitude of the driver offset voltage (V_{CM}), measured with the test load of figure A.3 shall be greater than or equal to ~~0,700~~ 0,845 V and less than or equal to ~~1,800~~ 1,655 V for either binary state. The steady-state magnitude of the difference of V_{CM} for one logical state and for the opposite logical state, $\Delta V_{CM,}$ shall be 120 mV or less for all $V_{applied}$ in the range: ~~0,700~~ 0,845 ≤ $V_{applied}$ ≤ ~~1,800~~ 1,655. See figure A.4.

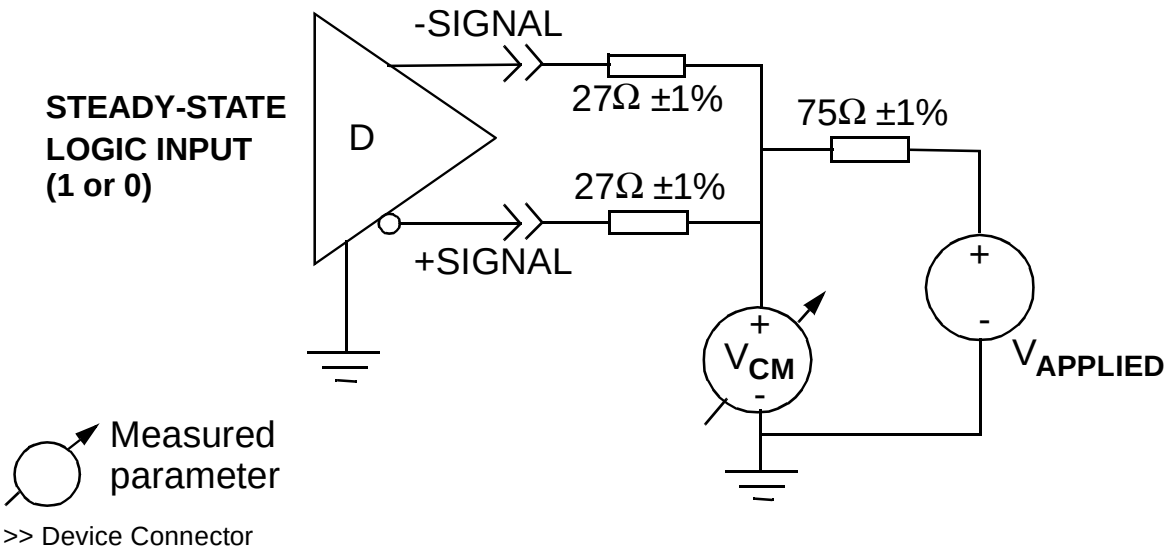


Figure A.3 - Driver offset steady-state voltage test circuit

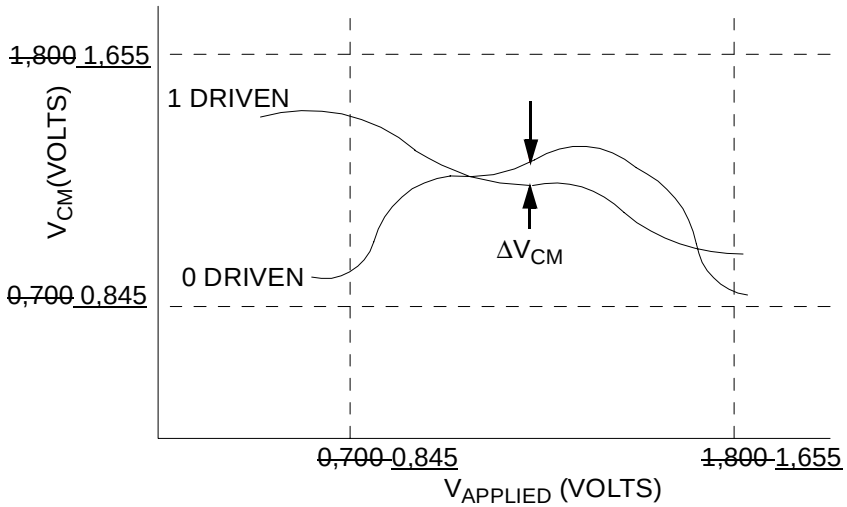


Figure A.4 - Common mode output voltage test

A.2.3 Short-circuit currents, I_{O-S} and I_{O+S}

Since an LVD bus allows multiple drivers, the possibility of contention requires a restriction on the power that may be sourced to the bus by a device. This is accomplished with a maximum allowable current from the driver.

With the driver output terminals short-circuited to a variable voltage source, the magnitudes of the currents (I_{O-S} and I_{O+S}) shall not exceed 24 mA for either logical state over the range $0 \leq V_{applied} \leq 2,5$ V. (see figure A.5).

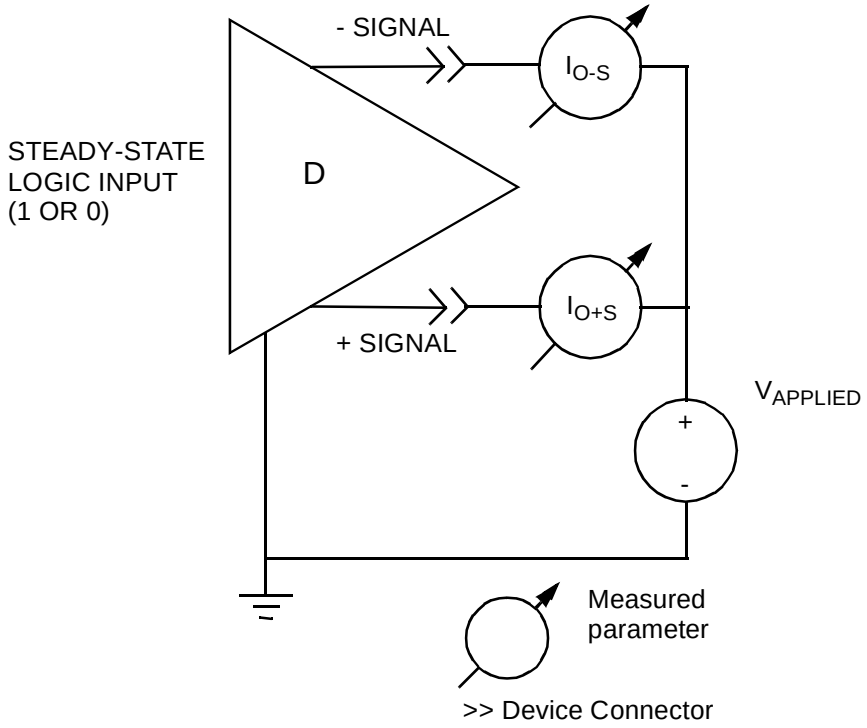


Figure A.5 - Driver short-circuit test circuit

A.2.4 Open-circuit output voltages, $V_{O-(OC)}$ and $V_{O+(OC)}$

To limit the maximum steady-state voltage at any device connector, the voltage between each output terminal of the driver circuit and its common shall be between 0 V and 3,6 V when measured in accordance with figure A.6. This requirement shall be met in all logical or high impedance states (0 V $\leq$ $V_{O-(OC)} \leq$ 3,6V and 0 V $\leq$ $V_{O+(OC)} \leq$ 3,6 V). The highest output voltage occurs with no output current.

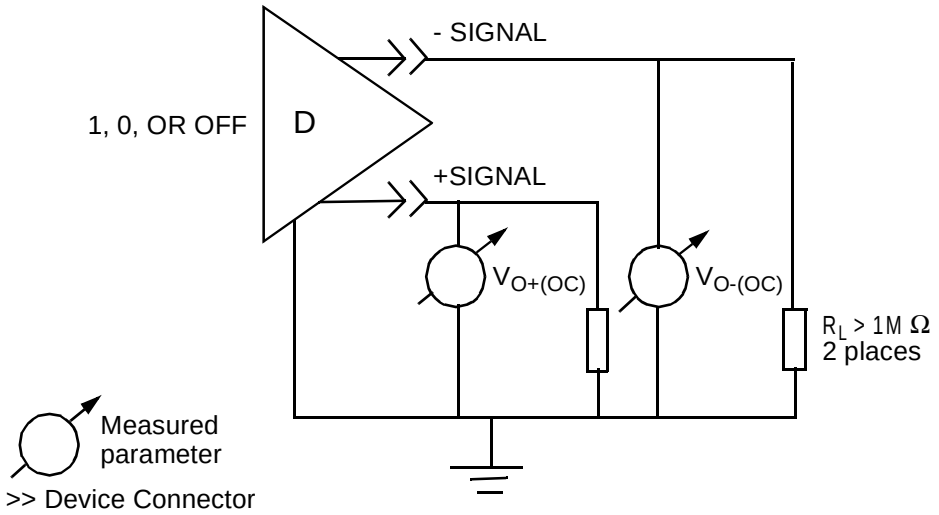


Figure A.6 - Open-circuit output voltage test circuit

A.2.5 Output signal waveform

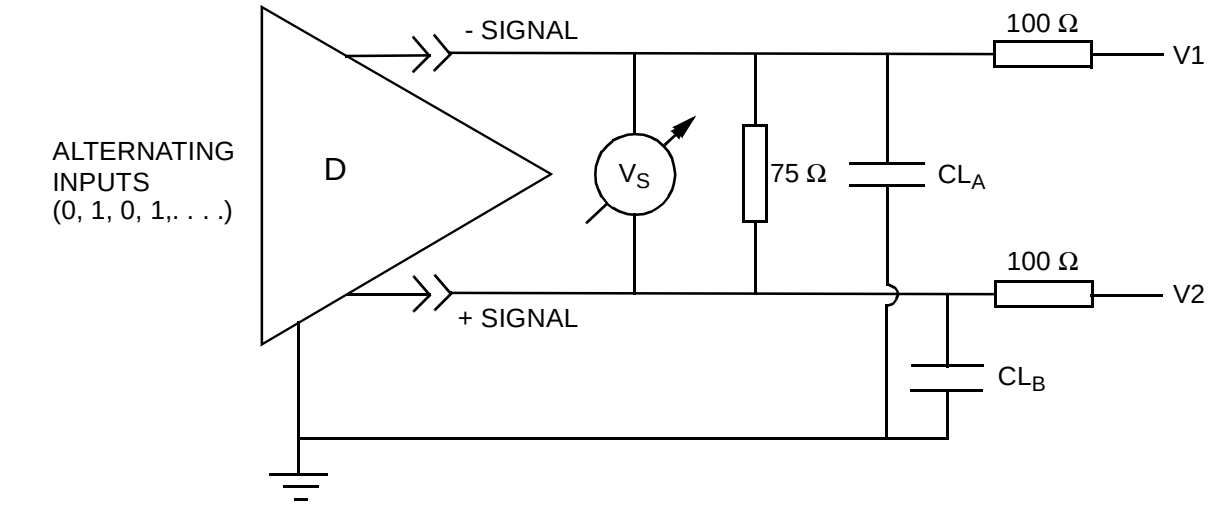
The differential output rise or fall time of a driver is specified since they influence the timing measurements and stub lengths of an LVD interface. Excessive over and under shoot of the output signal may cause electromagnetic emissions or false logic state changes.

During transitions of the driver output between alternating logical states (one - zero, zero - one, one - off, off - one, zero - off, off - zero), the differential voltage measured with the test circuit of figure A.7 and table A.3, shall be such that the voltage monotonically changes between 0,2 and 0,8 of the steady-state output, V_{SS}. V_{SS} is defined as the voltage difference between the two steady-state values of the driver output (V_{SS} = $|V_A| + |V_N|$) (See figure A.8 and table A.2). V_{SS} is expected to be different for different transitions.

The output signal rise or fall times (see t_r in figure A.8) between 0,2 and 0,8 of V_{SS} shall be greater than or equal to 1 ns.

The slew rates specified above are requirements for a driver when using the LVD test circuit in figure A.7. They are not the observed rise or fall rates on an actual SCSI bus.

Measurement equipment used for rise and fall rate testing shall provide a bandwidth of 2 GHz minimum.



Measured parameter

>> Device Connector

Notes:

a) Resistors are ±1% and surface-mount metal film type.

b) CL_A and CL_B are 5 pF ±0,2 pF and include the instrumentation capacitance.

c) The longest physical dimension between the device connector pins and any test circuit component shall be no greater than 0,1 meter.

d) V1 and V2 are applied voltages from a source having a source impedance of less than 5 Ω from 0 Hz to 40 MHz.

Figure A.7 - Differential output switching voltage test circuit

Table A.3 - Driver switching test circuit parameters

Test condition (see figure A.7)	V1	V2
Low common-mode voltage	~~1,375~~ 1,311 V	~~0,807~~ 0,889 V
High common-mode voltage	~~1,693~~ 1,611 V	~~1,125~~ 1,189 V

The signal voltage shall comply with the requirements shown in figure A.8.

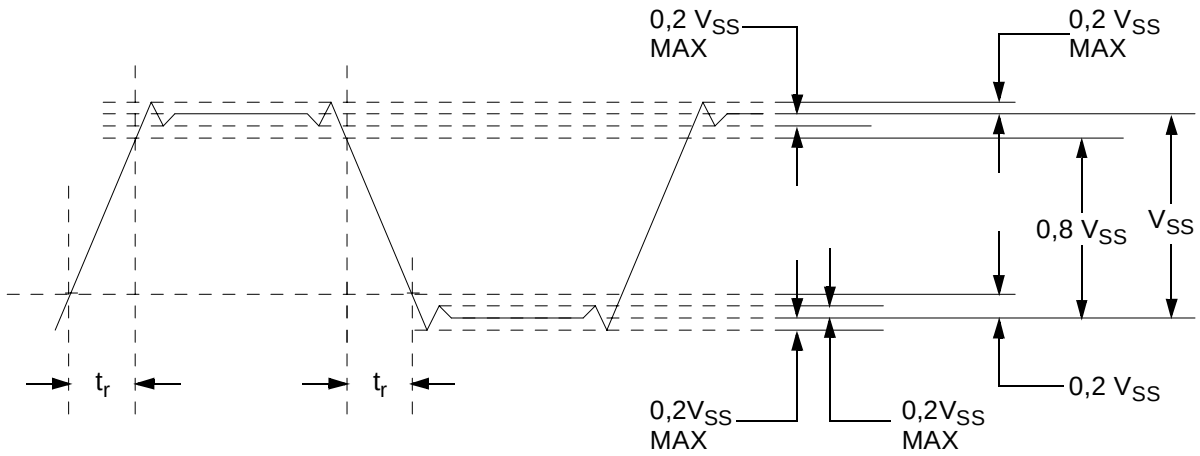


Figure A.8 - Driver output signal waveform

A.2.6 Dynamic output signal balance, $V_{CM(PP)}$

A mismatch in the magnitude of rate at which the voltage changes at the - signal and + signal connector pins, results in a common-mode AC signal. This may cause electromagnetic emissions from the media, excursions outside the receivers' common-mode input voltage range, and/or differential noise.

During transitions of the driver output between any state transition of high-to-low, low-to-high, high-to-off, off-to-high, low-to-off, or off-to-low, the voltage (V_{CM}) measured with the test circuit shown in figure A.9, shall not vary more than specified in table A.4 as $V_{applied}$ is varied over the range ~~0,700~~ 0,845 ≤ $V_{applied}$ ≤ ~~1,800~~ 1,655. Measurement equipment used for dynamic signal output balance testing shall provide a bandwidth of 400 MHz minimum. The requirements in this subclause apply only to the applicable state transitions.

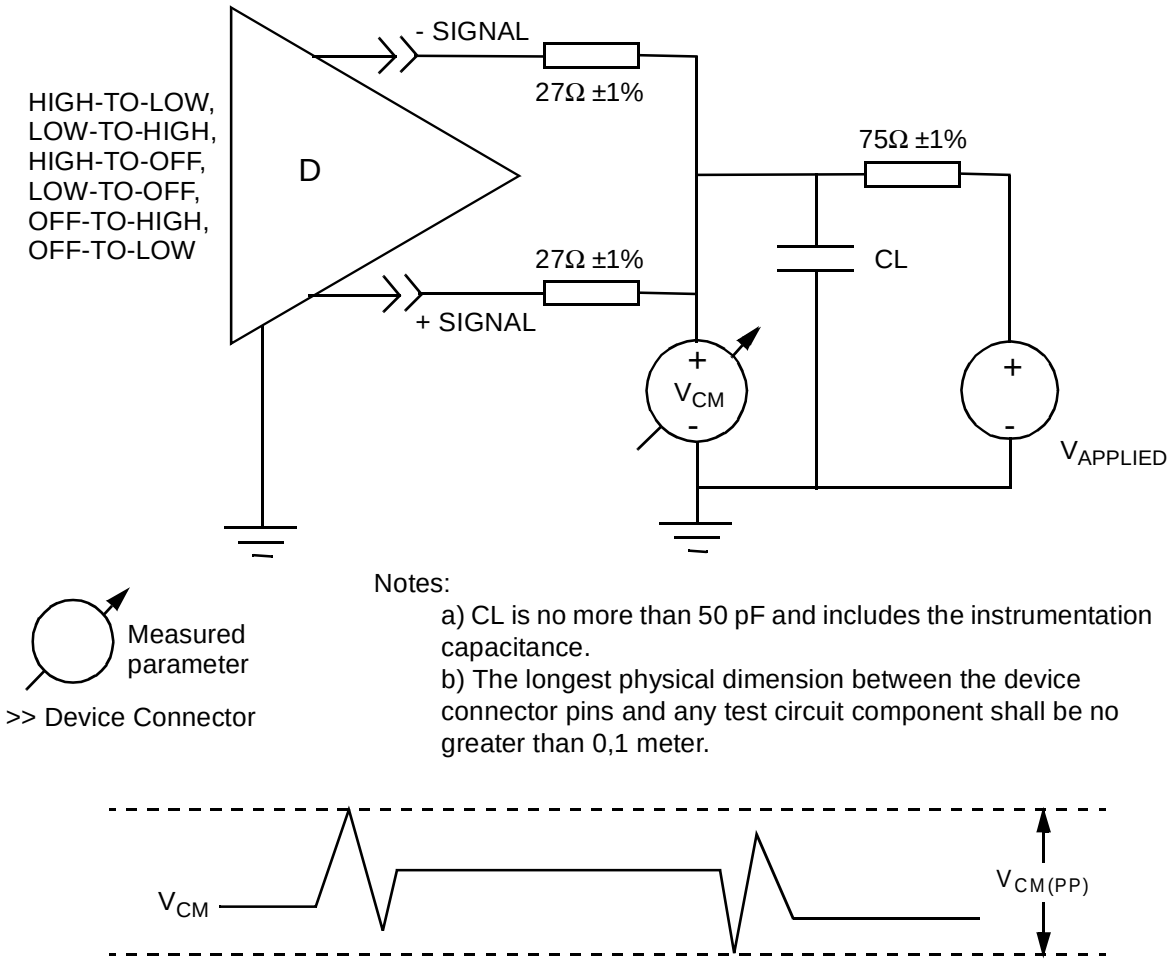


Figure A.9 - Driver offset switching voltage test circuit

Lower values of $V_{CM(PP)}$ have lower EMI risk.

Table A.4 - Dynamic output balance limits

Transition	$V_{CM(PP)}$ mV max
high-low	120
low-high	120
high-off	400
low-off	400
off-high	400
off-low	400

A.3 Receiver characteristics

A receiver indicates the logical state of the LVD bus as defined by the differential voltage that exists at the device connector. A minimum steady state differential voltage defines the logic state. The receiver shall detect this difference over the allowable common-mode input voltage range as determined by the driver and terminator output offsets and ground difference voltages.

Table A.5 defines the voltages and currents for the requirements in this subclause.

A.3.1 Receiver steady state input voltage requirements

Within the common-mode input voltage range (V_{CM}), (figure 41) ~~0,700~~ 0,845 V ≤ V_{CM} ≤ ~~1,800~~ 1,655 V an LVD receiver shall indicate the logical states shown in table A.5 with V_{IN} within the ranges shown in table A.5.

Table A.5 - Receiver steady state input voltage ranges

Input voltage range steady state (V_{IN})	Receiver detects
-3,6 V ≤ V_{IN} ≤ -0,030 V	1
0,030 V ≤ V_{IN} ≤ 3,6V	0

SCSI devices should incorporate a glitch filter function on REQ and ACK signals to reduce or eliminate the effect of glitch pulses.

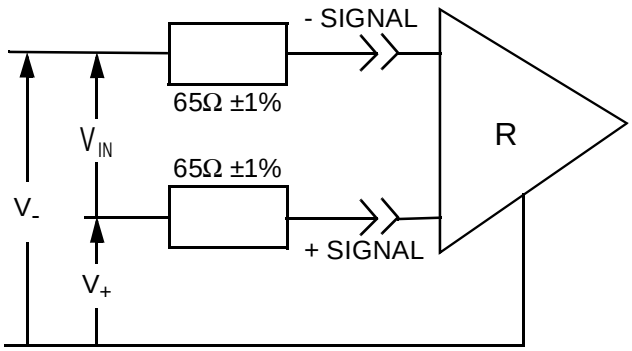
If implemented, the glitch filter period shall not be so long as to mask out the subsequent valid transition edges of the incoming REQ and ACK signals.

A.3.2 Compliance test

Compliance to the requirements in A.3.1 shall be verified with the input voltages of table A.6 and the circuit of figure A.10.

Table A.6 - Receiver minimum and maximum input voltages.

Applied voltages (input voltage referenced to circuit common) (see figure A.10)		Resulting differential input voltage	Resulting common-voltage input voltage
V_-	V_+	V_{IN}	V_{CM}
~~0,715~~ 0,860	~~0,685~~ 0,830	0,030	~~0,700~~ 0,845
~~0,685~~ 0,830	~~0.715~~ 0,860	-0.030	~~0,700~~ 0,845
~~1,815~~ 1,670	~~1,785~~ 1,640	0,030	~~1,800~~ 1,655
~~1,785~~ 1,640	~~1,815~~ 1,670	-0.030	~~1,800~~ 1,655
~~3,600~~ 3,310	0,000	~~3,600~~ 3,310	~~1,800~~ 1,655
0,000	~~3,600~~ 3,310	~~-3,600~~ -3,310	~~1,800~~ 1,655
~~3,955~~ 3,665	~~-0,355~~ 0,355 ?	~~4,310~~ 4,020	~~1,800~~ 1,655
~~-0,355~~ 0,355 ?	~~3,955~~ 3,665	~~-4,310~~ -4,020	~~1,800~~ 1,655



>> Device Connector

Figure A.10 - Receiver input voltage threshold test circuit

A.3.3 Receiver setup and hold times

Figure 44 and figure 48 define the receiver setup and hold times.

NOTE 1 - Dynamic testing is required to verify these timings.

A.4 Transceiver characteristics

A.4.1 Transceiver output/input currents, I_{I-L} and I_{I+L}

The requirements in this clause apply as a test method to ensure compliance with table 15 and table 16. With the transceiver in an off condition (i.e., not transmitting) and the + and - signals connected to a variable voltage source, $V_{applied}$, the output leakage currents I_{I-L} and I_{I+L} shall not exceed the applicable values in table 16 over the range 0,00 V ≤ $V_{applied}$ ≤ 3,6 V (see figure A.11). The maximum applicable current from table 16 is I_{max}.

These measurements apply with the transceiver's power supply in both power-on and power-off conditions.

$| I_{I-L} | < I_{max}$

$| I_{I+L} | < I_{max}$

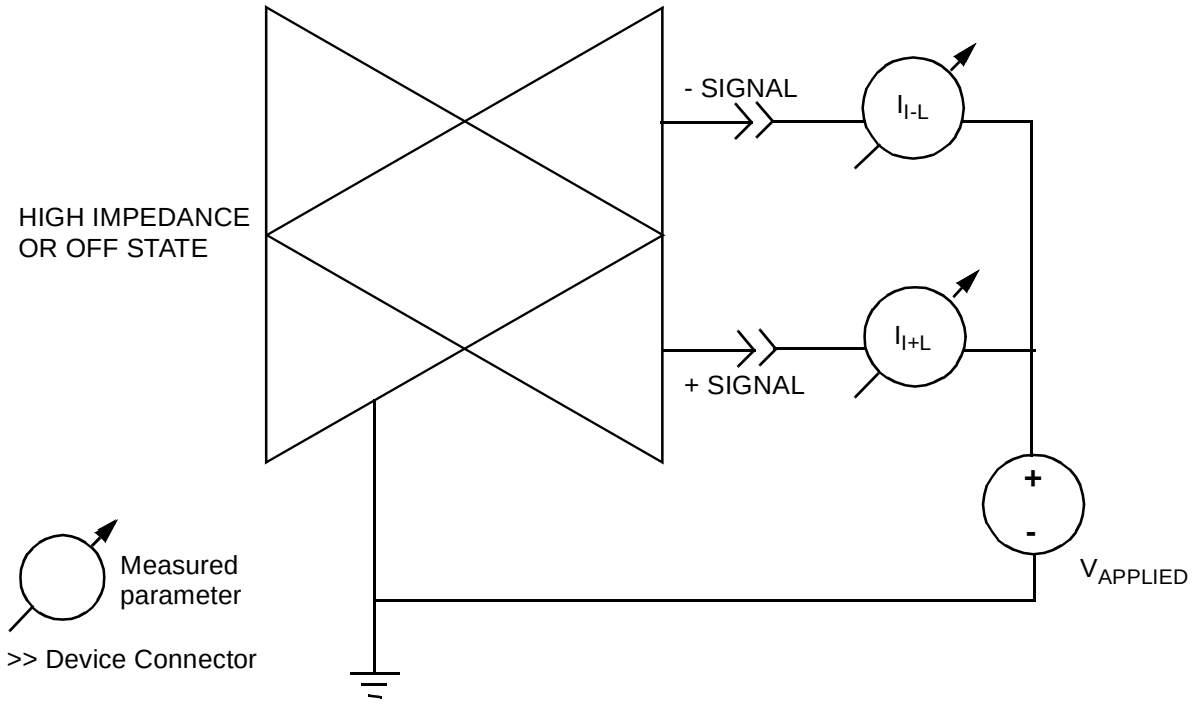


Figure A.11 - Transceiver off-state output current test circuit

A.4.2 Transceiver maximum input voltages

See table 15 and table 16.