Justification for Asynchronous Information Phase Protection

• LVD is still new
  – Widespread deployment of hot-plug capable LVD systems and drives is only now beginning
  – Hot plug events do cause problems
    • glitches on “plus pins” not visible on SE systems
• Industry is moving towards better data protection in entire system
  – Serial busses protect every bit with CRC; processor busses have ECC
  – Covering each bus individually is not as good as end-to-end CRC, but better than just having “odd number of errors” detection on some busses
• Packetized protects command and status phases, but is still in infancy
  – More complex implementation, may require host software changes
  – Details still being worked on (e.g. length field, redundant CRC)
  – Host adapters and drives not ready until well after the “Ultra 160/m” generation
  – Not yet proven in hardware
• The Quantum/LSI Logic proposal is easier
  – Simple and optional; doesn’t require redesign of existing logic
  – Completely handled by hardware; software just sees “parity errors”
• Compaq wants this for 2nd generation of Ultra 160/m low profile drives in year 2000
  – Packetized is probably not ready in this time frame