

LVD Timing Diagram Correction

SPI-3R7 Figure 44 & 45 correction

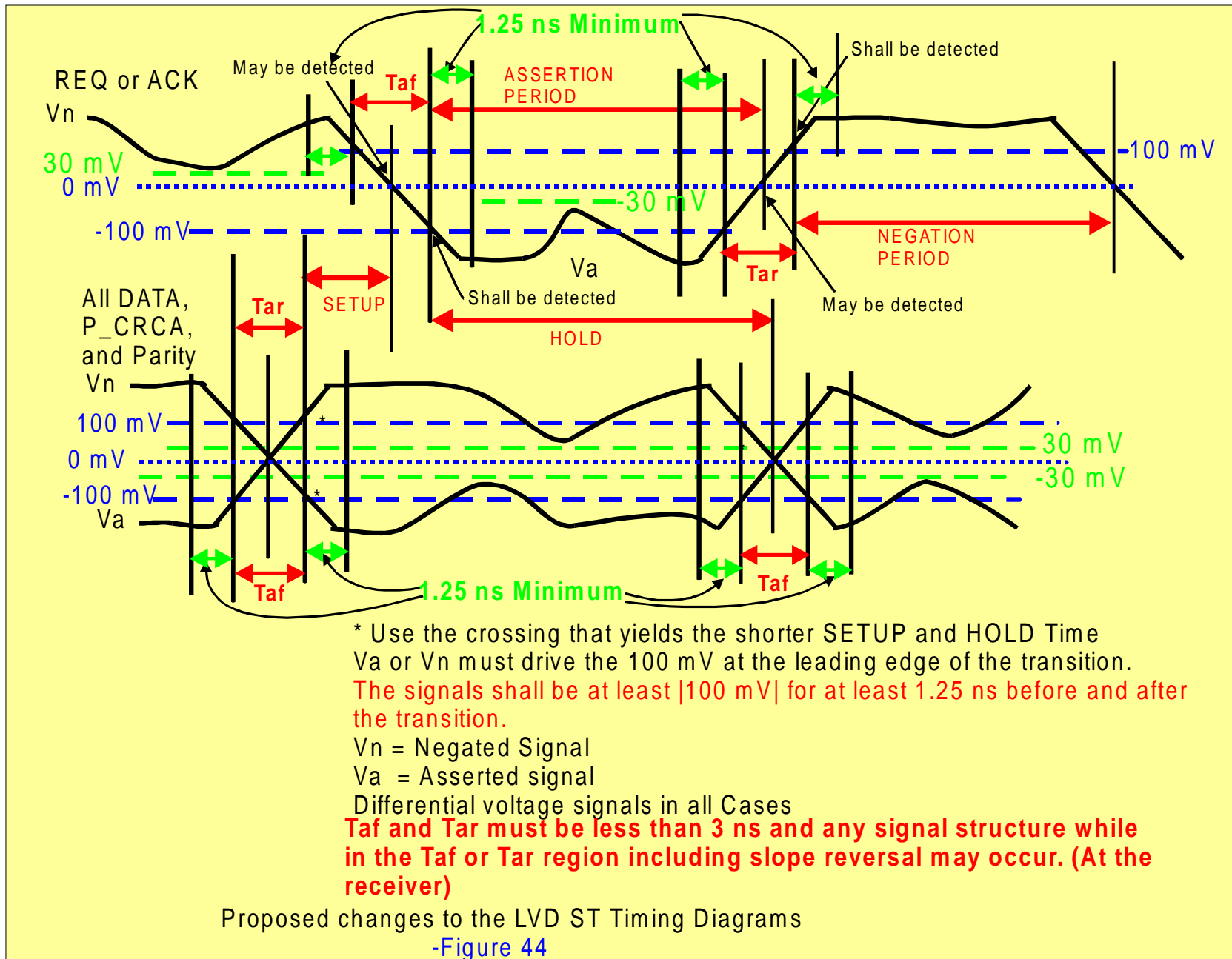
Text Correction

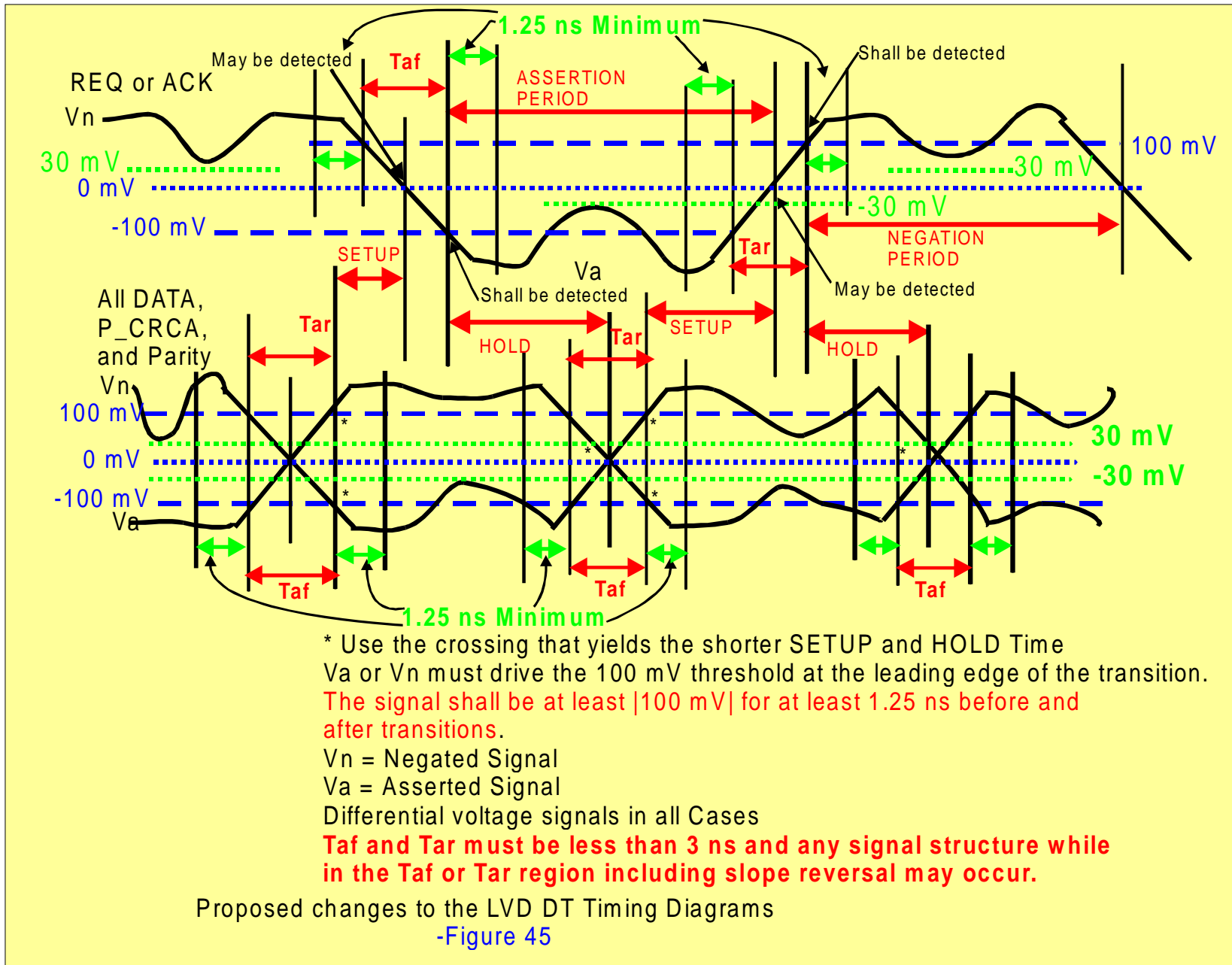
Driver Level Issues

Receiver Requirement

- The receivers require at least 100 mV to switch fast enough to meet the skew requirements. These signals are measured at the receiving device connector.
- The Receiver requires a maximum of 3 ns rise / fall time from -100 to 100 mV Rise, 100 to -100 mV Fall - the waveform in this region -100 and 100 mV is not defined.
- Notes for Engineers; Receivers simulations should use very fast rise times. Rise times of 0 to 3 ns with the 0 ns any point during the 3 ns switching time. Amplitudes from +/- 100 MV to +/- 800 mV should be simulated with the range of rise times maintaining the 4 to 1 maximum amplitude. All line will see different wave forms, worst should be simulated against best over Process, Temperature and voltage to insure the receivers will meet the skew requirements.

Note: Blue is delete, red is add



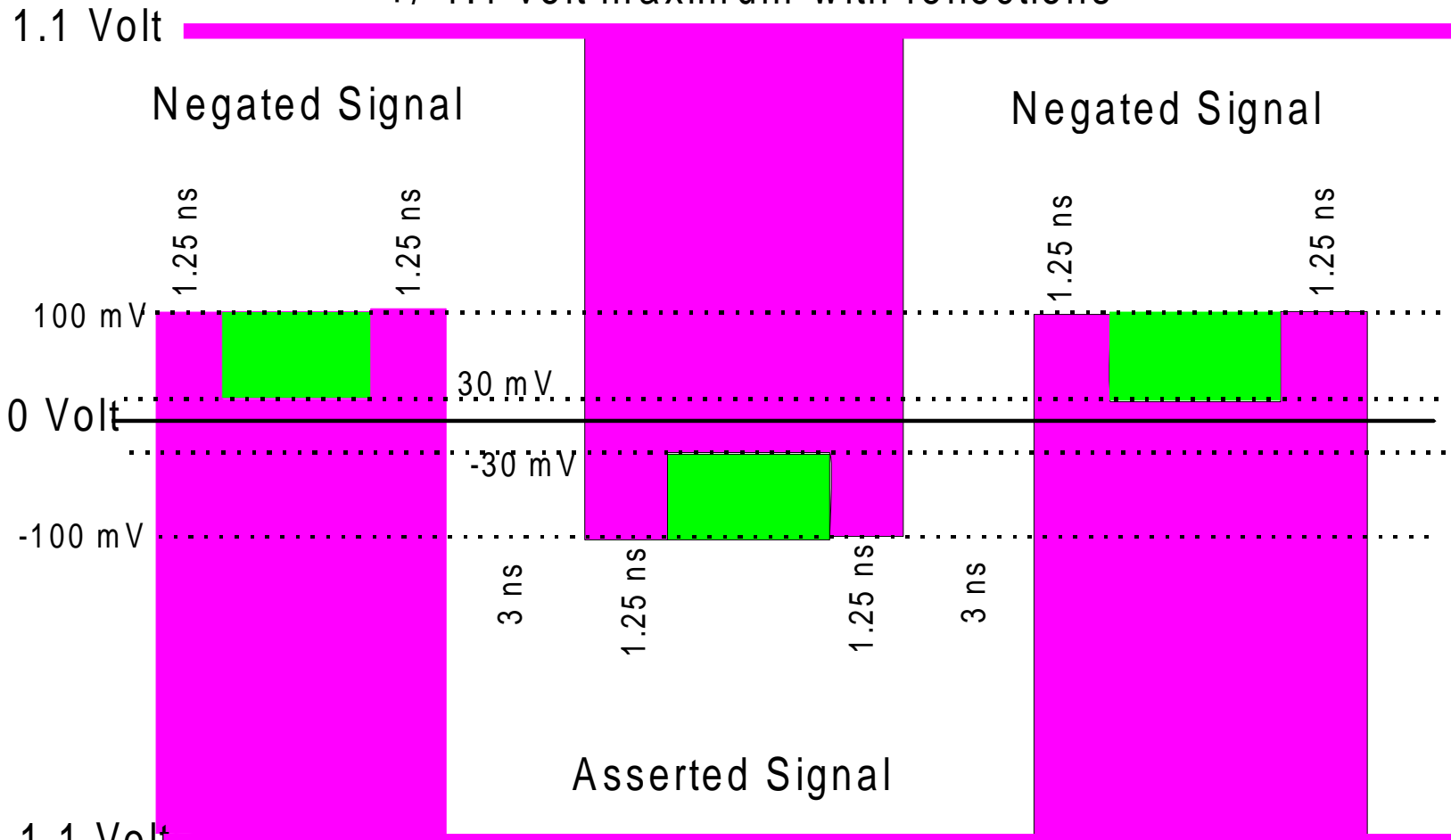


- 9.3.3 LVD Transfer Rates second paragraph Text Correction
- Figure 44 and figure 45 illustrates the signal must transition from -100 to 100 mV or 100 to - 100 mV in 3 ns, the waveform between -100 and 100 mV is not otherwise specified. Signals shall remain above the |100 mV| level for 1.25 ns at each end of the transition. The signals shall not drop below |30 mV| except during the transitions. Conditions exist with longer loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 and 45 are used in the measurement of timing parameters.

Receiver Mask

- Add a receiver mask for the allowable signal at the Receiving device connector.
 - Edges of transitions are require at least $|100 \text{ mV}|$ for 1.25 ns.
 - Signals are allowed to have noise inside the assertion or negation signal that drop back to $|30 \text{ mV}|$.

Receiver Mask, during the data transitions
 +/-1.1 volt maximum with reflections



The ratio of the Peak before the transition to the Peak after the transition in the 1.25 ns range shall not exceed 4 to 1.

Not Allowed

Tolerated

Not Recommended

System Loss, Driver Requirements

- **Crosstalk should be considered 60 mV or 160 mV receiver level should be used to calculate the drive level required.**
- The previous system requirement was 115 mV
 - 100 mV AC threshold plus 60 mV for crosstalk
 - System requirements of 160 mV
 - The system test show a 50% reduction in signal level on a loaded bus. (A.2.1 2nd Paragraph lists what is included in the 50%)
 - Minimum drive level of 320 mV is required.

Table A.1 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V _A (except OR-tied signals)	-1 V	-100 mV -175 mV	note 1
V _N (except OR-tied signals)	100 mV 175 mV	1 V	note 1
V _A (OR-tied signals)	-3,6 V	-100 mV -175 mV	note 1
V _N (OR-tied signals)	100 mV	125 mV	note 1
attenuation (%)		15	note 2
loaded media impedance (ohms)	85	135	note 3
unloaded media impedance (ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (ohms)	100	110	subclause 7.3.1
device leakage (μA)	-20	20	table 16
number of devices	2	16	subclause 4.1.7
ground offset level (mV)	-355	355	note 4
<p>Note:</p> <p>1 - These limits allow 60 mV base A.C. level and a minimum of 115 mV overdrive</p> <p>2 - Measured from the driver to the farthest receiver.</p> <p>3 - Caused by the addition of device capacitive load (see annex F for calculations).</p> <p>4 - This is the difference in voltage signal commons for devices on the bus (see figure 3).</p>			

Note 1 - These are the signals at the receiver, system allowance for 60 mV crosstalk is used for the driver power.

Annex A Continued

- A.2.1 second paragraph second sentence
 - This value shall be large enough that, after allowance for attenuation (AC & DC), reflections, Terminator bias difference and differential noise coupling, V S is at least +60 +100 mV at the device connector to the LVD SCSI bus.

A.2.1 Paragraph 4

- With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V_S , for an asserted state (V A), shall be greater than or equal to 320 375 mV and less than or equal to 800 mV. For the negated state, the polarity of V_S shall be reversed (V N) and the differential voltage magnitude shall be greater than or equal to 320 375 mV and less than or equal to 800 mV. The relationship between V A and V N specified in table A.2 and shown graphically in figure A.2 shall be maintained.

Annex A Continued

- Table A.2
 - Change all the minimums to 320 mV
- Figure A.2
 - Move the lower part of the shaded area to 320 mV on both axis.

