LVD Timing Diagram Correction

Thoughts for late May SPI-3 meeting

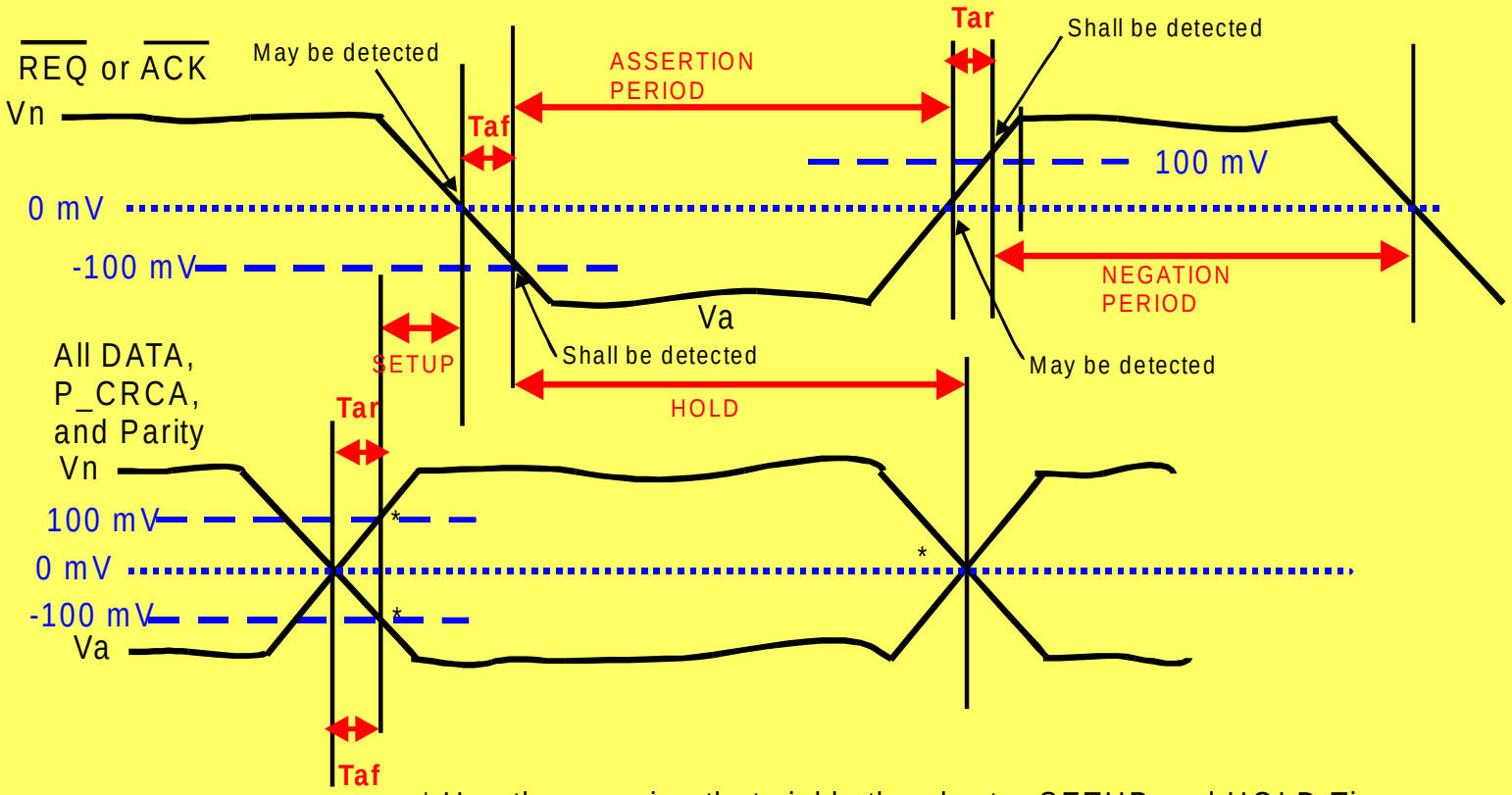
SPI-3R5 Figure 44 & 45 correction

Text Correction

Driver Level Issues

Receiver Requirement

- The receivers require 100 mV to switch fast enough to not have skew problems. This is at the receiving device connector.
- 2 ns Receiver rise - fall time requirements specified

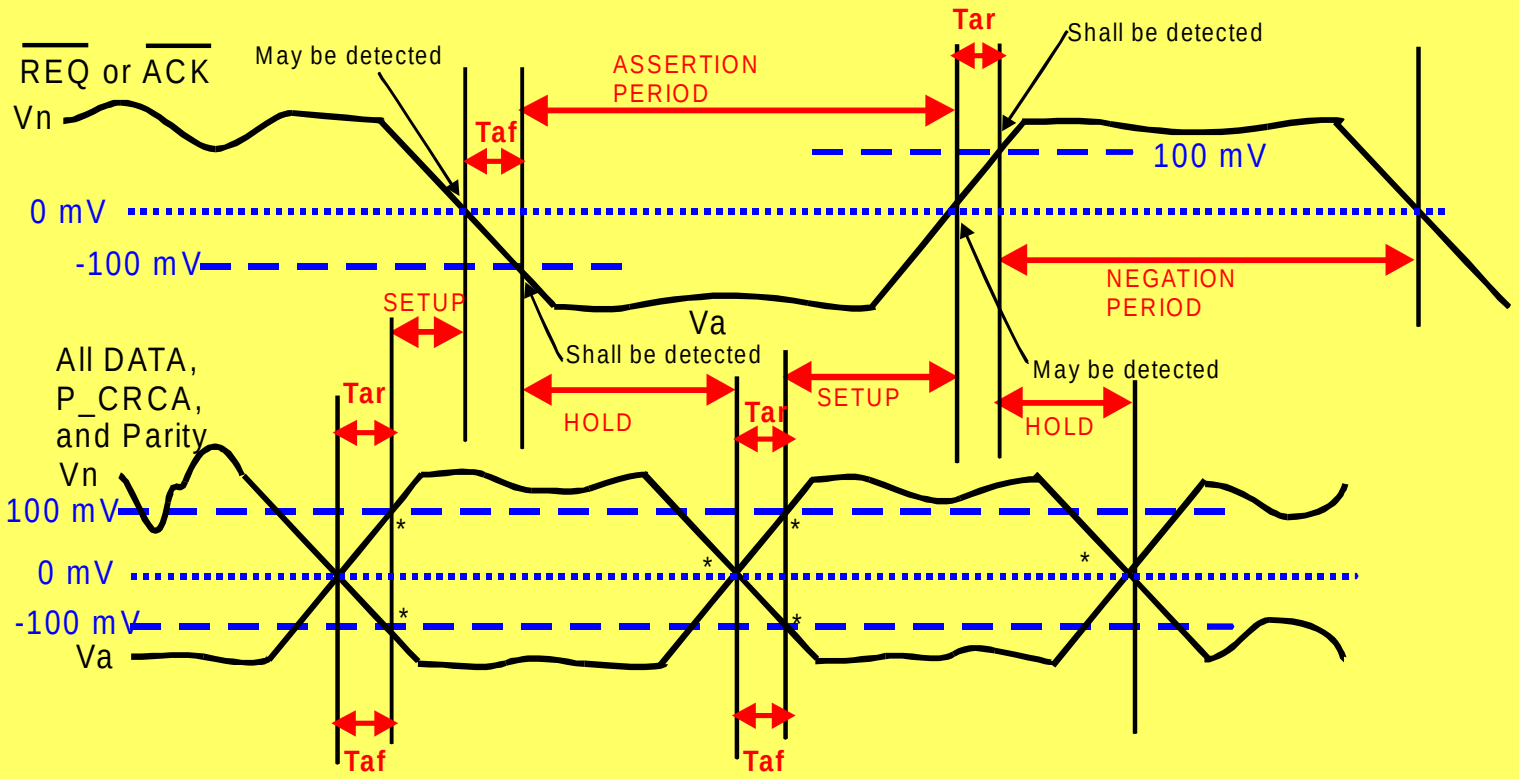


* Use the crossing that yields the shorter SETUP and HOLD Time
Va or Vn must drive the 100 mV at the leading edge of the transition.
Vn = Negated Signal
Va = Asserted signal
Differential voltage signals in all Cases

Taf and Tar must be less than 2 ns and any signal structure while in the Taf or Tar region including slope reversal may occur. (At the receiver)

Proposed changes to the LVD ST Timing Diagrams

-Figure 44



* Use the crossing that yields the shorter SETUP and HOLD Time
Va or Vn must drive the 100 mV threshold at the leading edge of the transition.
Vn = Negated Signal
Va = Asserted Signal
Differential voltage signals in all Cases

Taf and Tar must be less than 2 ns and any signal structure while in the Taf or Tar region including slope reversal may occur.

Proposed changes to the LVD DT Timing Diagrams

-Figure 45

Text Correction

- 9.3.3 LVD Transfer Rates second paragraph
- Figure 44 and figure 45 illustrate that receivers may require a larger LVD signal to overcome a strongly asserted or negated state than required for a weakly asserted or negated state. Receivers require at least 115 mV over the 60 mV A.C. threshold or 175 mV to guarantee detection with the proper receiver switching time. The same relationship applies for the maximum negated level V N . Conditions exist with longer loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 are used in the measurement of timing parameters.
- Change to: Figure 44 and 45 illustrate that receivers require at least 100 mV AC threshold to guarantee detection with the proper receiver switching time. Rise and fall times from 0 to +/- 100 mV must be faster than 2 ns. Conditions exist with longer loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 are used in the measurement of timing parameters.
- Crosstalk should be consider, 55 mV or 155 mV should be used to calculate the drive level required.

System Loss, Driver Requirements

- The previous system requirement was 115 mV
  - 100 mV AC threshold plus 55 mV for crosstalk
  - System requirements of 155 mV
  - The system test show a 50% reduction in signal level on a loaded bus.
  - Minimum drive level of 310 mV is required, the current level is 270 mV.

Annex A Changes

- Table A.1
  - Va Max Min -1V, -155 mV
  - Vn Min 155 mV, Max 1V
  - Remove the third line of the table
  - Note 1 -These limits allow 100 mV base A.C. level and a maximum 55 mV for crosstalk and other non-common mode noise. Changes to: These limits allow 100 mV base A,C, level and a minimum of 155 mV overdrive.

Annex A Continued

- A.2.1 second paragraph second sentence
  - This value shall be large enough that, after allowance for attenuation, reflections, and differential noise coupling, V S is at least +60 +100 mV at the device connector to the LVD bus.

A.2.1 Paragraph 4

- With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V S , for an asserted state (V A), shall be greater than or equal to 400 310 mV and less than or equal to 800 mV. For the negated state, the polarity of V S shall be reversed (V N) and the differential voltage magnitude shall be greater than or equal to 400 310 mV and less than or equal to 800 mV. The relationship between V A and V N specified in table A.2 and shown graphically in figure A.2 shall be maintained.

Annex A Continued

- Table A.2
  - Change all the minimums to 310 mV
- Figure A.2
  - Move the lower part of the shaded area to 310 mV on both axis.