

LVD Timing Diagram Correction

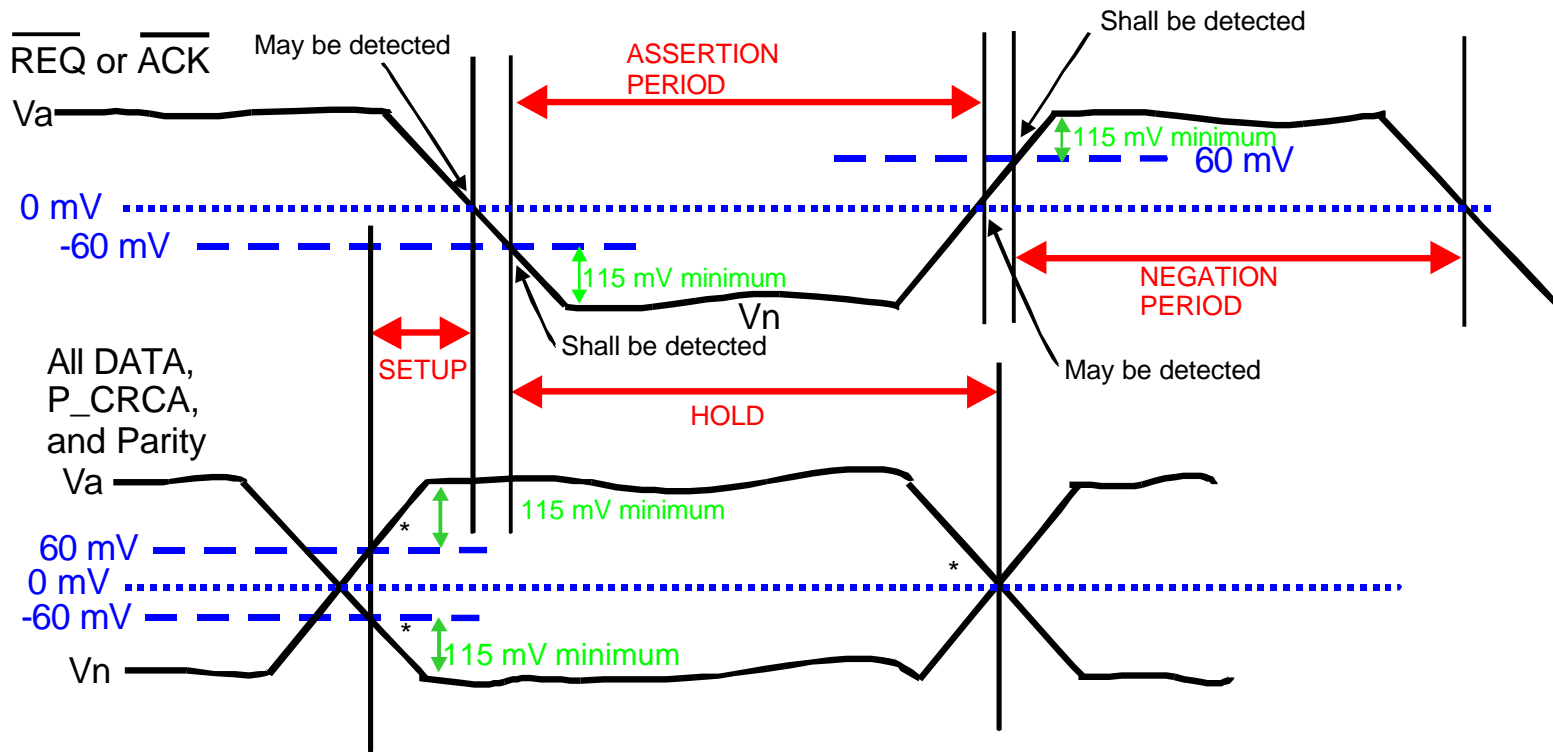
SPI-3R2 Figure 44 & 45 correction

Text Correction

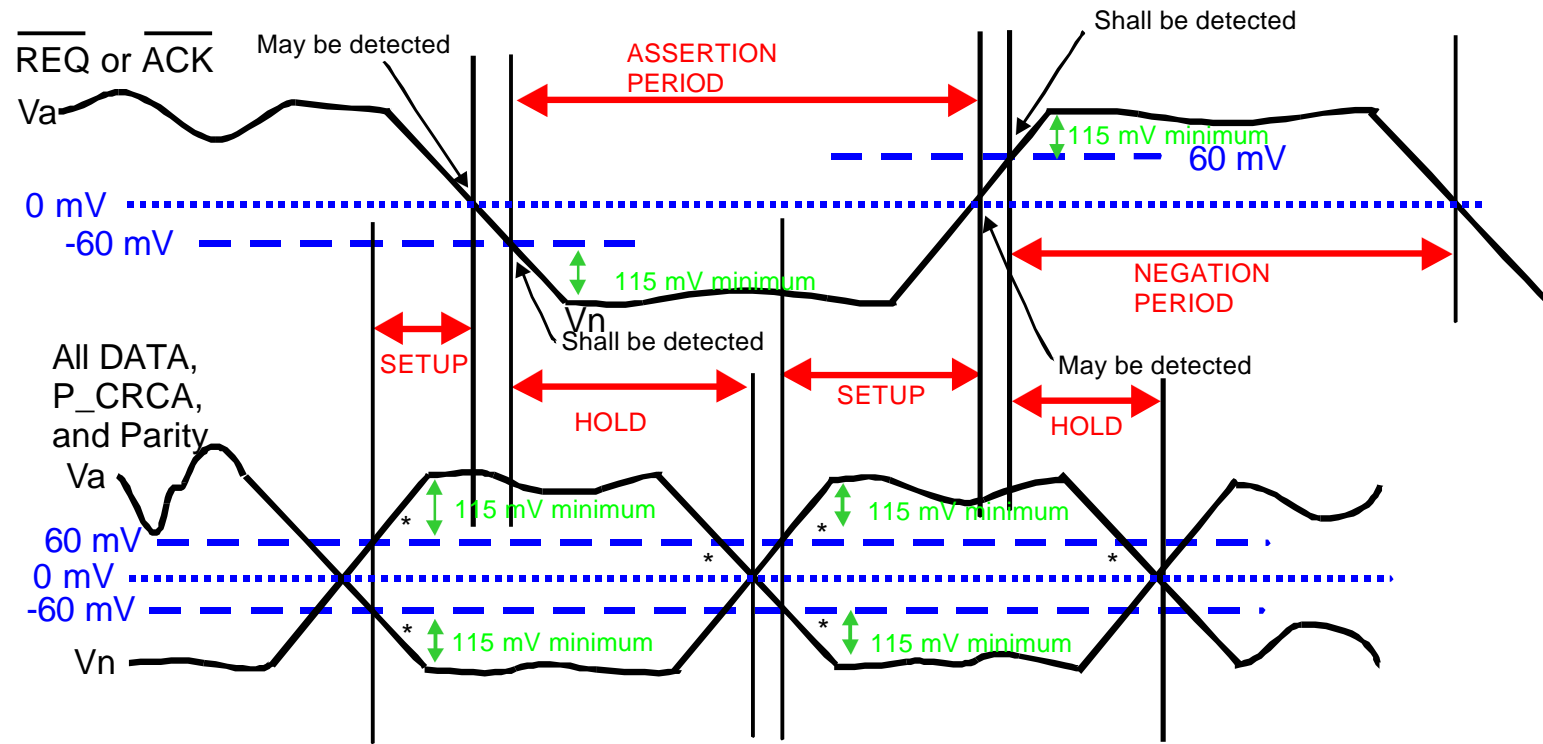
Driver Level Issues

Receiver Requirement

- The receivers require over drive to switch fast enough to not have skew problems.
- The receiver overdrive is not a function of the previous voltage, but a fixed 115 mV over the 60 mV AC threshold.
- AC measurement may switch is not 60 mV, it is 0 mV.



* Use the crossing that yields the shorter SETUP and HOLD Time
 V_a or V_n must over drive the 60 mV threshold by 115 mV at the leading edge of the transition.
 V_n = Negated Signal
 V_a = Asserted signal
 Differential voltage signals in all Cases



* Use the crossing that yields the shorter SETUP and HOLD Time
 Va or Vn must over drive the 60 mV threshold by 115 mV at the leading edge of the transition.
 Vn = Negated Signal
 Va = Asserted Signal
 Differential voltage signals in all Cases

Text Correction

- 9.2.3 ST Timing & 9.2.4 DT Timing second paragraph second sentence
 - With the maximum assertion level of V_A it requires a signal that crosses the zero differential level by at least $0,25 \times V_A$ (but at least by 60 mV in all cases) to guarantee detection of a negation for fast signals.
 - Change to: Receivers require at least 115 mV over the 60 mV AC threshold or 175 mV to guarantee detection with the proper receiver switching time.

System Loss, Driver Requirements

- The previous system requirement was 115 mV
 - 60 mV AC threshold plus 55 mV for crosstalk
 - Receiver requirements of 175 mV
 - The system test show a 50% reduction in signal level on a loaded bus.
 - Minimum drive level of 350 mV is required, the current level is 270 mV.

Annex A Changes

- Table A.1
 - V_a Max Min -1V, -175 mV
 - V_n Min 175 mV, Max 1V
 - Remove the third line of the table
 - Note 1 -These limits allow 60 mV base A.C. level and a maximum 55 mV for crosstalk and other non-common mode noise.
Changes to: These limits allow 60 mV base A,C, level and a minimum of 115 mV

Annex A Continued

- A.2.1 second paragraph second sentence
 - This value shall be large enough that, after allowance for attenuation, reflections, and differential noise coupling, V_S is at least **+60 +175** mV at the device connector to the LVD bus.

A.2.1 Paragraph 4

- With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V_S , for an asserted state (V A), shall be greater than or equal to 270 350 mV and less than or equal to 780 mV. For the negated state, the polarity of V_S shall be reversed (V N) and the differential voltage magnitude shall be greater than or equal to 260 350 mV and less than or equal to 640 mV. The relationship between V A and V N specified in table A.2 and shown graphically in figure A.2 shall be maintained.
- Concern about too big of an increase, 80 mV versus 115 mV added to the receiver level. 385 mV should be the minimum if all the other requirements are part of the calculation.

Annex A Continued

- Table A.2
 - Change all the minimums to 350 mV
- Figure A.2
 - Move the lower part of the shaded area to 350 mV on both axis.