LSI LOGIC

SPI-3 LVD Setup/Hold Time Issues

Frank Gasparik, January 25, 1998

Signal Dips / Glitches

The SPI-3 document defines the LVD timing as shown in Figure 45. For both REQB and ACKB signals the “May be detected” values are 60mV before the differential zero crossing. This values are used incorrectly as the threshold for the LVD Receiver. Some LVD system users are assuming that if the signal dip (glitch) gets to this value (or to the differential zero crossing) it will result in a system integrity problem. None of the customers’ or our tests could show the LVD system failures due such dips as shown below.

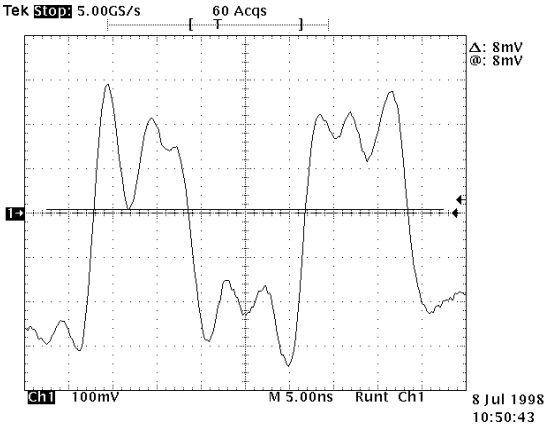
The following pages show the simulation results for glitch width from 1ns to 3ns. The glitch depth starts with +60mV above the differential zero crossing signal level (reference voltage 1.25V) and progressively deepens by 30mV. I will cross the differential zero crossing level and continue with the overdrive increase until it will cause the receiver to detect the glitch.

Figure 1 shows the results for the glitch 1ns wide. The receiver has to be overdriven by an amount of -180mV to propagate the signal to the output.

For the glitch width equal to 2ns the overdrive must be -120mV to propagate to the output as illustrated in Figure 2.

Similarly, Figure 3 shows the case with glitch width 3ns. The amount of the overdrive is equal to -60mV for glitch to be detected.

This data is presented at the January 26, 1999 SPI-3 meeting in order to modify the SPI-3 Figure 45 and similar figure in SPI-2 document.



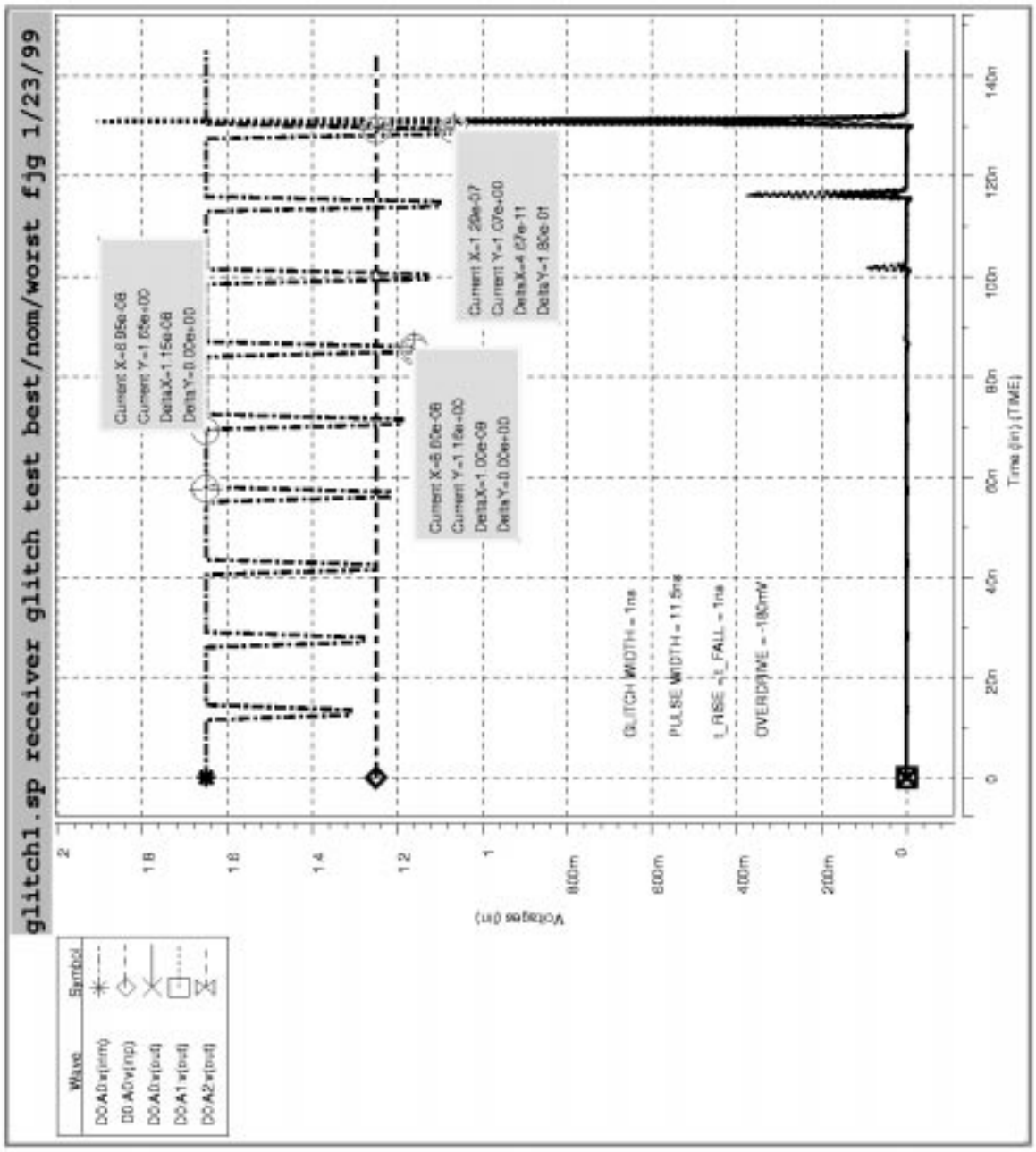


Figure 1 Glitch Width 1ns

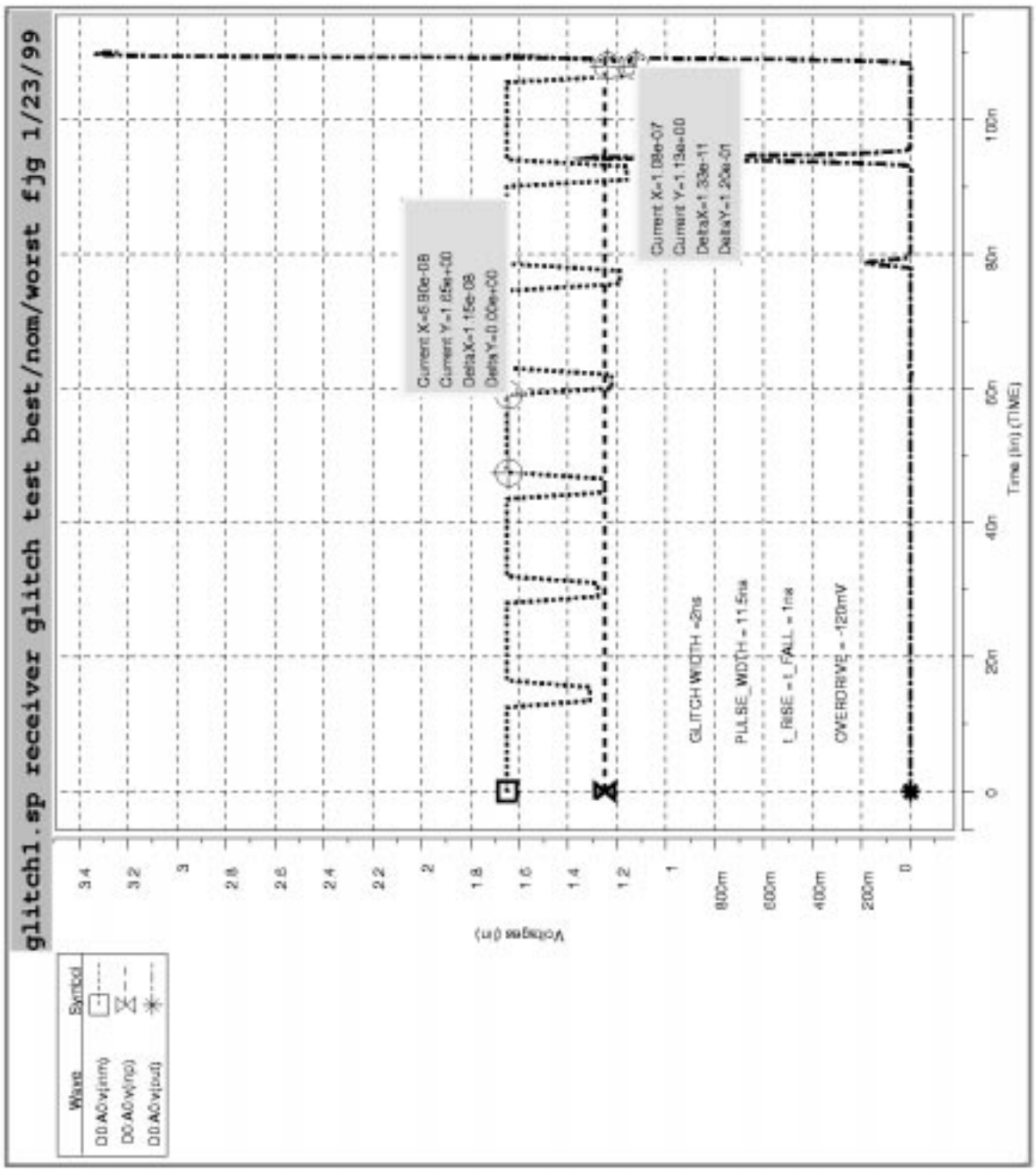


Figure 2 Glitch Width 2ns

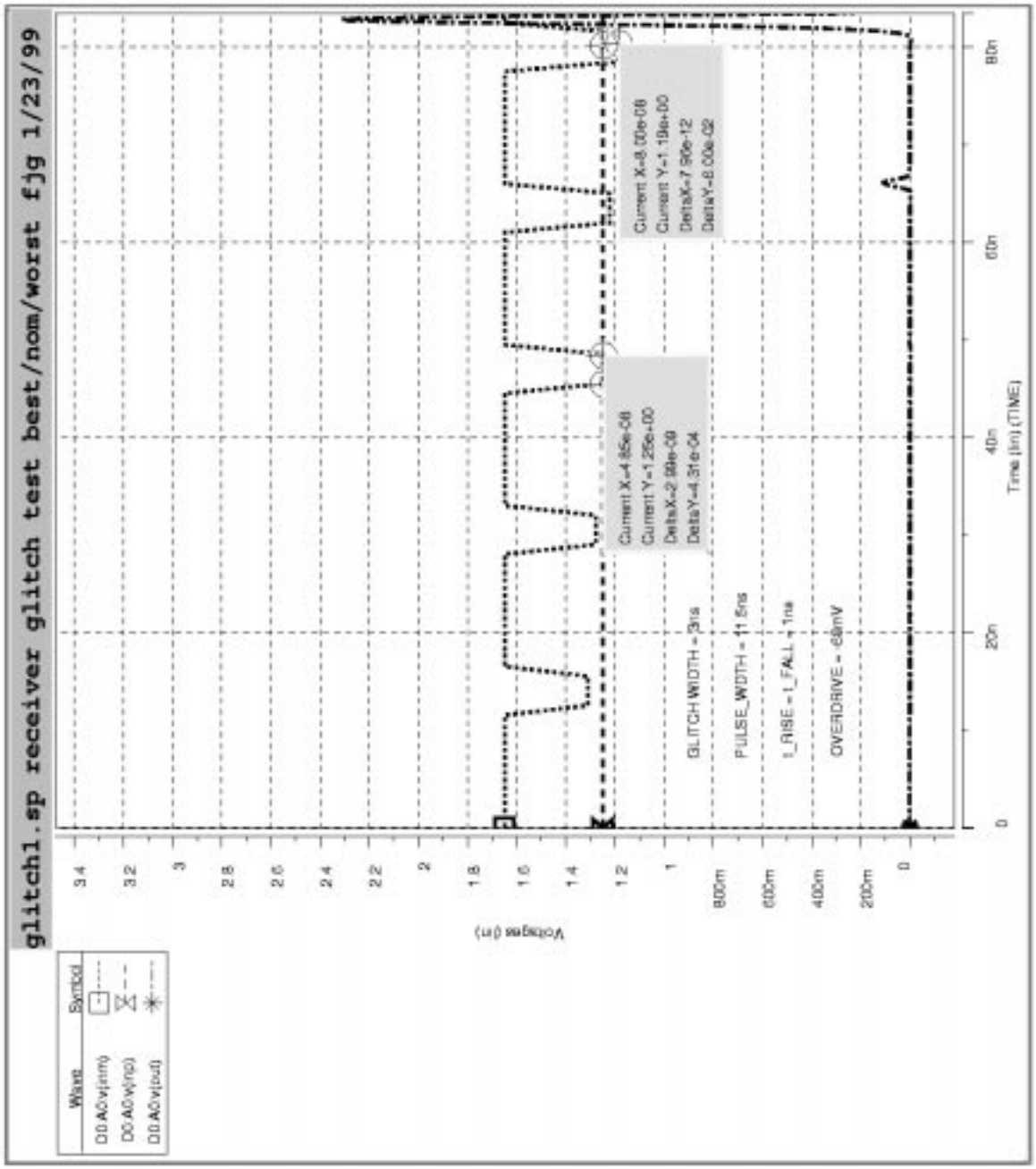


Figure 3 Glitch Width 3ns