Protection for the Asynchronous Information Phases (Command, Message, and Status)

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1 Introduction

With the advent of CRC on the DT data phases, customers have requested similar types of protection on non-data information phases (COMMAND, MESSAGE, and STATUS) in those cases where the information may become corrupted (e.g., by hot plugging events). These requests include having protection coverage on the phase lines (MSG, C/D, and I/O) as well. The constraint for the solution to this issue is that it should be a simple, modular addition to the existing SCSI protocol (i.e., these customers desire this capability in a non-Packetized SCSI protocol). The solution in this proposal resolves this issue.

2 Overview

In the current DT protocol with CRC, the SCSI bus is restricted to 16-bit (wide) data phases only. COMMAND, MESSAGE, and STATUS information is sent along the 8-bit (narrow) bus as normal. For these phases, the upper eight data bits on the wide bus could be used for other purposes such as carrying enhanced protection information, including protection coverage on the phase lines (MSG, C/D, and I/O). So long as the protection information only protects the data being transferred during that transition of REQ/ACK, then the protection is separable as well. That is, no change in the underlying COMMAND, MESSAGE, or STATUS phase protocols is needed in order to accommodate the added protection.

Using some of the upper eight bits for added protection would also allow the remaining bits on the bus not required for the protection scheme to be used for additional functions.

3 Protection on COMMAND, MESSAGE, and STATUS

The proposal to implement added protection on COMMAND, MESSAGE, and STATUS phases (including protection on the phase lines) is simple. First, a new value is required to be defined in the PROTOCOL OPTIONS field of the PARALLEL PROTOCOL REQUEST message to set this option.

Second, an adequate protection code needs to be determined, and the items to be encoded need to be specified. The only potential backward compatibility issue identified to date is that expanders must repeat all of the data bits in a wide bus, even in these (inherently narrow) information phases.

Several protection codes were examined by Dr. Lih Weng of Quantum. The following is the code that he recommends for this application. The code is a cyclic binary BCH code:

Code	Maximum data bits allowed	Number of redundant bits	Minimum distance of the code
(21,15,4)	15	6	4

Given the less stressful nature of the asynchronous information transfer phases, and the extremely short code words (approximately 20 bits compared to the thousands of bits during a DT data phase), the requirements for Hamming distance for the BCH code should not be stricter than for the CRC used on the high speed synchronous DT data phases. Earlier calculations indicated that the data CRC has a Hamming distance of at least four for data transfers less than eight kilobytes. This is the same minimum distance provided by this BCH code.

A computer program for the code written in the C language has been made available on the T10 reflector.

The following signals are to be covered by the code. Associated with each signal is its bit location in the 21 bit code word. When a device receives the information byte, it also latches the state of the other SCSI signals and values noted in the table.

Codeword Bit Location	**SCSI Signal**	**Meaning**
0	DB0	Data bit 0 of the information byte
1	DB1	Data bit 1 of the information byte
2	DB2	Data bit 2 of the information byte
3	DB3	Data bit 3 of the information byte
4	DB4	Data bit 4 of the information byte
5	DB5	Data bit 5 of the information byte
6	DB6	Data bit 6 of the information byte
7	DB7	Data bit 7 of the information byte
8	DB8	Reserved
9	DB9	Reserved
10	DB10	Redundant bit 0 of the code word
11	DB11	Redundant bit 1 of the code word
12	DB12	Redundant bit 2 of the code word
13	DB13	Redundant bit 3 of the code word
14	DB14	Redundant bit 4 of the code word
15	DB15	Redundant bit 5 of the code word
16	MSG	Phase control line (see note)
17	C/D	Phase control line (see note)
18	I/O	Phase control line (see note)
19	Seq ID 0	Sequence ID bit 0
20	Seq ID 1	Sequence ID bit 1
Note: For calculation purposes the application client uses the values that should be on these signal lines as determined by the current phase.		

The reserved signals (DB8 and DB9, or bits 8 and 9 of the codeword) can be used for other functions in the future.

The Sequence ID is a “virtual” signal which is carried in the encoding. The Sequence ID serves as the seed for the BCH calculation by the sender. The receiver then uses the expected seed for the transfer for decoding.

The Sequence ID increments in value during a “run”. A “run” is a sequence of transfers during a MESSAGE, COMMAND, or STATUS phase, without an intervening DATA, BUS FREE, ARBITRATION, SELECTION, or RESELECTION phase. In addition, a new run begins with every phase change and every time that ATN is negated.

For each new run, the Sequence ID is set to zero for the first word transferred, one for the second word transferred, two for the third word transferred, and three for the fourth word transferred. The Sequence ID then cycles back to zero for the fifth word transferred, and so forth until the run is complete. At the beginning of the next run, the Sequence ID starts at zero again.

The Sequence ID provides protection for errors where a data transfer is missed or double clocked. If a BCH code error is detected or if a sequence ID value is missing during a run, then the transfer is invalid. Recovery from these protection errors is the same as parity error recovery.

As stated above, this feature must be negotiated in the PPR message exchange as is the DT/CRC protocol. Enhancements to that message will be developed to negotiate for this feature in the next revision of this proposal.

4 Detailed changes in SPI

These will be developed in the next revision of this proposal. It may be decided that this proposal should be included in SPI-4 rather than SPI-3.