Protection for the Asynchronous Information phases (Command, Message, and Status)

To: **T10 Technical committee**
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0 Overview

Rev 0

This proposal is based on SPI-3, revision 2. It is the outgrowth of discussions held at the January T10 SPI working group. A con call will be held before the March T10 meeting, and a revised proposal will be forthcoming after the con call and before the meeting.

1 Introduction

With the advent of CRC on the DT data phases, some customers have requested similar types of protection on non-data information phases (command, message, and status). The primary focus is to provide added protection in those cases where the information may become corrupted (e.g. hot plugging events). The constraint is that it should be a simple, modular addition to the existing SCSI protocol (e.g. these customers desire this capability in a non-packetized SCSI protocol).

Thumbnail Descriptions

In the current DT protocol with CRC, the SCSI bus is restricted to 16 bit (wide) data phases only. COMMAND, MESSAGE, and STATUS information is sent along the 8 bit (narrow) bus as normal. The key observation is that the upper 8 data bits on the wide bus can, for these phases, carry protection information as well. As long as the protection information only protects the data being transferred during that transition of REQ/ACK, then the protection is separable as well. That is, no change in the underlying command, message, or status phase protocols is needed in order to accommodate the added protection.

Note that this implies that the proposal to implement the added protection is simple: first, an adequate code needs to be determined, and the items to be encoded need to be specified. Second, some ability to turn on and off this capability is needed. The only potential backward compatibility issue identified is to insure that expanders repeat all of the data bits in a wide bus, even in these (inherently narrow) information phases.

2 Detailed Proposal

Specific wording changes to SPI-3 will be devised before the T10 meeting. The intent of this revision is to insure adequate prior technical review at the con call.

Several protection codes were examined by Dr Lih Weng of Quantum. The code is a cyclic binary BCH codes:

Code	Maximum data bits allowed	Number of redundant bits	minimum distance of the code
(21,15,4)	15	6	4

Given the less stressful nature of the asynchronous information transfer phases, and the extremely short code words (approximately 20 bits compared to the thousands of bits during a DT data phase), the requirements should not be stricter than for the high speed synchronous DT data phases. Earlier calculations indicated that the data CRC has a Hamming distance of at least 4 for data transfers < 8 Kbytes.

A computer program for the code is available (to be included in the next revision of this proposal).

The following signals are to be covered by the code. Associated with each signal is its bit location in the 21 bit code word. When a device receives the information byte, it also latches the state of the other SCSI signals and values noted in the table.

Codeword bit location	SCSI signal	Meaning
0	DB0	Data bit 0 of the information byte
1	DB1	Data bit 1 of the information byte
2	DB2	Data bit 2 of the information byte
3	DB3	Data bit 3 of the information byte
4	DB4	Data bit 4 of the information byte
5	DB5	Data bit 5 of the information byte
6	DB6	Data bit 6 of the information byte
7	DB7	Data bit 7 of the information byte
8	DB8	Reserved
9	DB9	Reserved
10	DB10	Redundant bit 0 of the code word
11	DB11	Redundant bit 1 of the code word
12	DB12	Redundant bit 2 of the code word
13	DB13	Redundant bit 3 of the code word
14	DB14	Redundant bit 4 of the code word
15	DB15	Redundant bit 5 of the code word
16	MSG	Phase control lines
17	C/D	Phase control lines
18	I/O	Phase control lines
19	Seq ID 0	Sequence ID bit 0
20	Seq ID 1	Sequence ID bit 1

The reserved signals (DB8 and DB9, or bits 8 and 9 of the codeword) can be used for other functions in the future.

Finally, the Sequence ID is a “virtual” signal that increments in value during a “run”. A “run” is a sequence of MESSAGE, COMMAND, and STATUS phases, without an intervening DATA, BUS FREE, ARBITRATION, SELECTION, or RESELECTION phase. So a MESSAGE OUT/COMMAND sequence of phases is a run; a MESSAGE OUT/MESSAGE IN/COMMAND sequence of phases is a run; a COMMAND/DATA OUT/STATUS/MESSAGE IN is two runs.

During a run, the Sequence ID is set to 0 for the first word transferred, 1 for the second word transferred, 2 for the third word transferred, and 3 for the fourth word transferred. It then cycles back to 0 for the fifth word transferred, and so forth until the run is complete. At the beginning of the next run, the Sequence ID starts at 0 again.

While the CRC protects against errors in a given data transfer, the sequence ID provides some protection for errors where a data transfer is missed or double clocked. If either a CRC error is detected, or if a sequence ID value is missing during a run, then the transfer is invalid. Recovery from these protection errors is the same as parity error recovery.

Note that this feature must be negotiated in the PPR message exchange as is the DT/CRC protocol itself. Enhancements to that message will be developed to allow this feature (in the next revision of this proposal).

3 Changes in SPI-3

To be developed in the next revision.