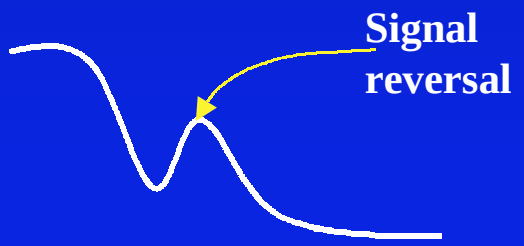
Interaction of QAS & Glitch Filters

- SPI-3 recommends “Glitch Filters” on the REQ & ACK signals
- What is a Glitch Filter?
  - Typically, the purpose of a SCSI glitch filter is to suppress apparent signal reversals following a signal transition. The reversal is caused by reflections accentuated by impedance discontinuities in the cable plant.



Filter Parameters

- SPI-2: “The filter period shall not be so long as to mask out the subsequent valid edges of the incoming REQ/REQQ and ACK/ACKQ signals.”
- Implementations vary widely within this budget. An filter in Fast-10 transfers could be as long as 30ns by spec, and perhaps longer during asynchronous transfers.
- A given chip could vary by 3:1 across process, temperature, & voltage.

Filter Necessity

- There are many systems with impedance discontinuities.
- Some SCSI devices are wildly out-of-spec for input capacitance and stub length.
- Lack of glitch filters causes unreliable operation in these environments.

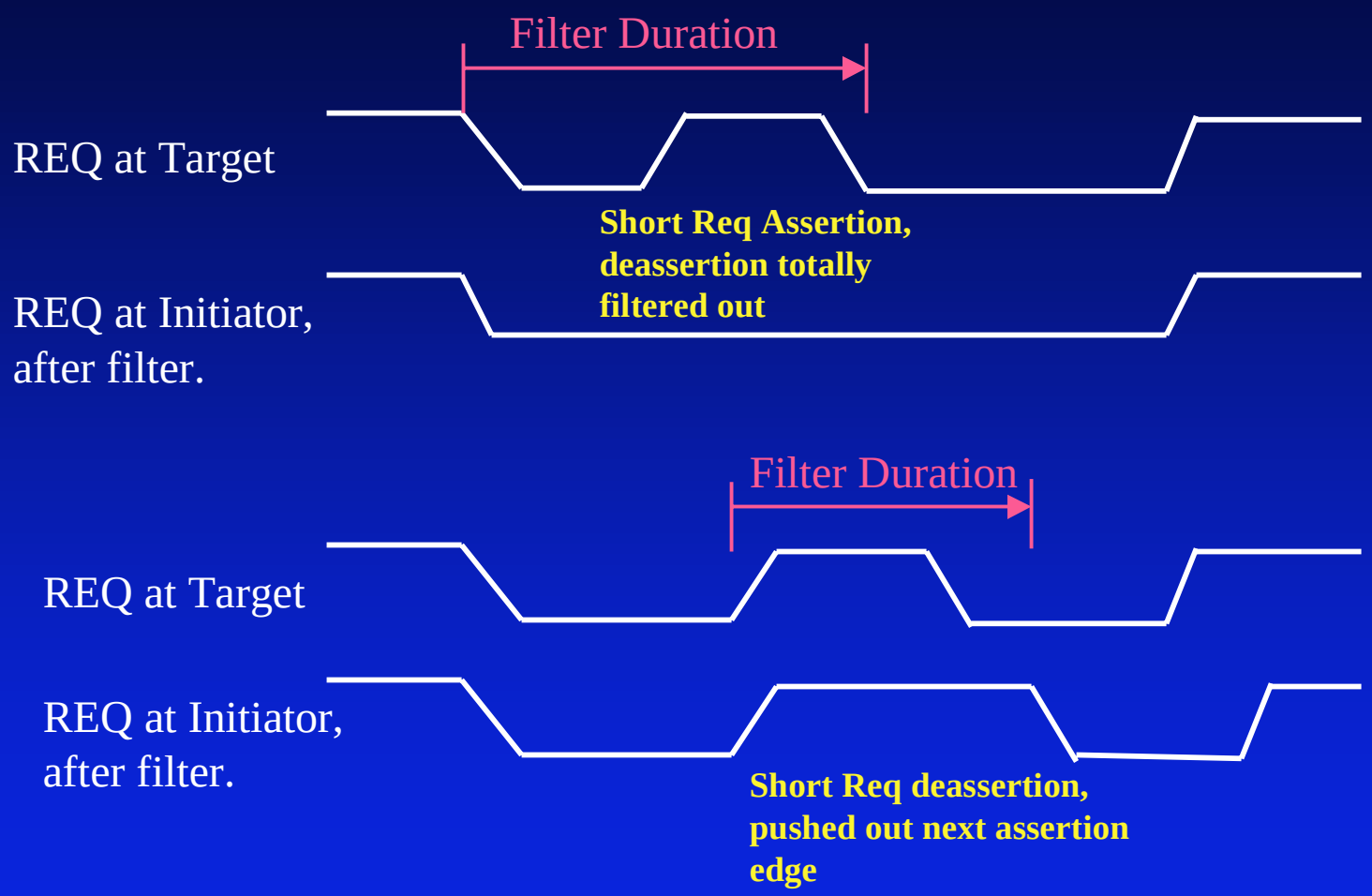
QAS

- QAS should require targets to add glitch filters on REQ, and initiators add them on ACK.
- The variation in filter length between different SCSI devices could prevent “bus snooping” from working.

QAS (continued)

- SPI-2 has no spec for minimum pulse width asserted or deasserted for REQ or ACK during asynchronous transfers.
- Devices with short glitch filters could have fast pulse widths which could distort or hide pulses from devices with longer filter times.

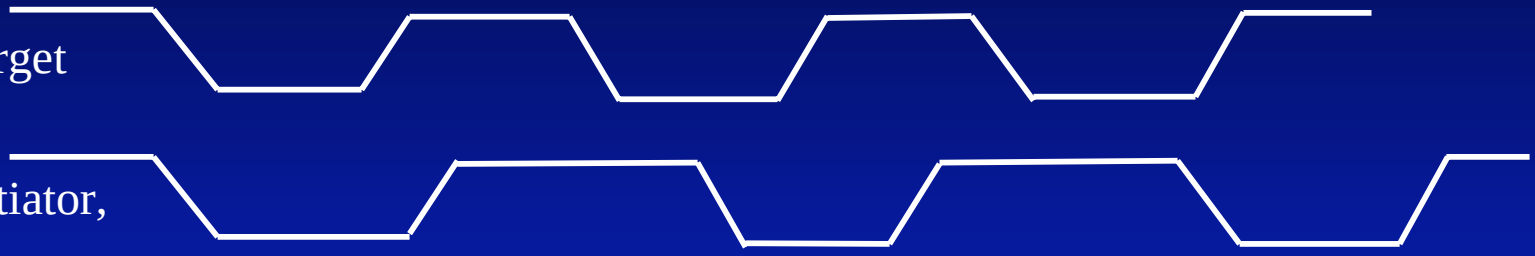
Asynchronous Transfer Examples



Effect Can Be Cumulative

REQ at Target

REQ at Initiator,
after filter.



Fixes?

- Spec'ing longer de-assertion times for QAS messages doesn't help - messages snooped from non-QAS devices could still be misinterpreted.
- Requiring relatively short glitch filters for QAS devices might work - BUT some system vendors would likely have signal integrity problems.
- Restricting QAS to LVD might help - reflection glitches can occur in LVD systems but should be less common.