Sun Microsystems, Inc.
2550 Garcia Avenue
Mountain View, CA 94045
415 960-1300

March 9,1999

John Lohmeyer
Chairman, T10
4420 Arrows West Drive
Colorado Springs, CO 80907-3444

Subject: Passive Lumped Capacitance Compensation on SCSI Signal Lines

Dear Mr. Lohmeyer:

This is a continuation of Sun's effort to simulate LVD SCSI bus environment consisting of an initiator, 3m cable, and differntial backplane at speeds of 160 and 320 Mtransfers/second. With a wide bus and double clocking, this would transform into 640 and 1280 MB/sec speed on the SCSI bus consecutively.

Our criteria for the simulation were defined at the last meeting in November 1998 in Plam Springs as follows:

1) Use 3 - 4 " stub.
2) Drive the bus from a host adapter (HA) 3 m apart.
3) Use 2 pF termination model.
4) Introduce ISI.
5) Introduce losses.

We used 30 AWG twisted pair 3m lossy cable and lossy backplanes for the simulation. We ran the simulations on one differential pair and did not consider any crosstalk. In the attached paper, we show that the stub length had to be shortend and the input capacitance lowered to create a working system. With a 4" stub and 12pF input capacitance not even compensation would yield usable results. On the other side, with a 1" stub length plus a connector and 5 pF input capacitance, the 160 Mtransfers/sec bus works fine even without a compensation.

With the exception of crosstalk, this is a very realistic simulation of a lossy environment. We have a high confidence based on our experience with modelling lossy backplanes that these results are correct and think that the 160 Mt/sec LVD SCSI bus will work without compensation with the mentioned parameters. The 320 Mt/sec (1,28GB/sec wide SCSI bus with double clocking) will however need some kind of compensation for a reasonable margin.

Sincerely,

Vit F. Novak
Sun Microsystems

Feasibility Simulations of Differential SCSI Backplanes at 160 and 320 Mt/sec Speeds

I. Topology and simulation parameters:

* Node naming convention:
* first two digits: slot number
* third digit: 1: upper trace
* 2: lower trace
* fourth digit: 1: Cvia, SCA-2 connector
* 2: **********
* 3: **********
* 4: **********
* 5: **********
* 6: **********
* 7: stub and SCSI device Cin

Main circuit topology

* Driver

```
Xdriver      dr10    dr20    Drv320ISI
```

* Input cable and bus traces

```
Xcable               dr10    0010    dr20    0020    diff_cable length=cable_length

Xlineleft    0010    0112    0020    0122    diff_trace length=term_spacing

Xline0102    0113    0212    0123    0222    diff_trace length=slot_spacing
Xline0203    0213    0312    0223    0322    diff_trace length=slot_spacing
Xline0304    0313    0412    0323    0422    diff_trace length=slot_spacing
Xline0405    0413    0512    0423    0522    diff_trace length=slot_spacing
Xline0506    0513    0612    0523    0622    diff_trace length=slot_spacing
Xline0607    0613    0712    0623    0722    diff_trace length=slot_spacing
Xline0708    0713    0812    0723    0822    diff_trace length=slot_spacing
Xline0809    0813    0912    0823    0922    diff_trace length=slot_spacing
Xline0910    0913    1012    0923    1022    diff_trace length=slot_spacing
Xline1011    1013    1112    1023    1122    diff_trace length=slot_spacing
Xline1112    1113    1212    1123    1222    diff_trace length=slot_spacing
```

```
Xlineright      1213    1310    1223    1320    diff_trace length=term_spacing
Xtermright      1310    1320    Term_nom
```

Main simulation parameters at 320Mt/sec:

```
.options list node post
.option RISETIME=200ps
.tran 5ps 60ns

.param term_b=125
.param term_a=52
.param slot_spacing=1.5          $ in inch
.param term_spacing=0.75         $ in inch
.param stub_length=0.75          $ in inch
.param cable_length=3            $ in meters
*
.param source_a=50
.param source_b=50

* Via capacitance
.param Cvia=1e-12
*
* Drive input capacitance
.param Ci=2.5pF
```

Configurations:

All of the waveforms shown below were generated with

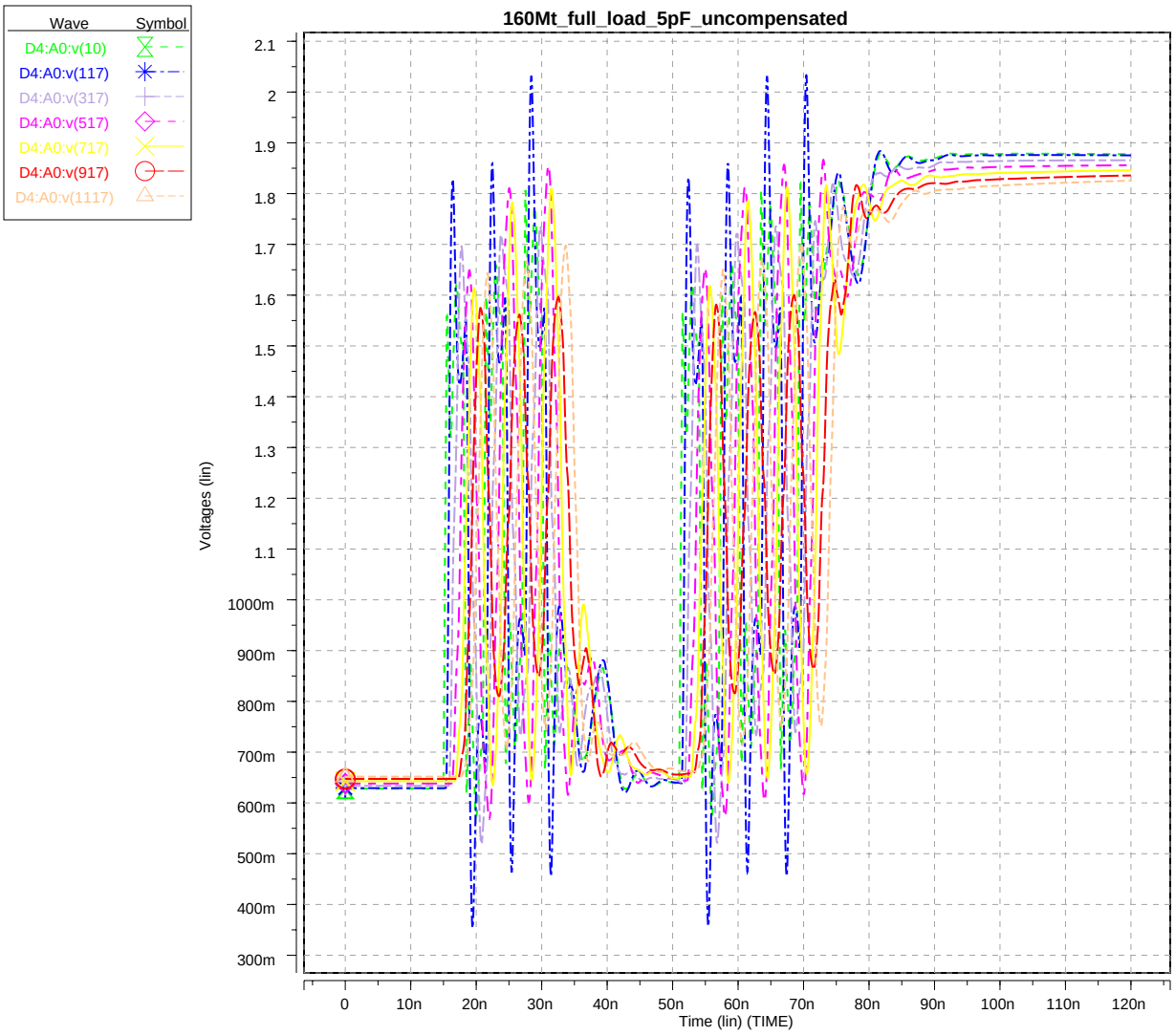
- HSPICE, w-line lossy interconnect models
- the 3-meter lossy cable connected to the left end of the backplane,
- a differential termination connected to the right end of the backplane
- all slots populated with the same equivalent circuit:
  - via
  - SCA-2 connector pin
  - trace (stub)
  - input capacitance of drive electronics

Topologies with different slot and drive configurations have not been simulated.

II. Simulated waveforms

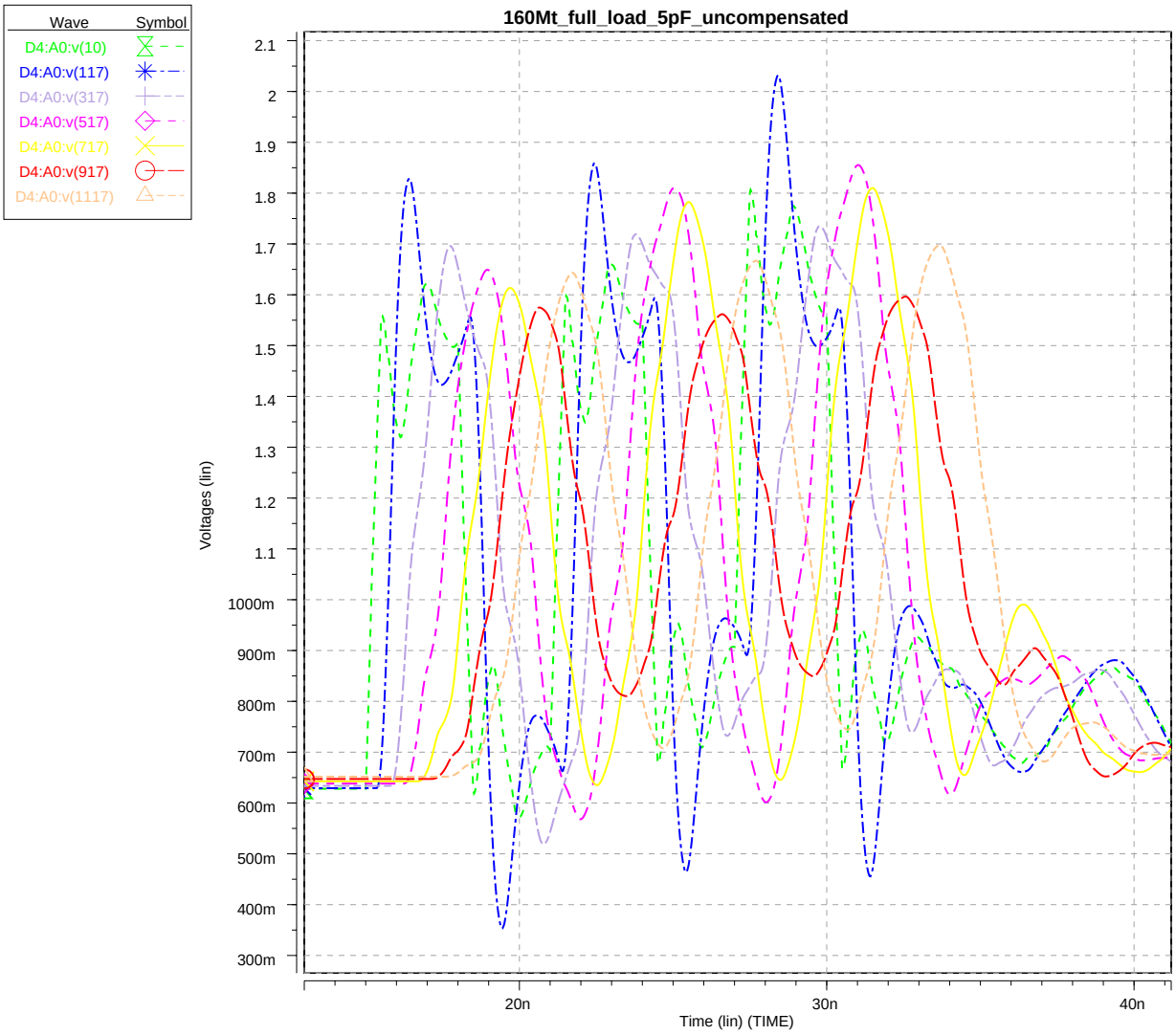
160Mt/sec speed, no compensation, full time scale:

Stub length: 1”
Drive input capacitance: 5pF



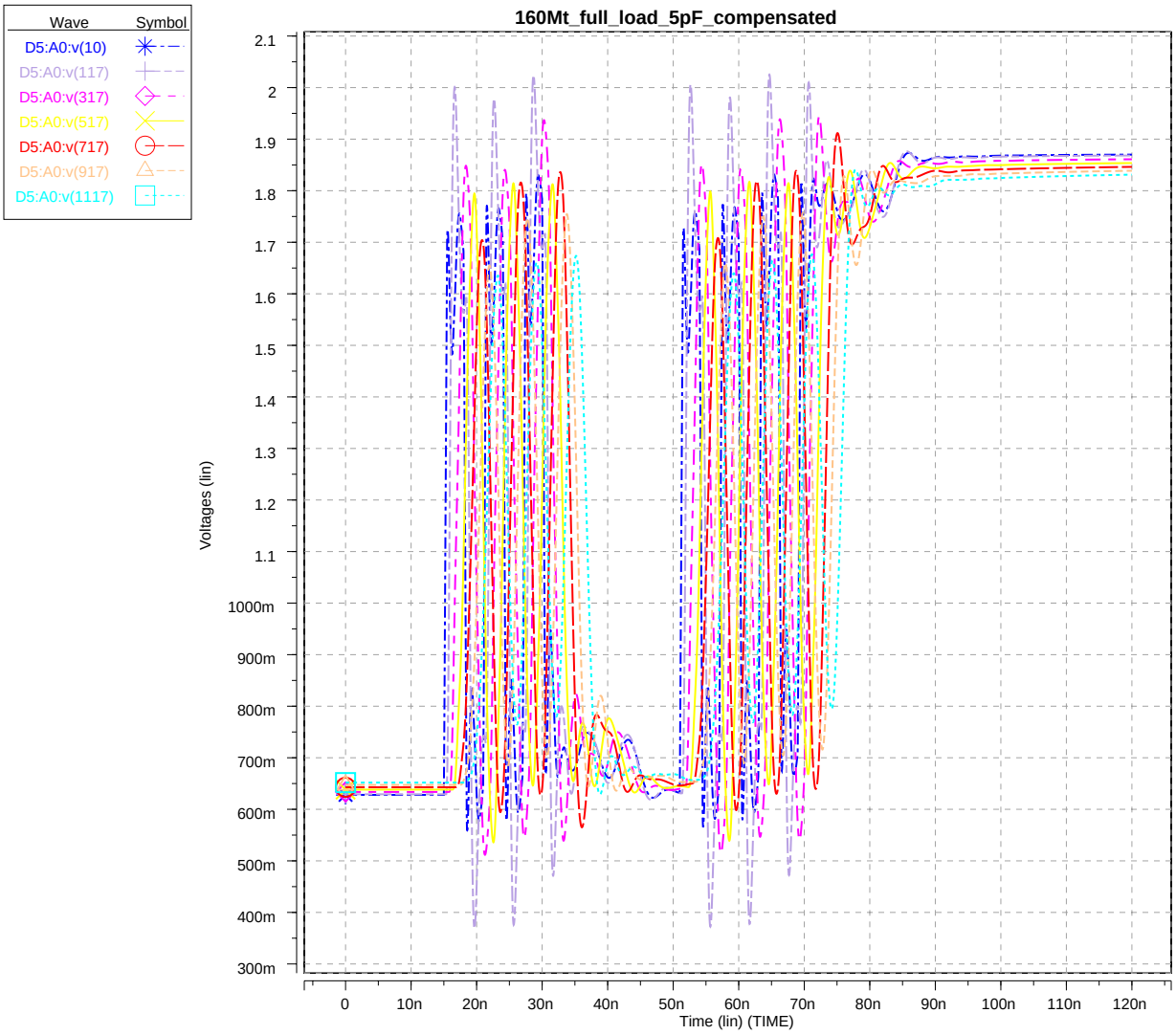
160Mt/sec speed, no compensation, zoomed time scale:

Stub length: 1”
Drive input capacitance: 5pF



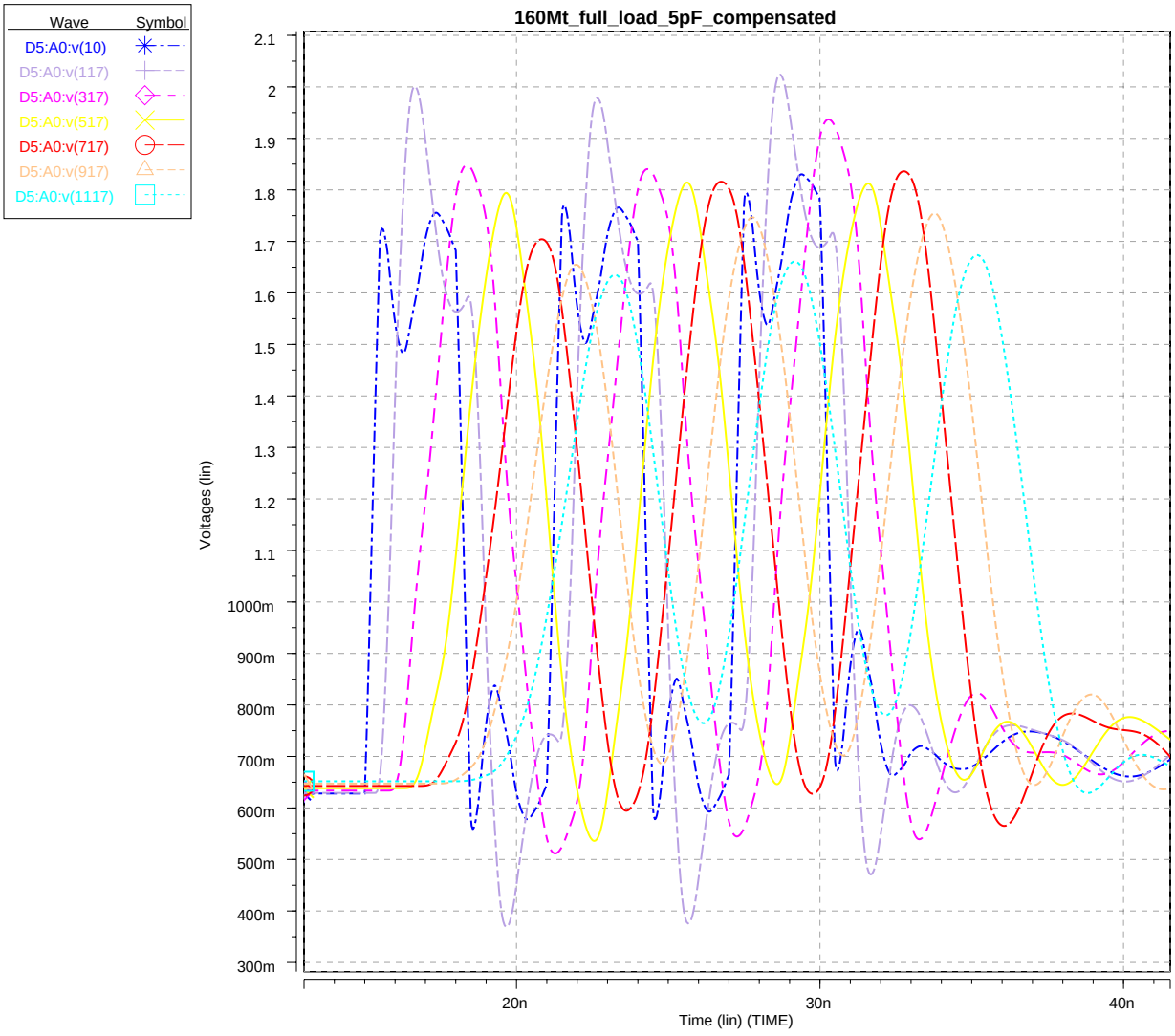
160Mt/sec speed, with compensation, full time scale:

Stub length: 1”
Drive input capacitance: 5pF



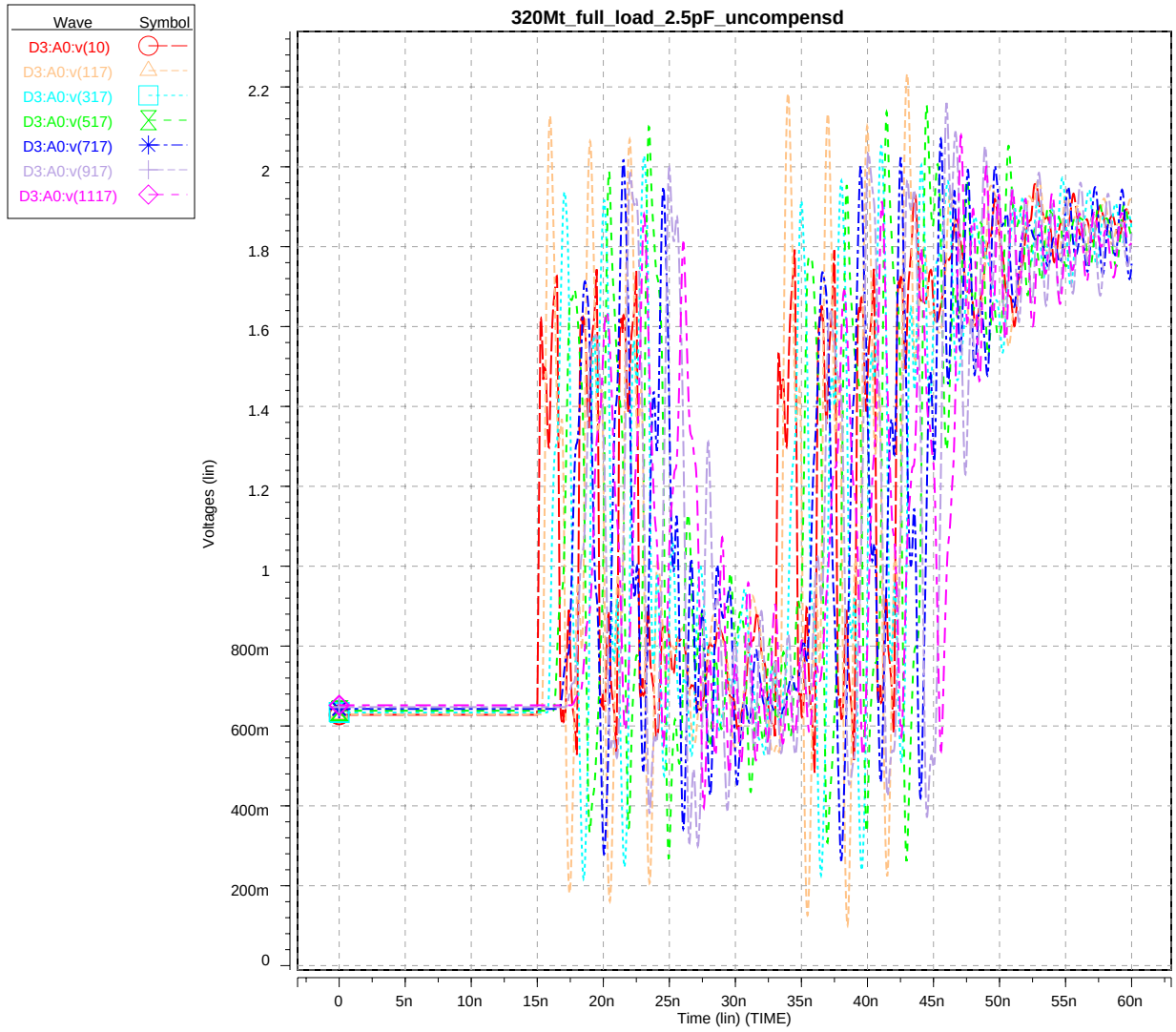
160Mt/sec speed, with compensation, zoomed time scale:

Stub length: 1”
Drive input capacitance: 5pF



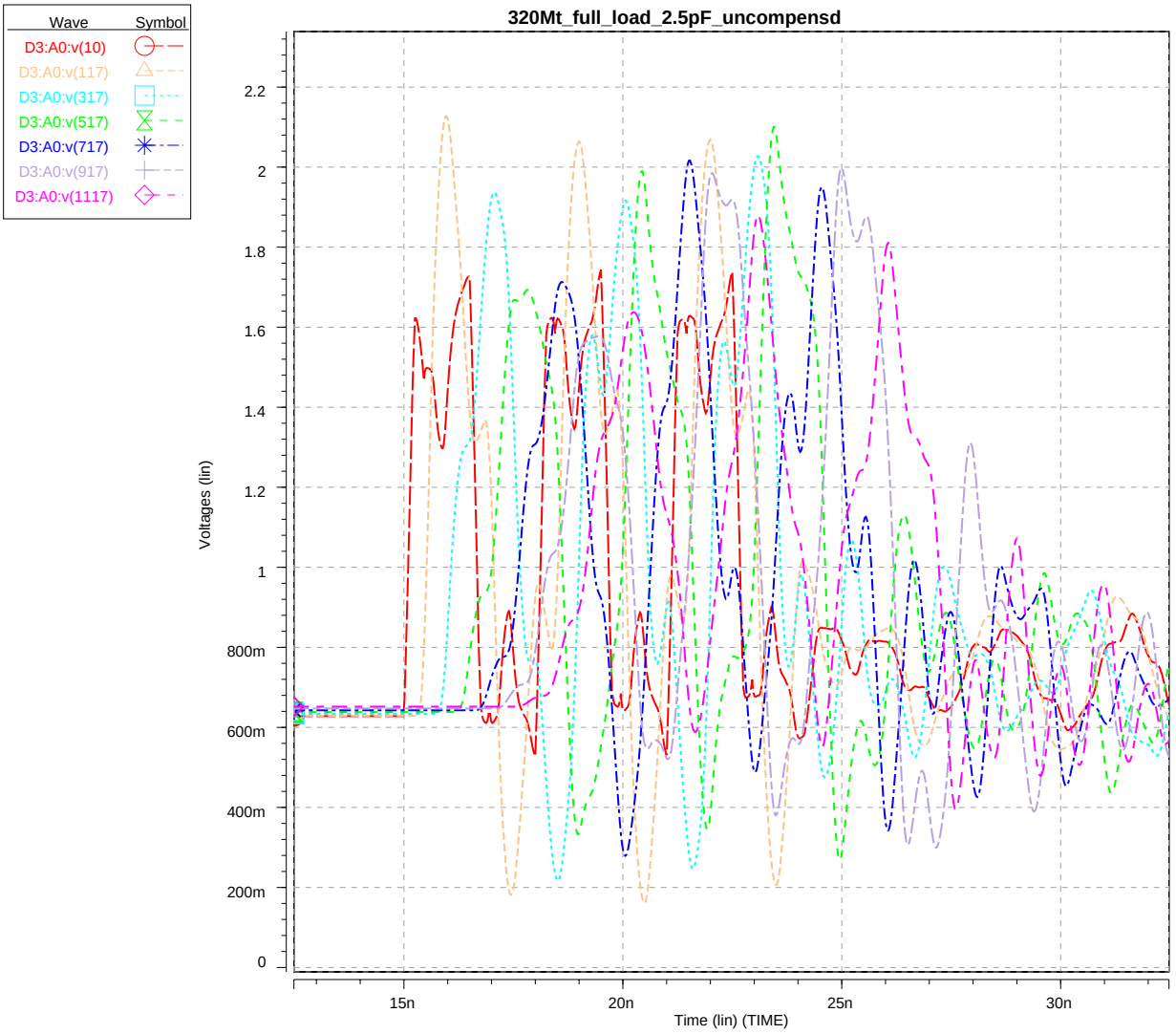
320Mt/sec speed, no compensation, full time scale:

Stub length: 0.75”
Drive input capacitance: 2.5pF



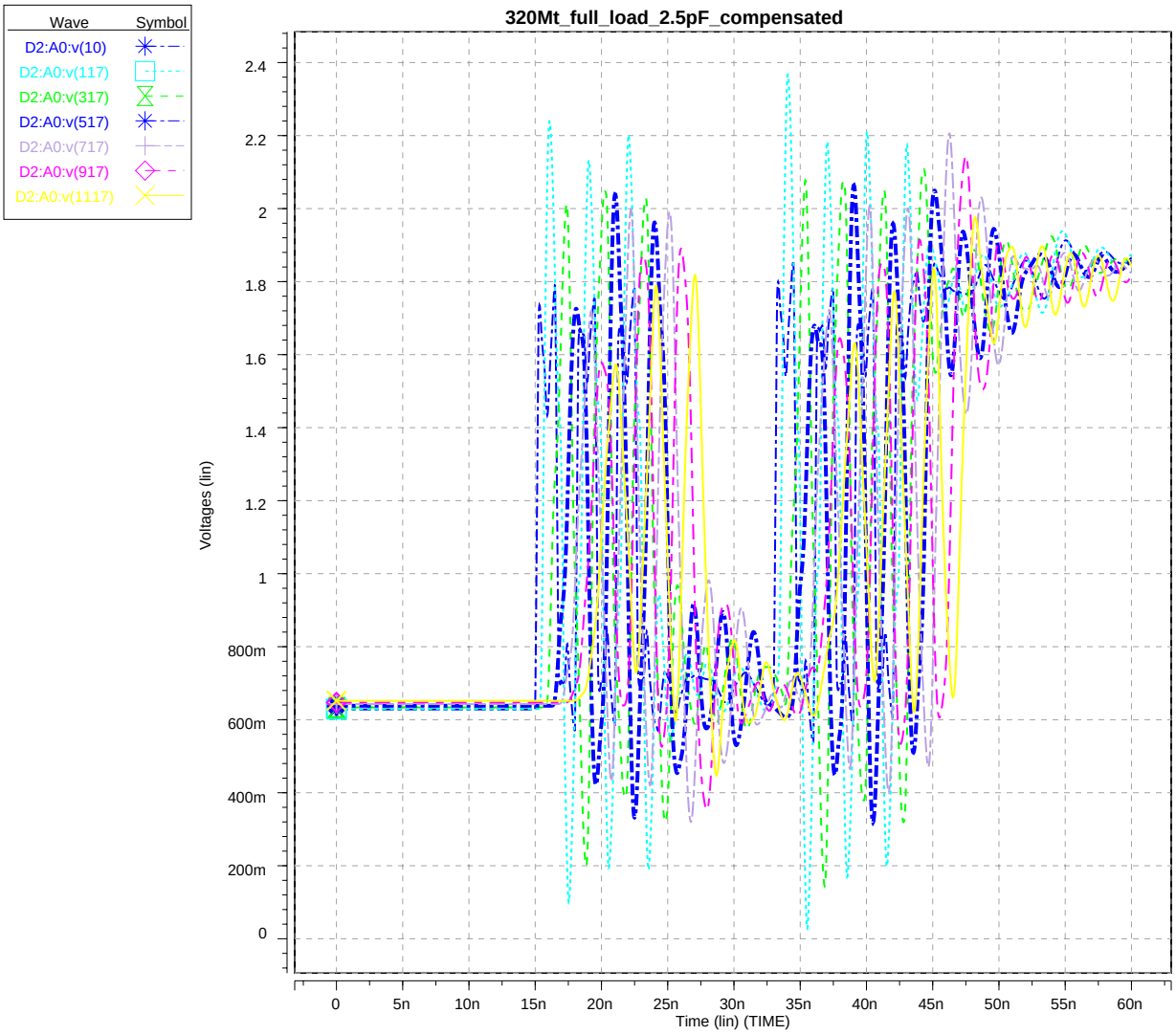
320Mt/sec speed, no compensation, zoomed time scale:

Stub length: 0.75”
Drive input capacitance: 2.5pF



320Mt/sec speed, with compensation, full time scale:

Stub length: 0.75”
Drive input capacitance: 2.5pF



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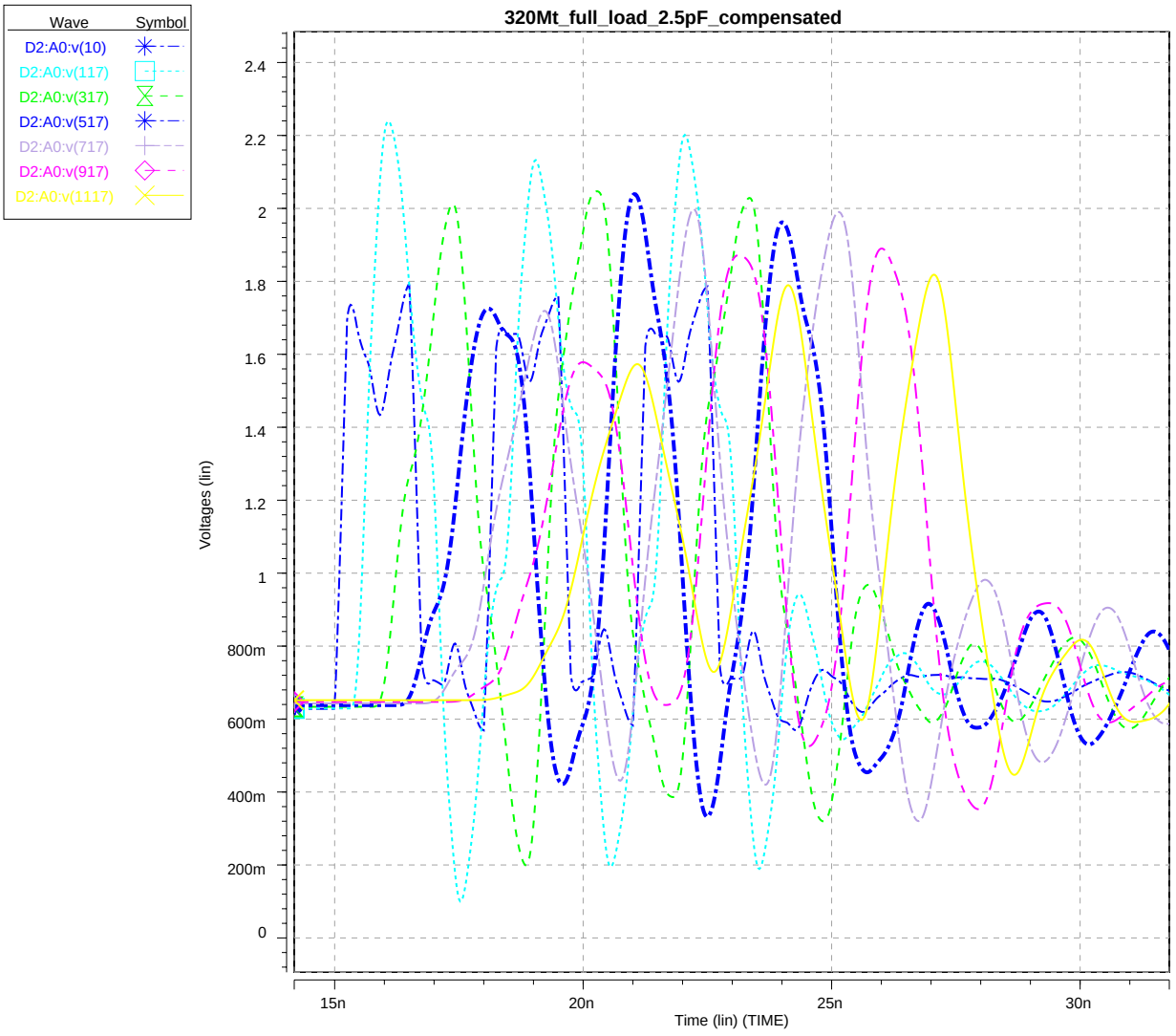

III. Conclusions

The simulation models included the lossy input cable, lossy backplane traces, plated-through-hole capacitance, connector, trace and drive-input-capacitance models. Through the lossy w-line models, the single-line simulations correctly discribe the losses, impedance mismatches and delay-related ringings/reflections. The simulations did not include crosstalk or any other multi-line effect. The simulations also did not include at this time the effect of different slot populations and drive configurations.

At higher speeds, the dominant limiting factor are the stub length and load capacitance. At every connector location, a stub is created by the connector and the trace going to the transceiver chip. At present, the connector is assumed to be the SCA-2 connector, which amounts to about 114psec delay. The connector and stub are in series, their delays can be added. The stub delay is: tpd_stub=tpd_connector+tpd_trace. The load capacitance was modeled separately by a lumped 1pF via capacitance at the connector, and the Cin input capacitance of the transceiver. The two capacitors at the two opposite ends of the stub. The sum of the load capacitances at one slot: Cload_sum=Cvia+Cin.

At 160Mt/sec speeds, compensation seems to be possible for up to 1” trace length (plus the 144psec connector delay) and 5pF drive input capacitance (plus 1pF via capacitance.

At 320 Mt/sec speeds, compensation seems to be possible for up to 0.75” trace length (plus 144psec connector delay) and 2.5pF drive input capacitance (plus 1pF via capacitance.

At both speeds, the compensation provides approximately 600-800mVpp single-ended noise margin, which may be enough even after degrading by multi-line noise and slot-configuration effects.