Policy Issues for Ultra3 Items: Applicability to 16 vs 8 bit Buses and LVD vs Single Ended Signaling

To: **T10 Technical committee**
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Date: **September 11,1998**

0 Overview

Rev 0

This proposal in response to some issues raised with respect to 98-177. Some people noted to me that there is no solid technical basis for looking at how Double Transition clocking/CRC applies based on bus width and signaling technology – or at least no more so than for the other items on our Ultra3 list: Domain Validation, Packetized, and QAS.

I would like the committee to consider these other issues with the goal of making a consistent and easily explainable rational for our decisions to customers who will be using Ultra3 technology in the future.

1 Options

For each Ultra3 item, I think we have the following options:

For each mode (16 bit, 8 bit, LVD, single ended), we have to either allow it, disallow it, be silent on it, or perhaps recommend it over another option. A table of such choices (along with the DT/CRC item) appears below:

Options		DT/CRC	Domain Validation	Packetized	QAS
32/16 bit	8 bit				
Allow	Disallow				
Allow	Silent				
Recommend	Allow				
Allow	Allow				
LVD	Single Ended				
Allow	Disallow				
Allow	Silent				
Recommend	Allow				
Allow	Allow				

2 Recomendation

My recommendations are as follows:

Options		DT/CRC	Domain Validation	Packetized	QAS
32/16 bit	8 bit				
Allow	Disallow				
Allow	Silent	X	X	X	X
Recommend	Allow				
Allow	Allow				
LVD	Single Ended				
Allow	Disallow				
Allow	Silent	X	X	X	X
Recommend	Allow				
Allow	Allow				

Which has the virtue of a consistent position for Ultra3 (focus on 16 bit LVD, and allow time to get feedback on whether any other combination would be useful before defining it.