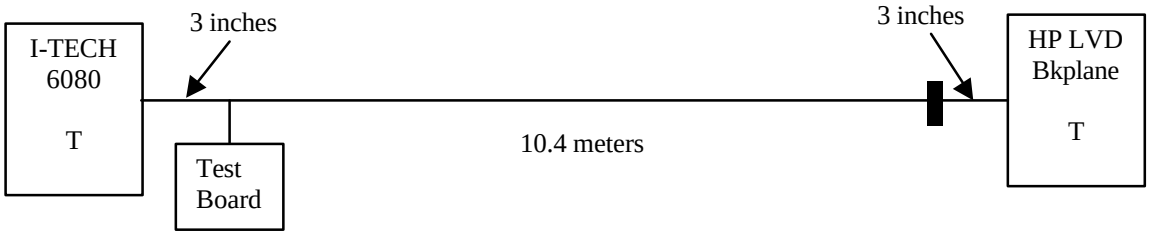
Fast-80 Case Study – Data Pattern Dependent Effects

Objective: Partially answer the question, "What effect does data pattern have on Fast-80 data bit amplitude, assertion/negation period, and setup/hold times?"

The long term purpose is to provide data for deciding whether SPI-2 configuration limits will have to made more stringent in SPI-3.

Caveat: Measurements were only taken in one configuration. I believe 3 or 4 more such studies with different cable plant and load configurations will be necessary before we can reasonably predict the effect of a given configuration on Fast-80 LVD signals. There will always be some uncertainty.

Physical
Configuration: This was a "simulated host" configuration with the target test board only 3" from the ITECH initiator. The 6-device backplane was connected on the other side of the target test board through a 10.4m shielded cable and a 3" ribbon cable (for physical compatibility). The REQ and data signals should appear at the backplane with essentially the same characteristics as ACK and data in a real system.



Device Loads: PCBs from QuantumViking II LVD SCSI drives were plugged into slots in the backplane and power was applied. The nominal node capacitance of the Viking II is 15pf.

Transfer Rate: All measurements were made while executing a 512 byte READ BUFFER command with Fast-80 double transition transfers enabled on the test board. The buffer was loaded originally in Fast-40 mode from the I-TECH 6080.

Data Pattern: Measurements were taken first with 512 byte patterns designed to stress the "isolated one" and "isolated zero" cases. For comparison, worst case isolated ones and zeros were then measured in 4 random-data blocks.

Pattern 1: Isolated one
The 512 byte block was divided into 8 sections of 64 bytes each. Each section was filled with all zeros except for data bit 5. Bit 5 was written in

each block to give the following patterns -

01010101…	Alternating zero/one pattern
001001001….	Two zeros before an isolated one
000100010001…	Three zeros before an isolated one
0000100001…	Four zeros before an isolated one
000001000001…	Five zeros before an isolated one
00000010000001…	Six zeros before an isolated one
0000000100000001…	Seven zeros before an isolated one
000000001000000001..	Eight zeros before an isolated one

Pattern 2: Isolated zero

The 512 byte block was divided into 8 sections of 64 bytes each. Each section was filled with all ones except for data bit 5. Bit 5 was written in each block to give the following patterns -

10101010…	Alternating one/zero pattern
110110110….	Two ones before an isolated zero
111011101110…	Three ones before an isolated zero
1111011110…	Four ones before an isolated zero
111110111110…	Five ones before an isolated zero
11111101111110…	Six ones before an isolated zero
1111111011111110…	Seven ones before an isolated zero
111111110111111110..	Eight ones before an isolated zero

In each of the two cases, only parity bit 0 is toggling along with bit 5. All other bits are static through the whole block, so crosstalk effects should be minimized. Variations in the DB5 signal should be primarily due to the preceding bit pattern, e.g. ISI.

Test Equipment: HP 1.5 GHz scope with Tektronix 1GHz differential probes

Cables: SPI-2 compliant round and ribbon cable for LVD.

******See T10/98-192r0 for detailed specs of test equipment and cable plant.

Measurement Description

A differential oscilloscope capture was made of DB5 and REQ as the block was transferred. For each pattern, the minimum asserted (or negated) level of the isolated one (or zero) was selected. Voltage level, assertion (or negation) period, and setup and hold times were measured. These measurements are presented in table form, followed by some representative traces.

Captured .bmp files of all traces are available to anyone who wants to study them.

Summary of Measured Values

Isolated One Test Case

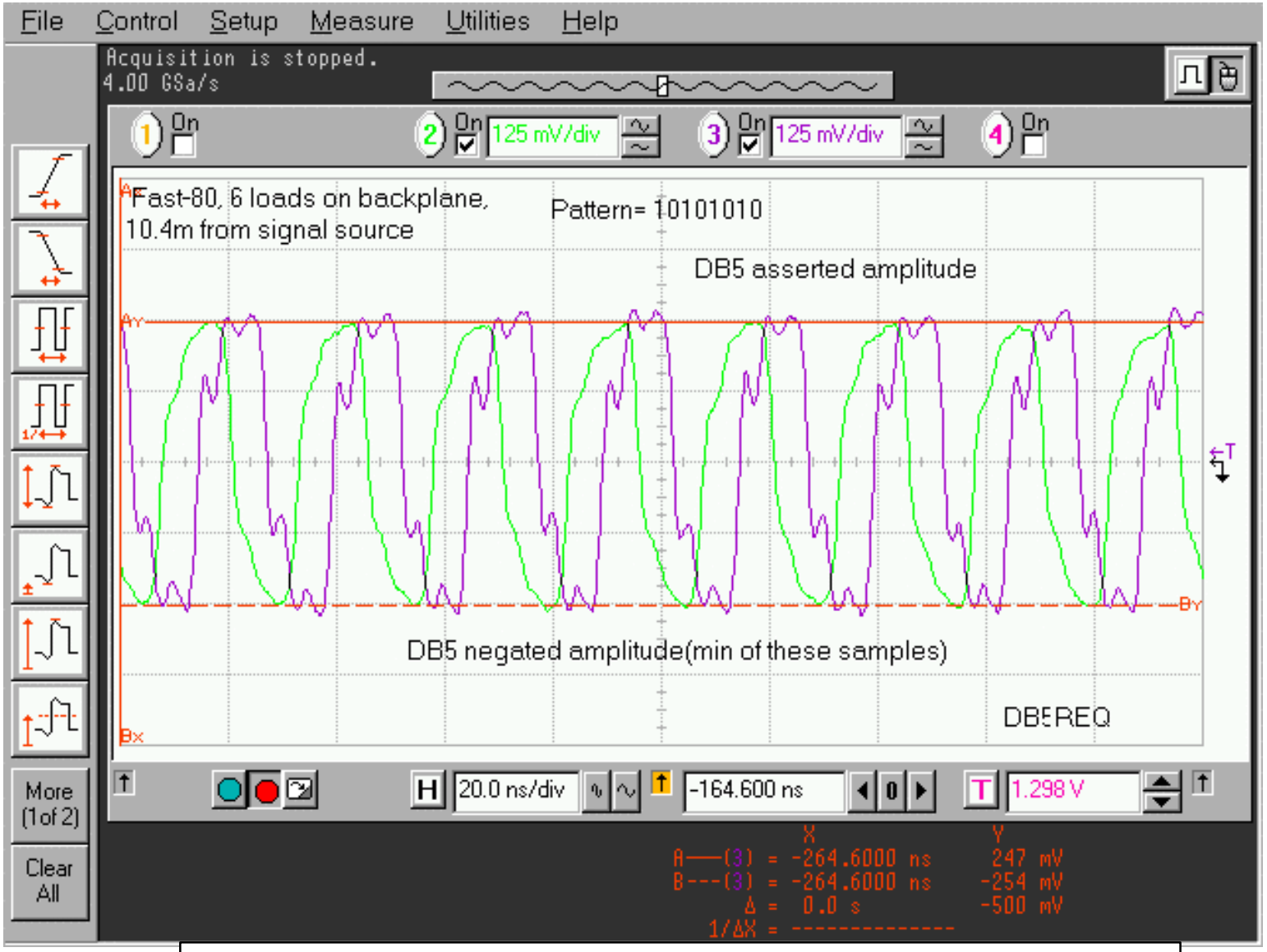
Pattern	Amplitude (mv)	Preceding Bit Amplitude (mv)	Assertion Period (ns)	Setup Time (ns)	Hold Time (ns)
010	245	-257	12.9	6.7	6.2
0010	202	-365	12.4	5.6	6.8
00010	205	-375	12.1	6.4	5.7
000010	194	-396	12.2	5.4	6.8
0000010	198	-392	11.9	6.1	5.8
00000010	222	-392	12.1	6.1	6.0
000000010	208	-396	12.1	6.4	5.7
0000000010	198	-396	12.0	6.0	6.0

Isolated Zero Test Case

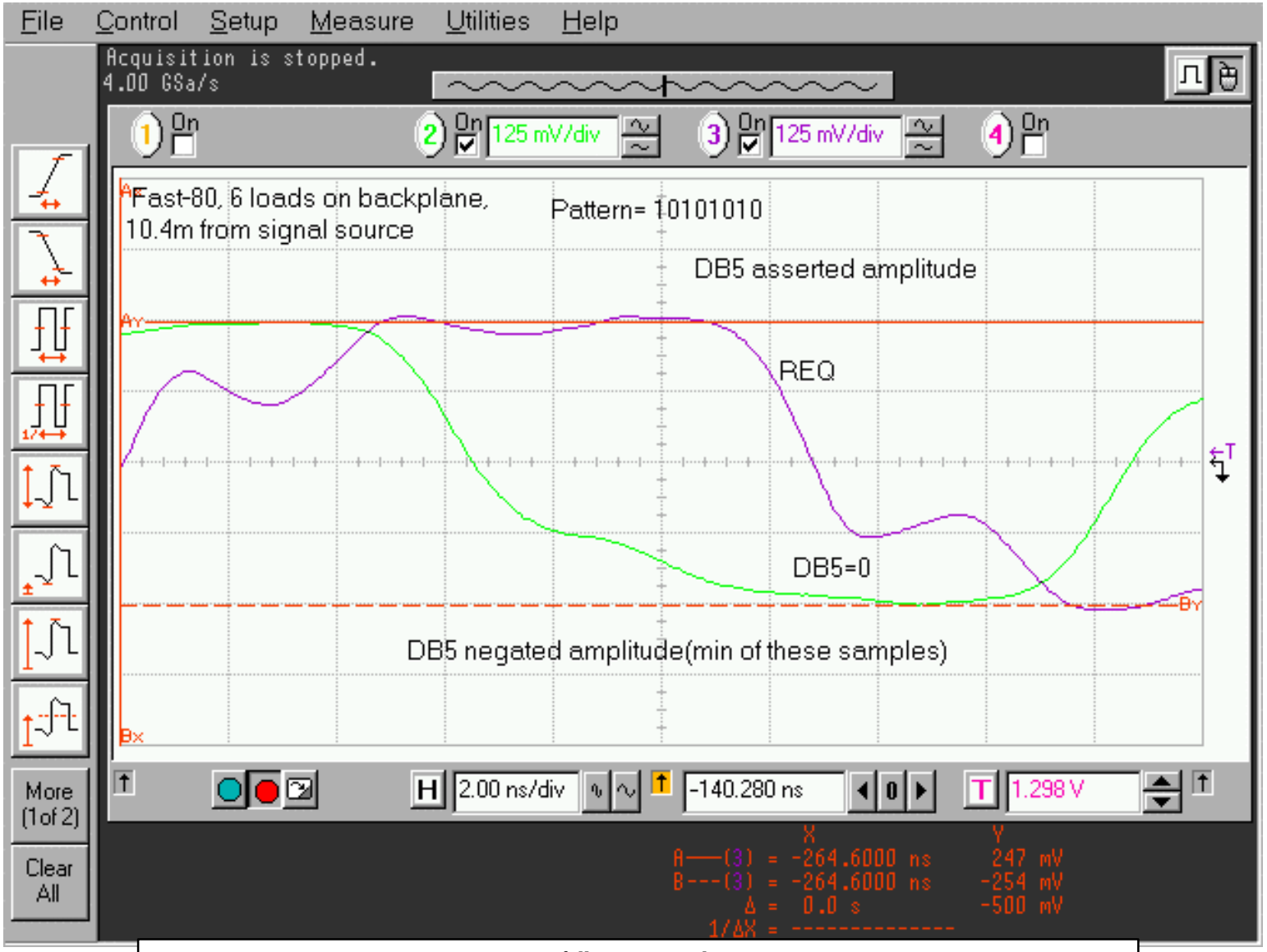
Pattern	Amplitude (mv)	Preceding Bit Amplitude (mv)	Negation Period (mv)	Setup Time (mv)	Hold Time (mv)
101	-254	247	12.2	6.3	5.9
1101	-213	361	11.2	5.1	6.1
11101	-213	392	11.4	5.9	5.5
111101	-198	399	11.0	4.8	6.2
1111101	-201	392	11.2	5.7	5.5
11111101	-207	396	11.0	5.0	6.0
111111101	-207	398	11.4	5.9	5.5
1111111101	-198	401	10.8	5.4	5.4

Random-data Minimum Amplitude Summary

Pattern	Amplitude, Min. one (mv)	Amplitude, Min. zero (mv)	Preceding Bit Amplitude (mv)	Number of Preceding Bits	Assertion Period (ns)	Setup Time (ns)	Hold Time (ns)
Random01	208		-347	6	12.3	5.7	6.6
		-194	382	3	11.2	4.9	6.3
Random02	205		-342	5	12.4	5.6	6.8
		-191	392	5	10.9	5.5	5.4
Random03	206		-351	3	12.2	6.1	6.1
		-191	358	4	10.9	5.8	5.1
Random04	202		-351	5	12.1	5.6	6.5
		-188	403	5	10.9	4.6	6.3

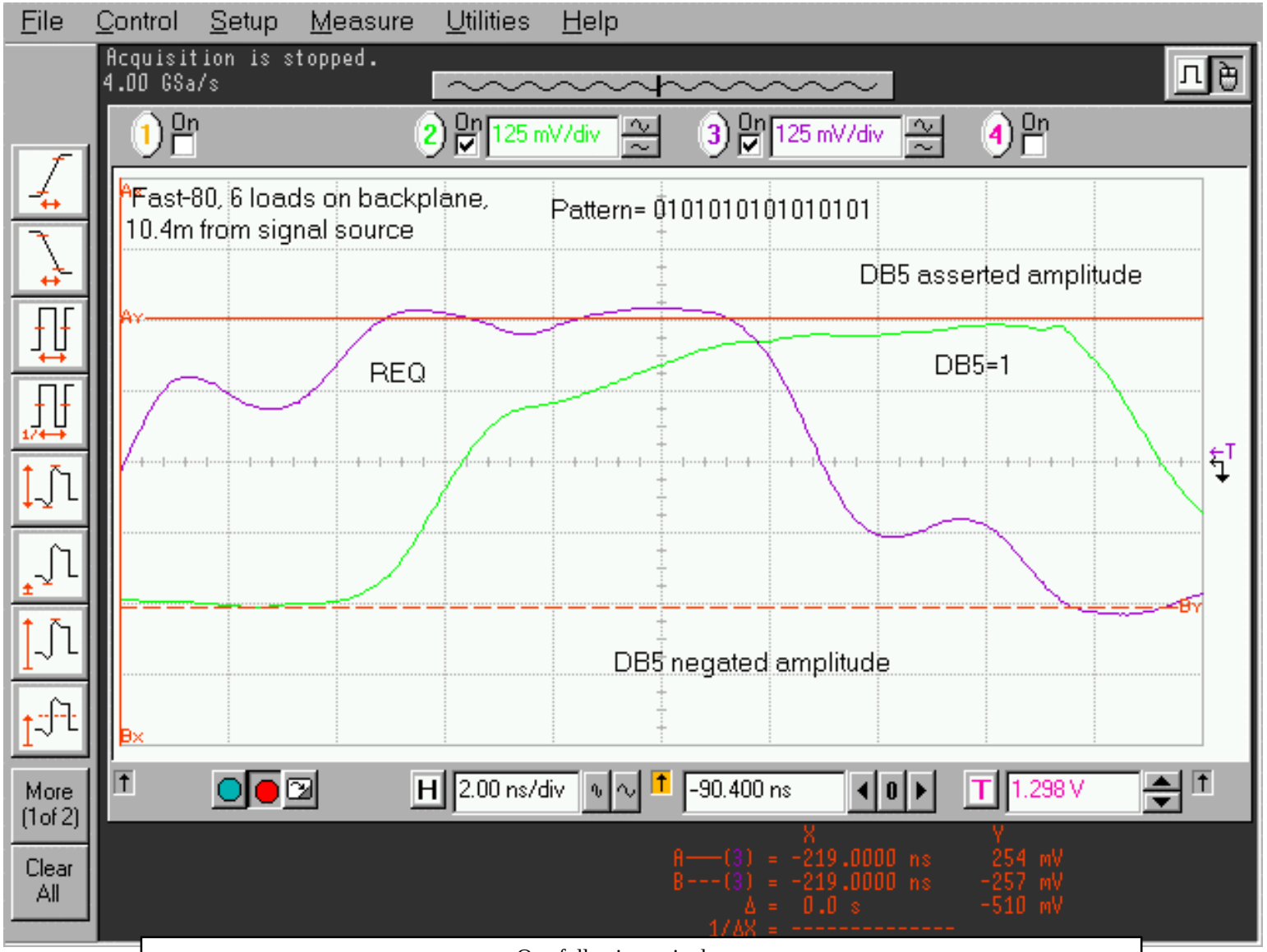


Zero following a single one.



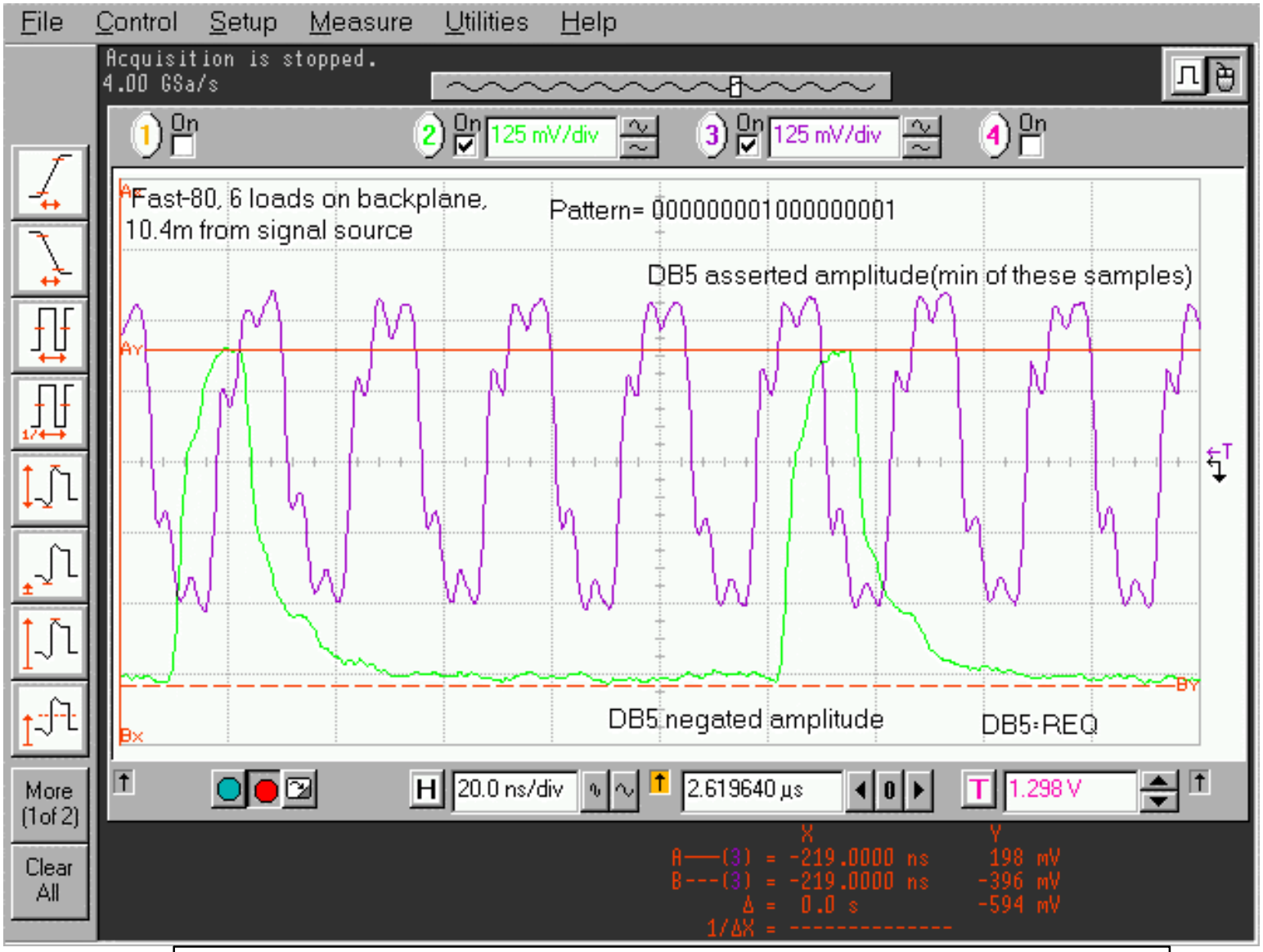
Zero following a single one.

Amplitude -254mv
Negation period 12.2ns
Setup time 6.3ns
Hold time 5.9ns

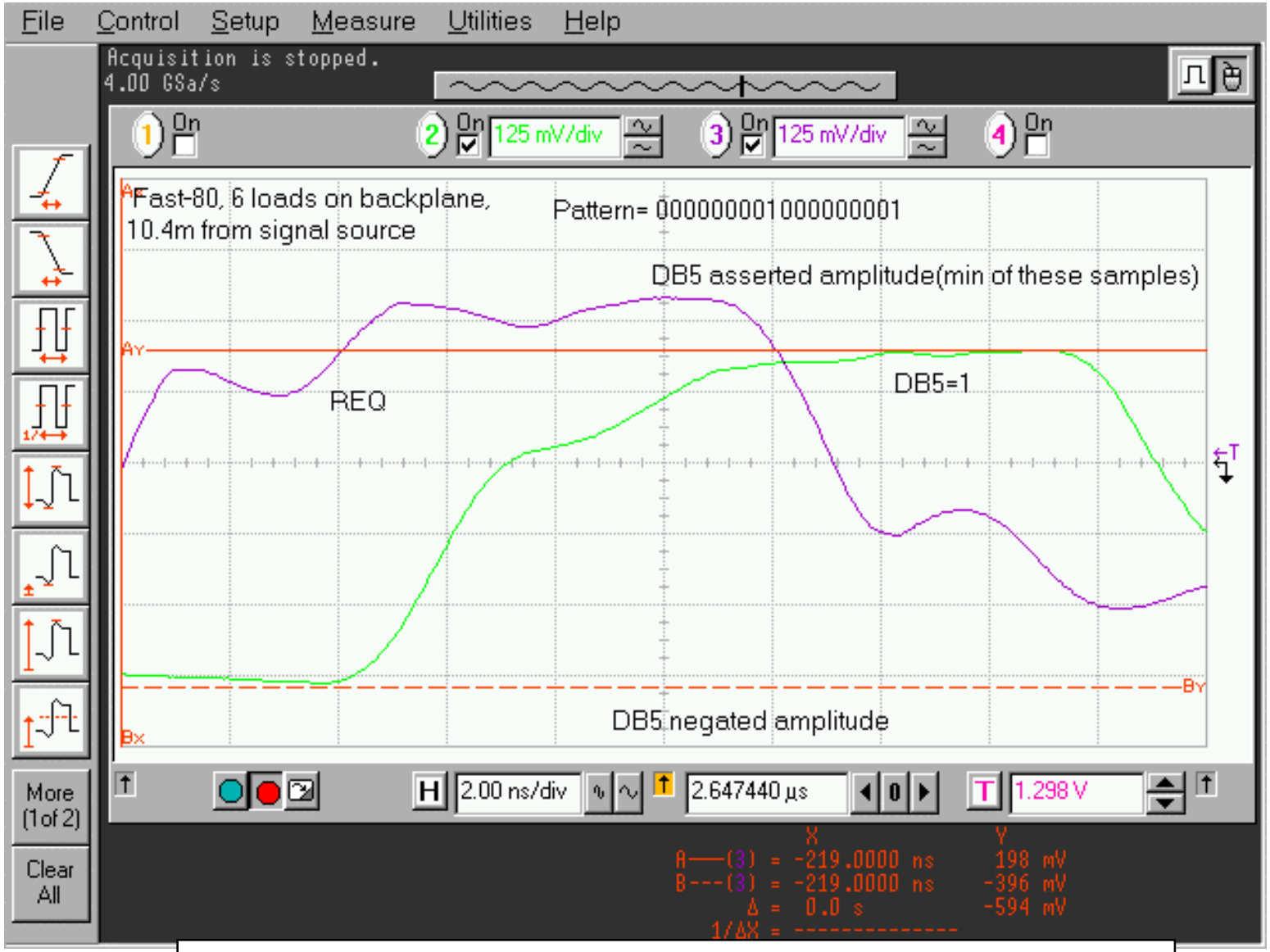


One following a single zero.

Amplitude 245mv (marker is misplaced on screen capture)
Negation period 12.9ns
Setup time 6.7ns
Hold time 6.2ns

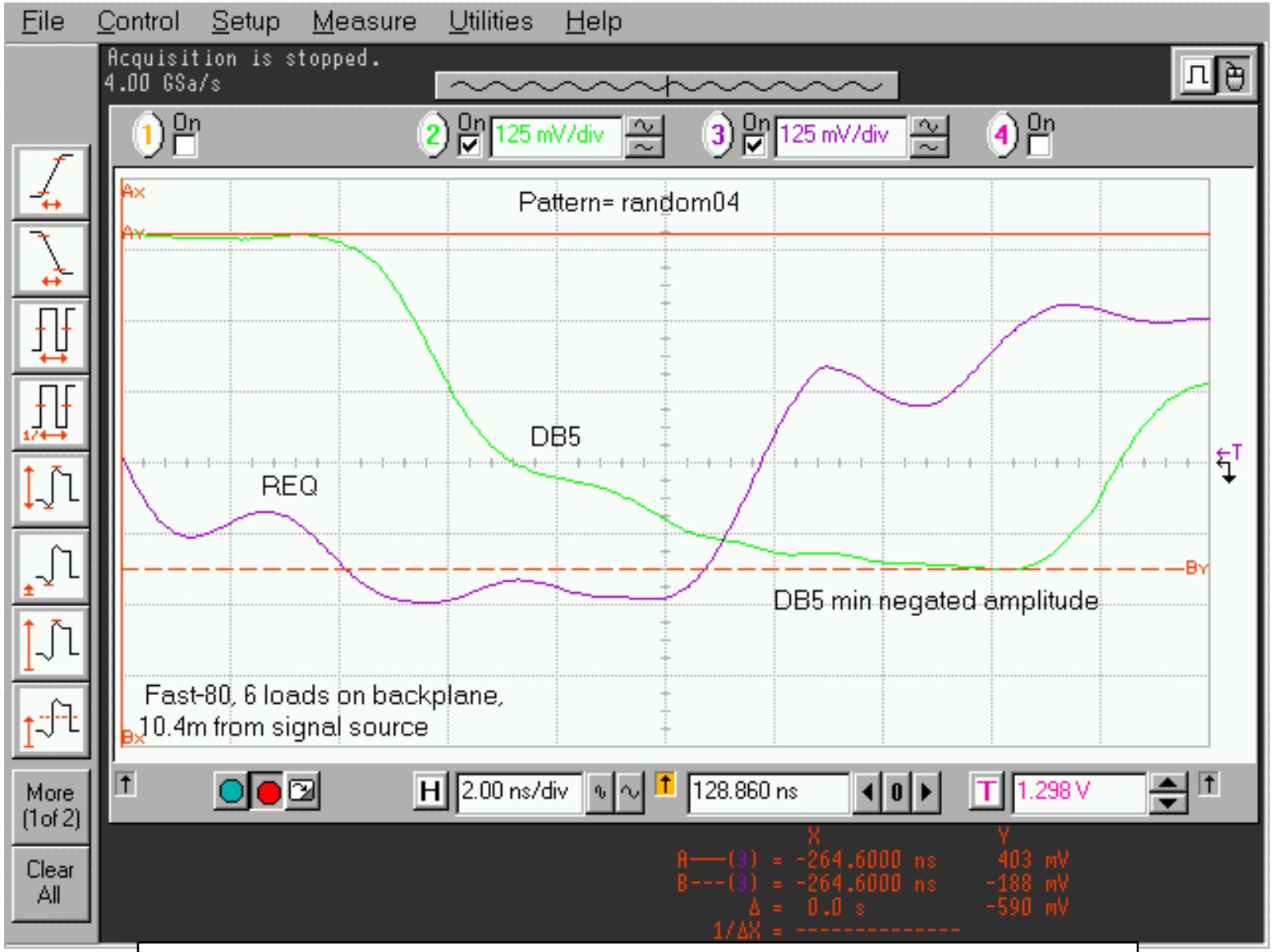


One following eight zeros.



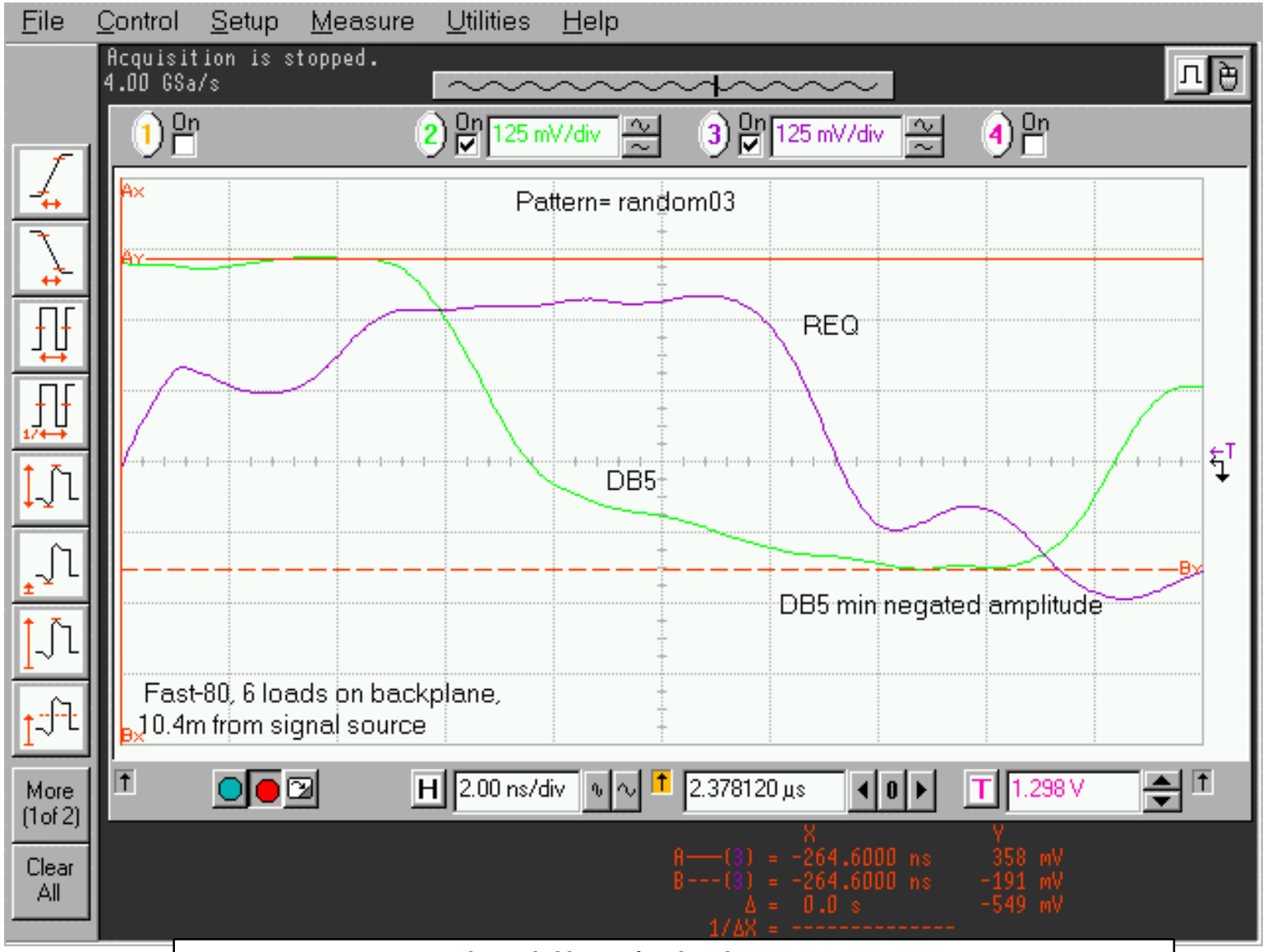
One following eight zeros.

Amplitude 198mv
Negation period 12.0ns
Setup time 6.0ns
Hold time 6.0ns



Shortest setup time of random-data measurements

Amplitude -188mv
Negation period 10.9 ns
Setup time 4.6ns
Hold time 6.3ns



Shortest hold time of random-data measurements

Amplitude -191mv
Negation period 10.9ns
Setup time 5.8ns
Hold time 5.1ns