

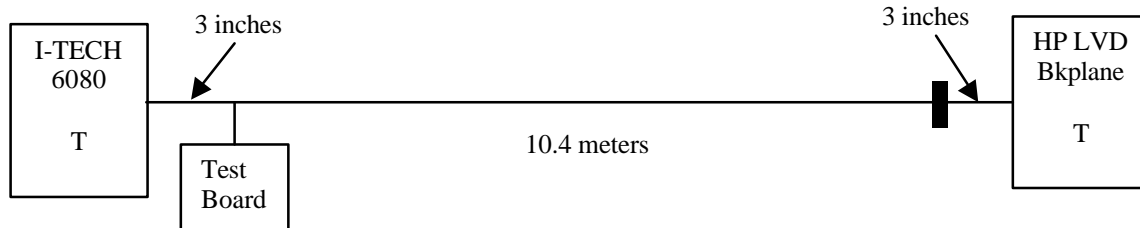
Fast-80 Case Study – One Bit Across a 6-device Backplane

Objective: Evaluate one bit in a fixed data pattern on an LVD backplane, under different load conditions and at different locations on the backplane.

This is intended to establish a baseline against which random and worst case ISI patterns can be evaluated in subsequent studies.

Physical

Configuration: This was a “simulated host” configuration with the target test board only 3” from the ITECH initiator. The 6-device backplane was connected on the other side of the target test board through a 10.4m shielded cable and a 3” ribbon cable (for physical compatibility). The REQ and data signals should appear at the backplane with essentially the same characteristics as ACK and data in a real system.



Device Loads: PCBs from QuantumViking II LVD SCSI drives were plugged into slots in the backplane and power was applied. The nominal node capacitance of the Viking II is 15pf.

Transfer Rate: All measurements were made while executing a 512 byte READ BUFFER command with Fast-80 double transition transfers enabled on the test board. The buffer was loaded originally in Fast-40 mode from the I-TECH 6080.

Data Pattern: The buffer pattern used was a repeating sequence of 0x0000FFFF. On a wide bus this generates an alternating 01010.... pattern on each individual data bit.

Test Equipment: HP 1.5 GHz scope with Tektronix 1GHz differential probes

Cables: SPI-2 compliant round and ribbon cable for LVD.

*****See T10/98-192r0 for detailed specs of test equipment and cable plant.

Measurement Description

The following data was gathered, using multiple transfers of the same data pattern. Data bit 5 was used for the measurements. This was an arbitrary choice. All bits except the parity bits switched each bit time, so crosstalk is a major consideration while ISI should not be an issue.

1. Trace captures of a single 'one bit' and a single 'zero bit', showing REQ and DB5 with a single device installed, at each of the 6 slots of the backplane.

On previous measurements it was shown that a single data bit exhibits considerable variation in amplitude and timing across a large block transfer, even with a stable data pattern. However, the variation in the same bit at the same offset on many repetitions of the pattern is more stable. E.g., DB5 may vary by +/-5% across a 512 byte transfer, but the 10th bit in one transfer will be very close to the 10th bit in all others, as long as the same physical configuration is maintained. The reasons for this are complex and are still under investigation.

To minimize uncontrolled variation, DB5 in the 9th and 10th words transferred was selected for measurement. This is the 5th zero and the fifth one clocked on the DB5 line. The selection was arbitrary and these transitions seemed reasonably representative.

2. One configuration was measured with 2 loads installed; loads were in slots 1 and 6.
3. Three configurations were measured with 3 devices installed.
4. Three configurations were measured with 4 devices installed.
5. Four configurations were measured with 5 devices installed.
6. Traces were taken at all 6 slots with 6 devices installed.

Results are shown on the following 2 pages in table form. Representative traces with 6 loads are attached.

Captured .bmp files of all traces are available to anyone who wants to study them.

Summary of Measurement Results

Case 1: A single load moved through all six slots. Measurements were taken at the connector of the PCB supplying the load.

| Slot Number | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|-------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1 | 294 | 12.7 | -317 | 12.2 |
| 2 | 283 | 12.7 | -306 | 12.0 |
| 3 | 278 | 12.9 | -300 | 12.0 |
| 4 | 267 | 12.9 | -300 | 12.2 |
| 5 | 278 | 12.8 | -289 | 12.2 |
| 6 | 261 | 12.9 | -289 | 12.4 |

Observation: Individual assertion/negation pairs don't necessarily add to exactly 25.0ns with this configuration and data pattern, although the average over even a few bits is exactly 25.0. Slot 2 had the worst deviation in this case, 24.7ns.

Case 2: Loads installed in slots 1 & 6. Measurements were taken at the connector of the PCB in slot 1.

| Slot Number | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|-------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1 | 283 | 12.7 | -294 | 12.0 |

Case 3: Loads installed in 3 slots. Measurements were taken at the connector of the PCB in slot 1.

| Slot Numbers | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|--------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1, 2, 6 | 288 | 12.7 | -317 | 12.0 |
| 1, 2, 3 | 275 | 12.7 | -306 | 12.0 |
| 1, 5, 6 | 272 | 12.8 | -269 | 12.2 |

Case 4: Loads installed in 4 slots. Measurements were taken at the connector of the PCB in slot 1.

| Slot Numbers Loaded | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|---------------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1, 2, 3, 6 | 261 | 12.7 | -291 | 12.0 |
| 1, 4, 5, 6 | 255 | 12.8 | -272 | 11.9 |

Case 5: Loads installed in 5 slots. Measurements were taken at the connector of the PCB in slot 1 except for the last configuration where slot 1 wasn't populated.

| Slot Numbers Loaded | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|---------------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1, 2, 3, 4, 6 | 255 | 12.9 | -253 | 11.8 |
| 1, 2, 3, 4, 5 | 261 | 12.7 | -261 | 12.0 |
| 1, 3, 4, 5, 6 | 255 | 12.8 | -236 | 11.9 |
| 2, 3, 4, 5, 6 | 272 | 12.8 | -261 | 12.2 |

Case 6: Loads installed in 6 slots. Measurements were taken at the connector of the PCB in each slot.

| Measured at Slot Number | Amplitude of 'one' (mv) | Assertion Period (ns) | Amplitude of 'zero' (mv) | Negation Period (ns) |
|-------------------------|-------------------------|-----------------------|--------------------------|----------------------|
| 1 | 255 | 12.9 | -247 | 12.0 |
| 2 | 266 | 12.6 | -236 | 12.2 |
| 3 | 255 | 12.8 | -261 | 12.0 |
| 4 | 252 | 12.6 | -275 | 12.3 |
| 5 | 238 | 12.7 | -269 | 12.2 |
| 6 | 244 | 12.6 | -266 | 12.2 |

