Richard Uber
Duncan Penman
June 18, 1998

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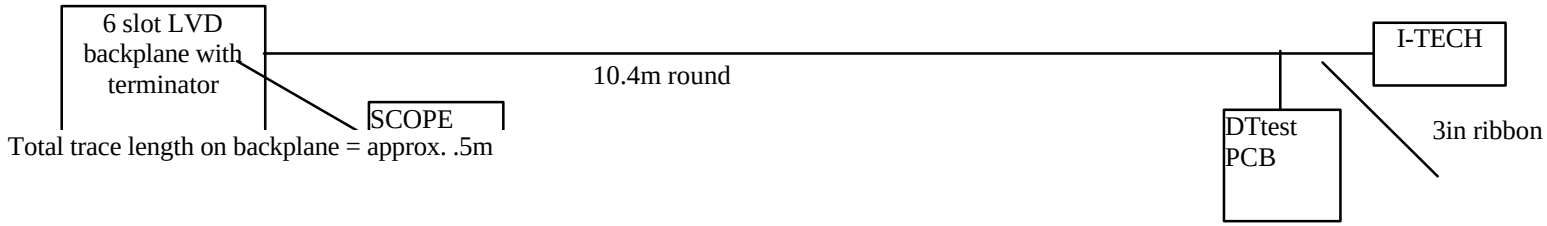
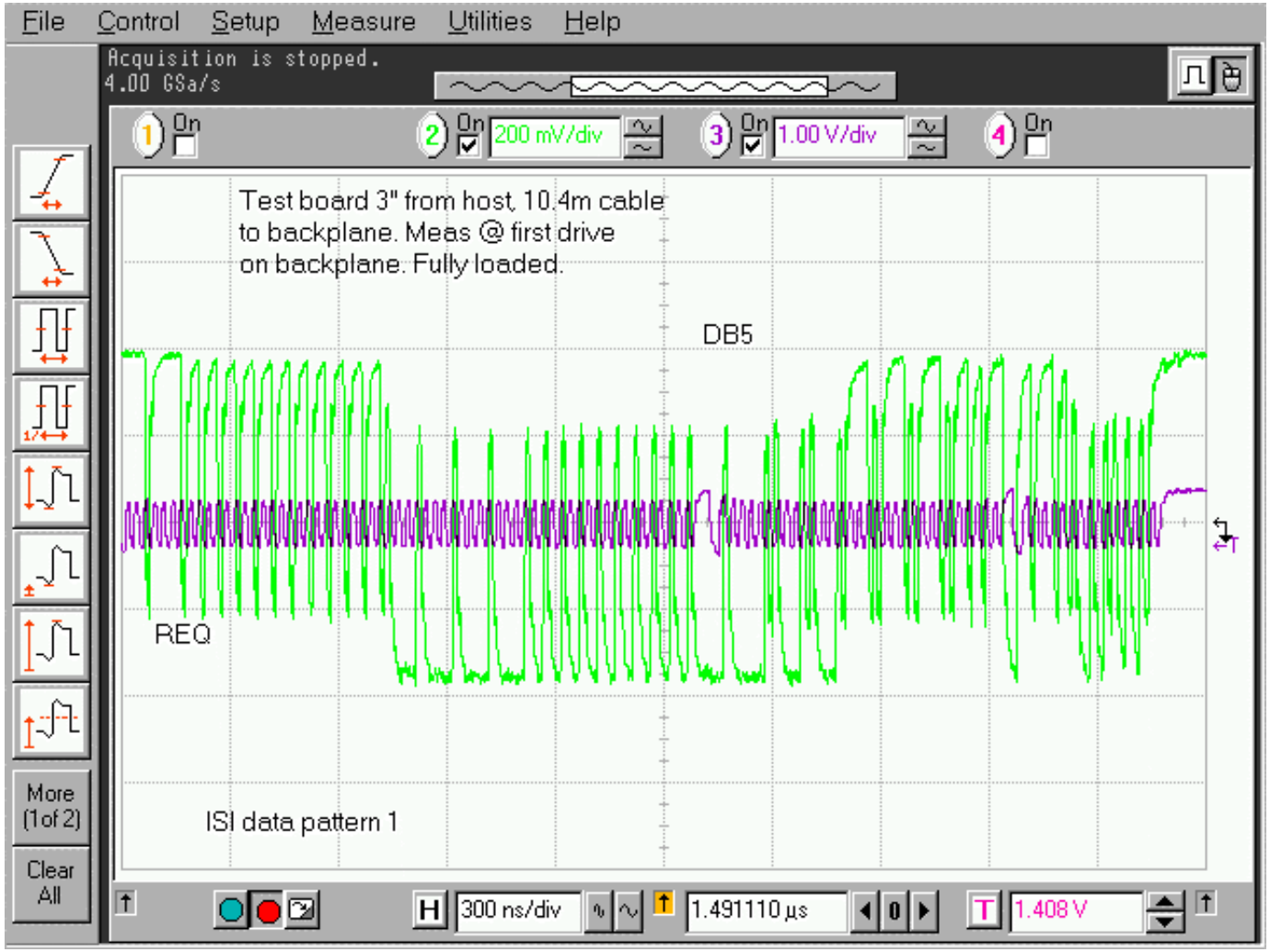
Fast-80 Simulated Host Waveforms
10.4 Meters from Driver to 6 Device LVD Backplane



Test Description: Setup – Drove REQ and data from a point very near the host. Observed waveforms 10.4m away on a loaded 6 device backplane. This was intended to simulate ACK and data as it would be seen by a backplane 10.4m away from a host adapter.
Data captured - REQ and DB5
Data was observed with TEK P6246 differential probes

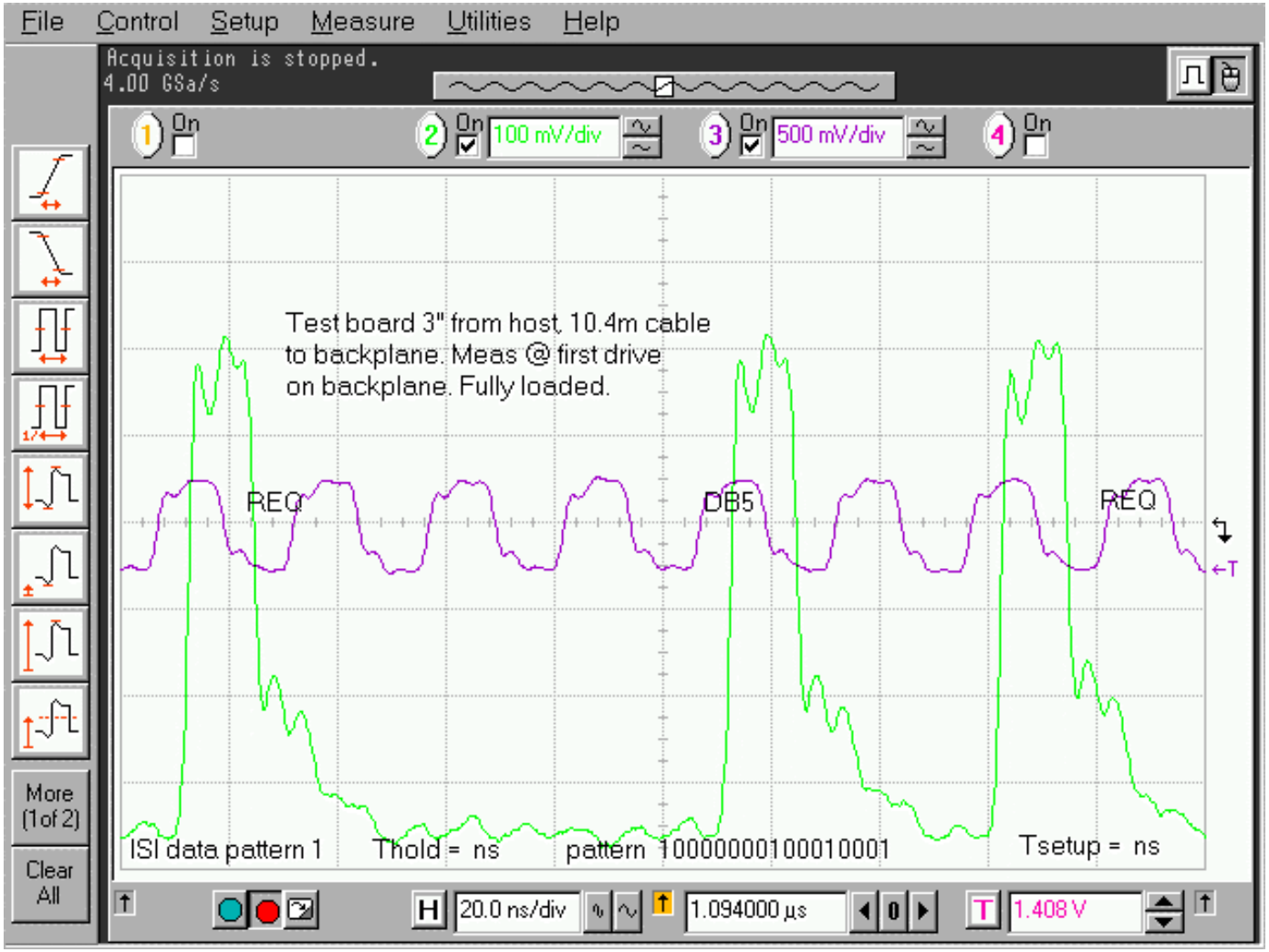
Notes:

1. The first 3 slides show overall waveforms, illustrating data dependent amplitude variations. These are followed by 5 slides showing setup and hold times for different potential ISI data sequences.
2. The most interesting observation in this set is slide 5A where a data transition from one to zero shows enough ringing to recross the threshold before achieving a good level. There was enough setup time on this bit to still be detected correctly but we could undoubtedly find worse conditions if we looked longer.

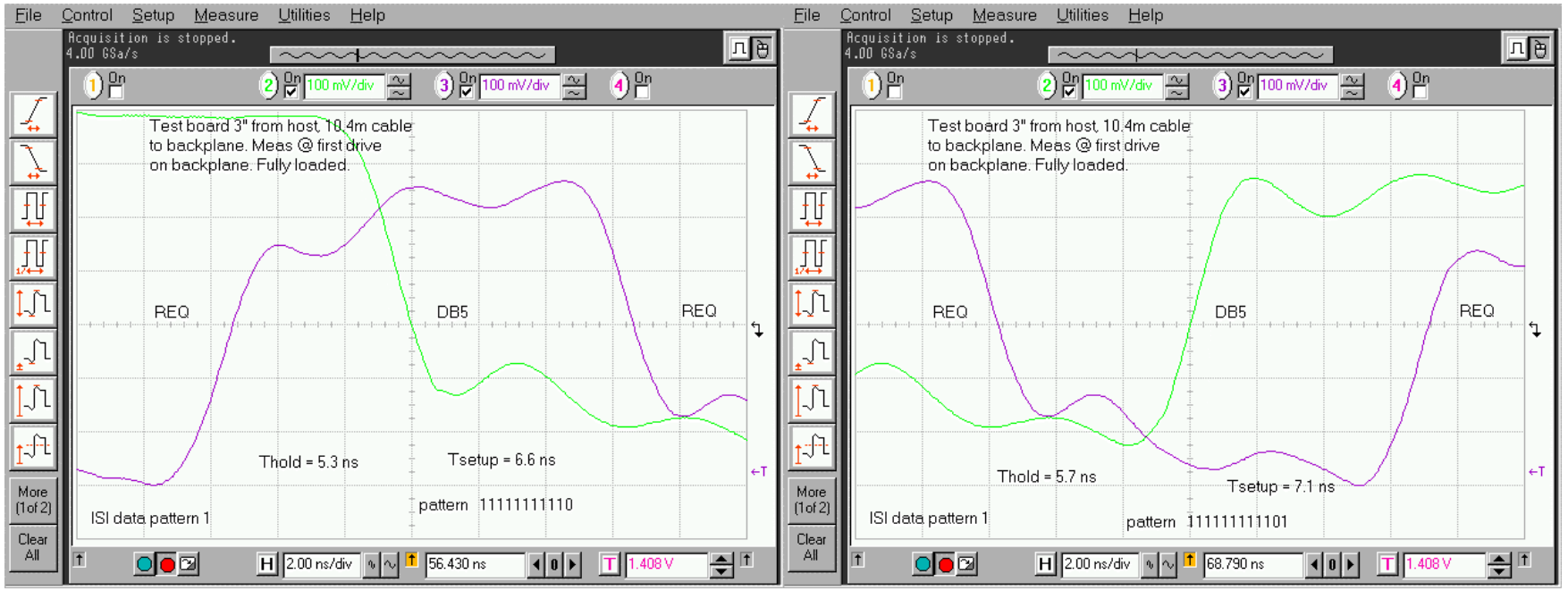


Slide 1: Overall waveform of 512 byte burst showing envelope of data bit 5. This data pattern was generated to emphasize data dependent amplitude variations. REQ is shown at 1.0 volt/div in order to more clearly see the data bit.

Slide 2: A region of slide 1 blown up to show an 18 bit sequence heavily dominated by ones. Note that DB5 is shown at 100 mv/div and REQ is shown at 500 mv/div.

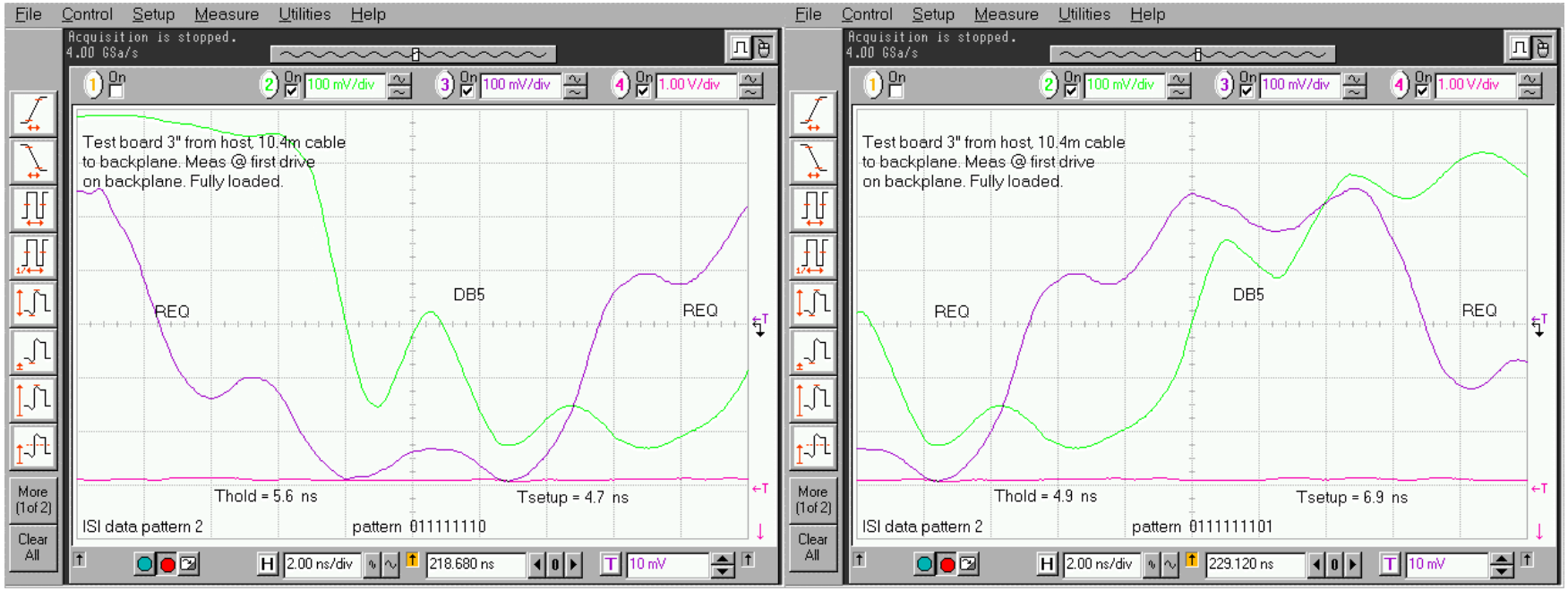


Slide 3: A region of slide 1 blown up to show a 17 bit sequence heavily dominated by zeroes. Note that DB5 is shown at 100 mv/div and REQ is shown at 500 mv/div.



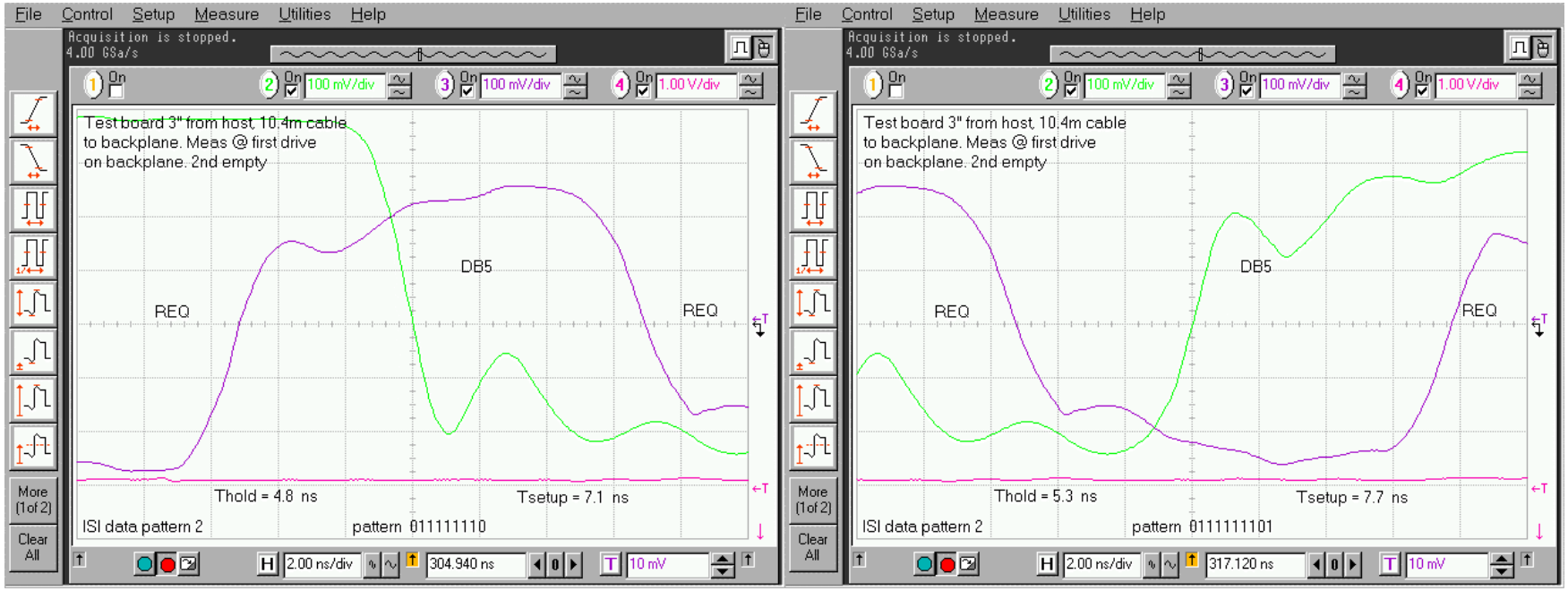
Slides 4A and 4B: Leading and trailing edge of a single zero following a run of ones. Data clocked on negative going edge of REQ.

Hold time for previous bit	5.3ns
Setup time for this bit	6.6ns
Hold time for this bit	5.7ns
Setup time for next bit	7.1ns



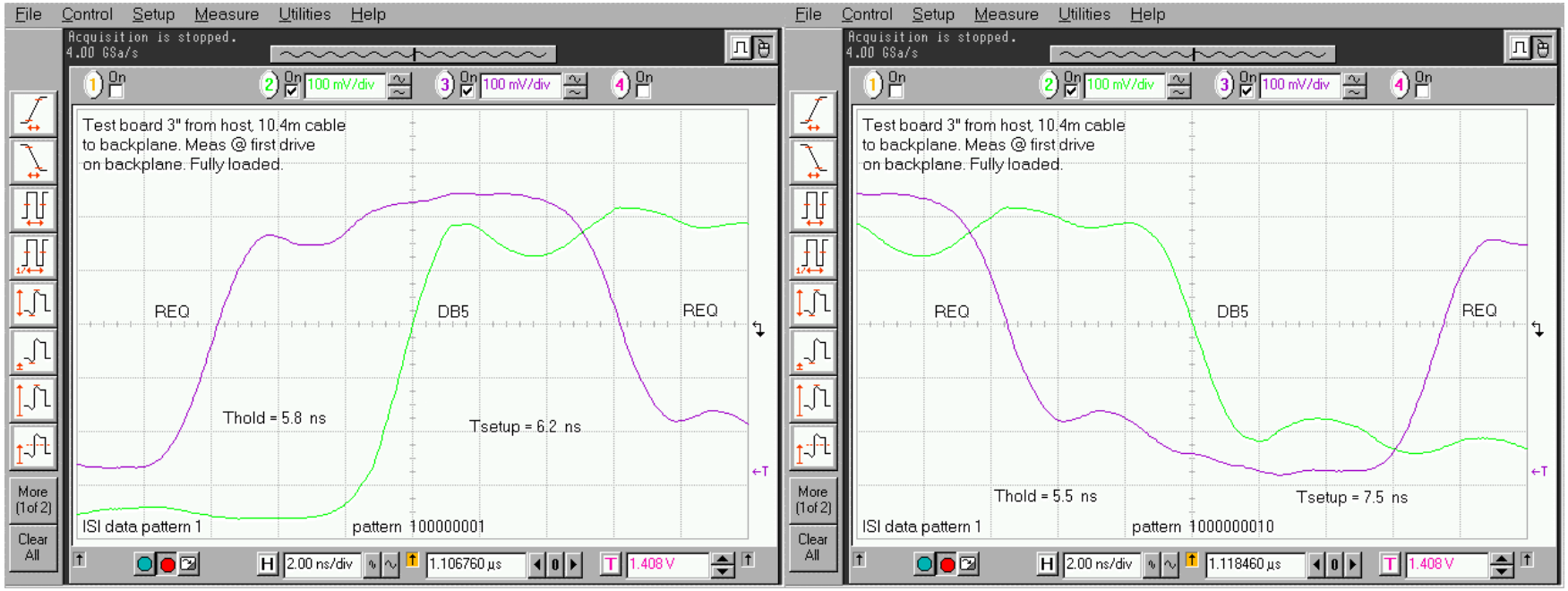
Slides 5A and 5B: Leading and trailing edge of a single zero following a run of ones. Data clocked on positive going edge of REQ. Note the apparent reflection that recrosses the baseline. Typical level of backplane reflection is shown on slide 4A. This excursion seems to depend on the data pattern of other bits. The coupling mechanism has not yet been determined.

Hold time for previous bit	5.6ns
Setup time for this bit	4.7ns
Hold time for this bit	4.9ns
Setup time for next bit	6.9ns



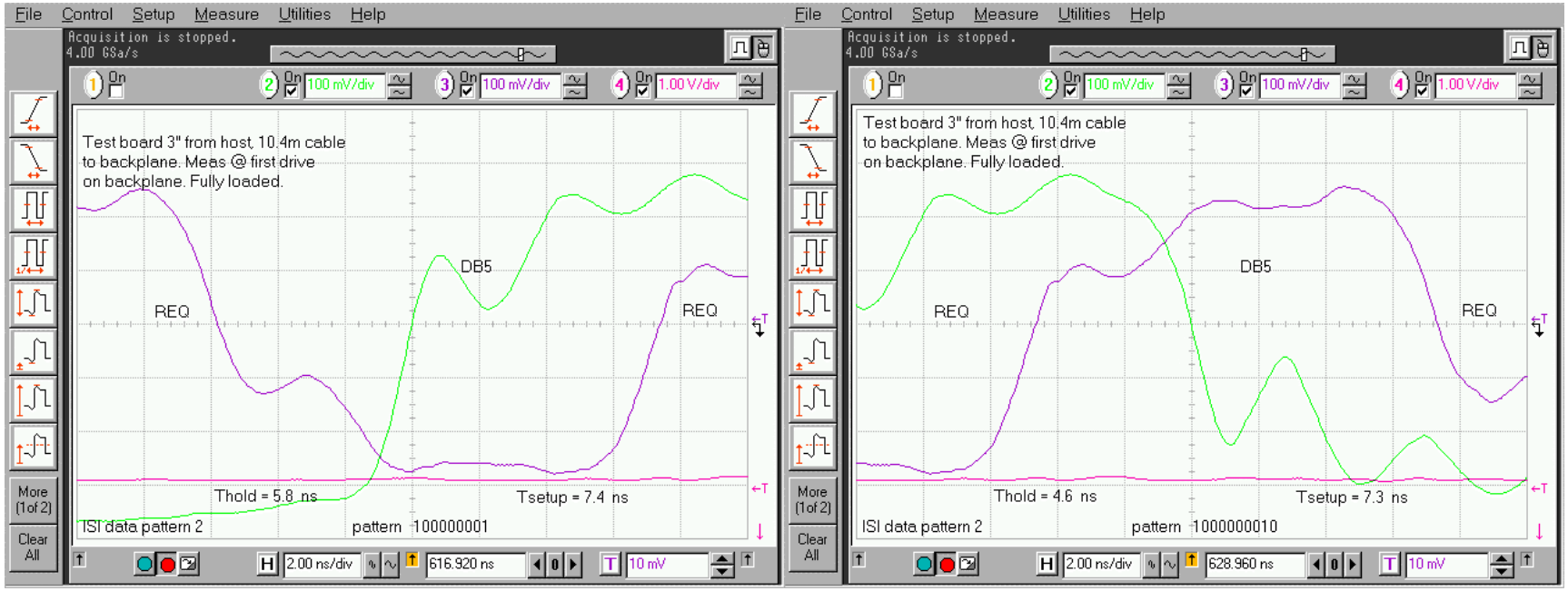
Slides 6A and 6B: A third case of a single zero following a long run of ones. Data clocked on negative going edge of REQ.

Hold time for previous bit	4.8ns
Setup time for this bit	7.1ns
Hold time for this bit	5.3ns
Setup time for next bit	7.7ns



Slides 7A and 7B: Leading and trailing edge of a single zero following a run of ones. Data clocked on negative going edge of REQ.

Hold time for previous bit	5.8ns
Setup time for this bit	6.2ns
Hold time for this bit	5.5ns
Setup time for next bit	7.5ns



Slides 8A and 8B: Leading and trailing edge of a single zero following a run of ones. Data clocked on positive going edge of REQ.

Hold time for previous bit	5.8ns
Setup time for this bit	7.4ns
Hold time for this bit	4.6ns
Setup time for next bit	7.3ns