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Experimental Results on Fast-80 SCSI Signals

This document and the three that follow are the result of work done at Quantum Corporation in Milpitas over the past two weeks. While many questions remain unanswered, we hope that presenting the data now will help the SPI-3 working group decide where attention needs to be focussed, and may also relieve some anxiety about some worst case scenarios.

Contents of this document:

- Test Equipment used
- Cable and termination description
- DC signal levels from the test chip
- Asserted/negated duty cycle measurements
- 16 setup/hold time measurements representing the combinations of data = 0/1, clocking on the rising/falling edge of REQ, and data width of 1_bit_time/>1_bit_time.
- Setup/hold time summary
- 2 traces of signal reflections

The three remaining documents cover specific configurations of interest:

1. A 6 device LVD backplane >10m from the host.
2. A 25m point-to-point connection.
3. Analysis of ISI effects on an LVD backplane 25m from the signal source.

Environment

Scope used: HP Infinium, 1.5GHz, 8 Gs

Capture resolution used: 4 Gs/sec

Probes: HP 1152A 2.5Ghz Active probes with 0.6 pF nominal input capacitance

TEK 6246 400Mhz differential probes with input capacitance < 1pf

Signal source: Quantum DTtest board with 68 pin connector

Host attachment: I-TECH 6080D SCSI tester, using a Symbios 53C985 host adapter chip.

Cable Specifications

Round: Madison, spec #13162 LVD Fast-40 Cable, 34 twisted pairs

Diff. Impedance: 123 ohms, +/- 10 ohms

Mutual Capacitance: 11 pF/ft nominal

Propagation Delay: 1.44 nsec/ft nominal

Conductor: 30AWG tin plated copper (except lengths > 12 meters@28AWG)

Conductor DC resistance: 0.108 ohms/ft maximum

Ribbon: Tempflex Teflon

Single ended impedance: 90 ohms +/- 6 ohms

Diff. Impedance: 130 ohms +/- 10 ohms

Single ended capacitance: 14.7 pF/ft

Diff. Capacitance: 10.0 pF/ft

Single ended inductance: 0.12 uH/ft

Diff. Inductance: 0.17 uH/ft

Propagation delay: 1.31 nsec/ft

Termination

On cable: DataMate(Method) DM1175 – a small (approx. 1"x2") PCB featuring a couple of voltage regulators and a lot of precision thin film resistors deposited on the board.

On host: Unitrode UCC5630

D.C. Levels for DTtest test chip, sample size = 1

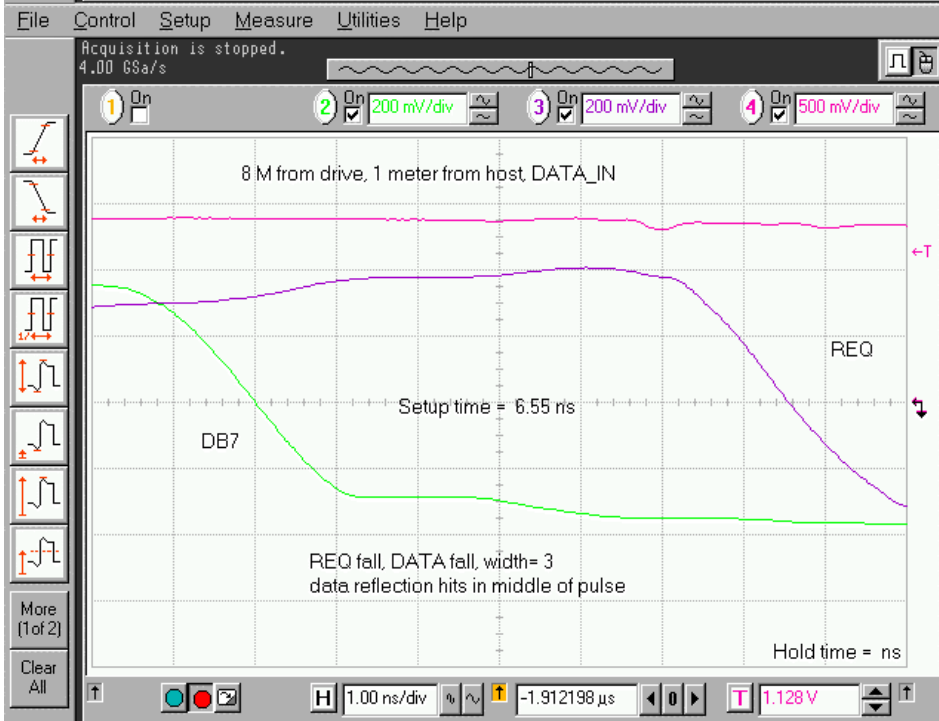
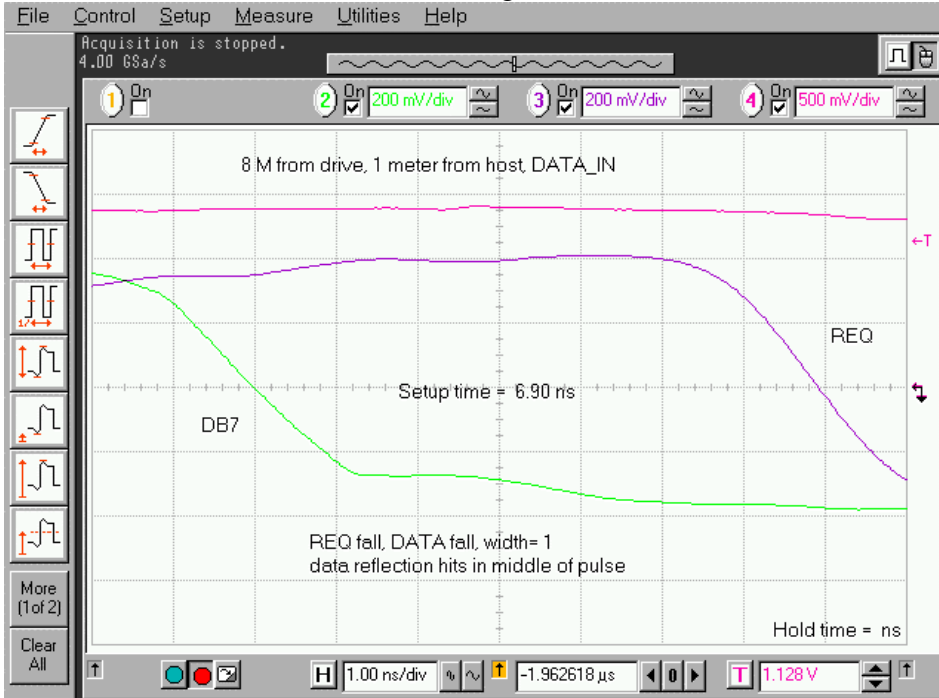
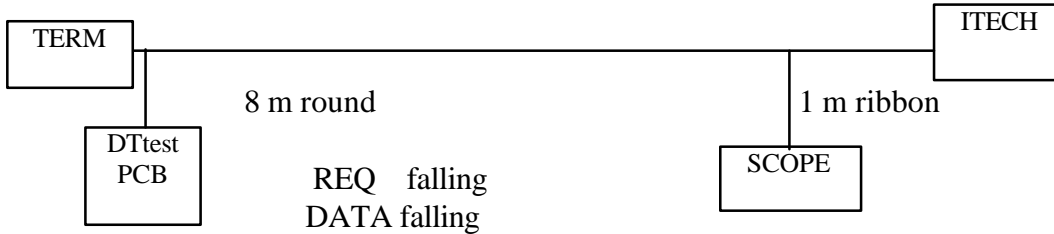
	Float	Assert	Negate	Imbalance	Swing
12	-117	448	-432	16	880
13	-118	449	-425	24	874
14	-118	452	-425	27	877
15	-118	447	-413	34	860
P1	-118	447	-388	59	835
0	-118	439	-422	17	861
1	-117	433	-416	17	849
2	-118	429	-417	12	846
3	-118	433	-413	20	846
4	-117	439	-405	34	844
5	-117	439	-400	39	839
6	-117	437	-395	42	832
7	-118	441	-395	46	836
P0	-117	473	-410	63	883
REQ	-117	461	-391	70	852
8	-117	459	-411	48	870
9	-117	458	-413	45	871
10	-117	454	-408	46	862
11	-117	454	-414	40	868
sum	-2231	8492	-7793	699	16285
average	-117.421	446.9474	-410.158	36.78947	857.1053
standard Deviation	0.507257	11.32585	12.08885	16.79146	16.33638

DT Signal Duty Cycle

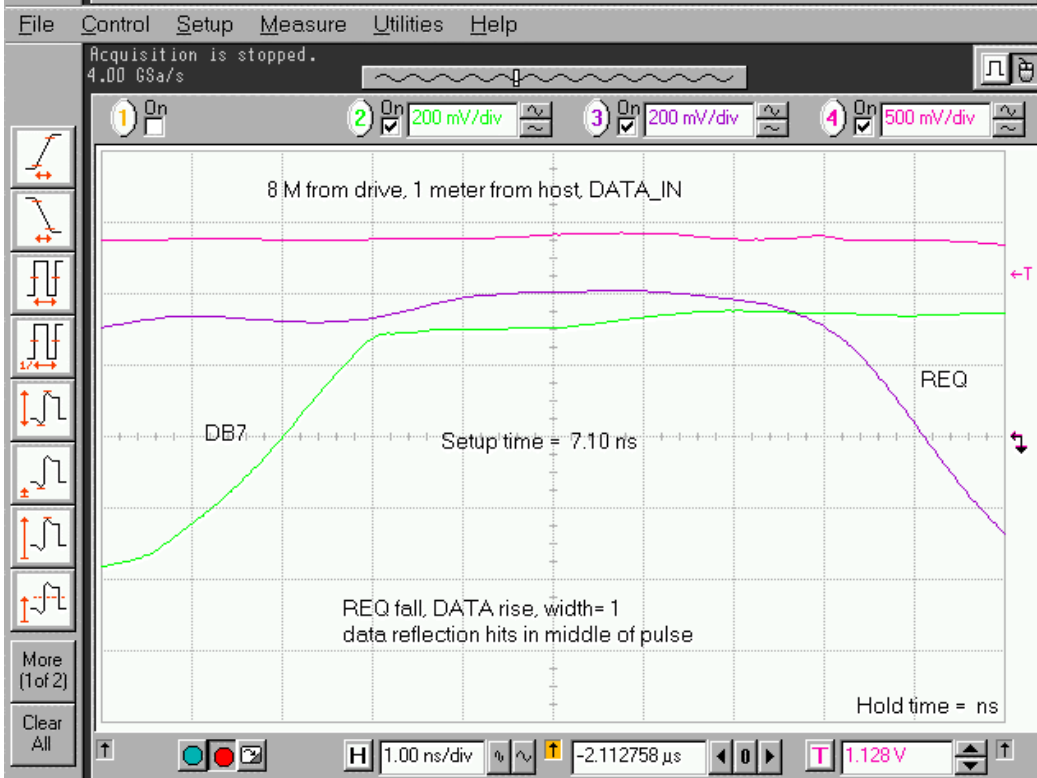
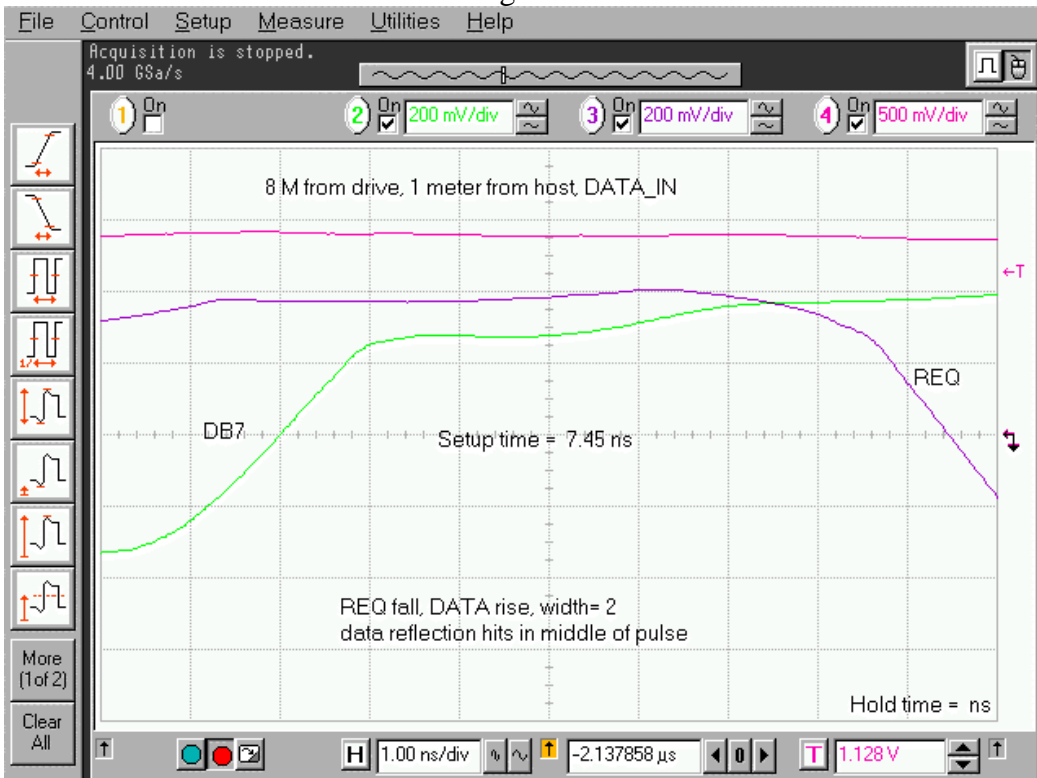
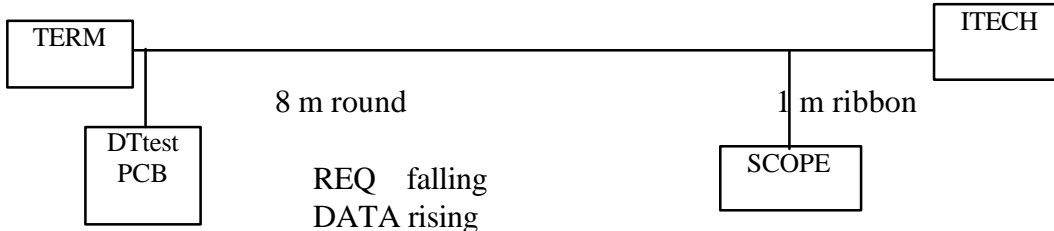
Pin	Asserted PW (ns)
12	12.9
13	12.8
14	12.8
15	13.0
P1	12.8
0	12.9
1	12.9
2	12.9
3	13.0
4	12.9
5	12.8
6	12.9
7	13.0
P0	12.8
REQ	13.0
8	12.8
9	12.9
10	12.8
11	12.9

The driver circuitry used in the DTtest chip is a 'hybrid driver', with 2 independent current sources. One is used for cancelling the terminator bias during data phases, and the other is used to symmetrically drive the data pattern.

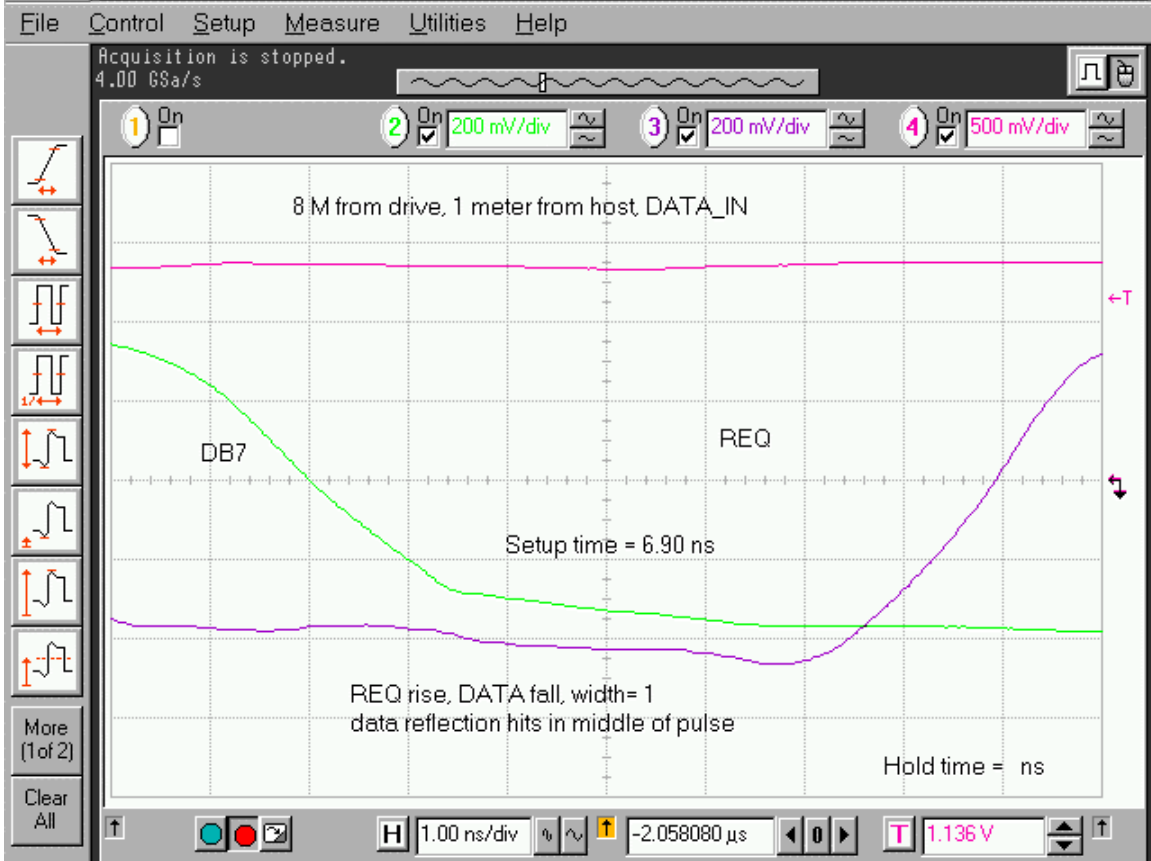
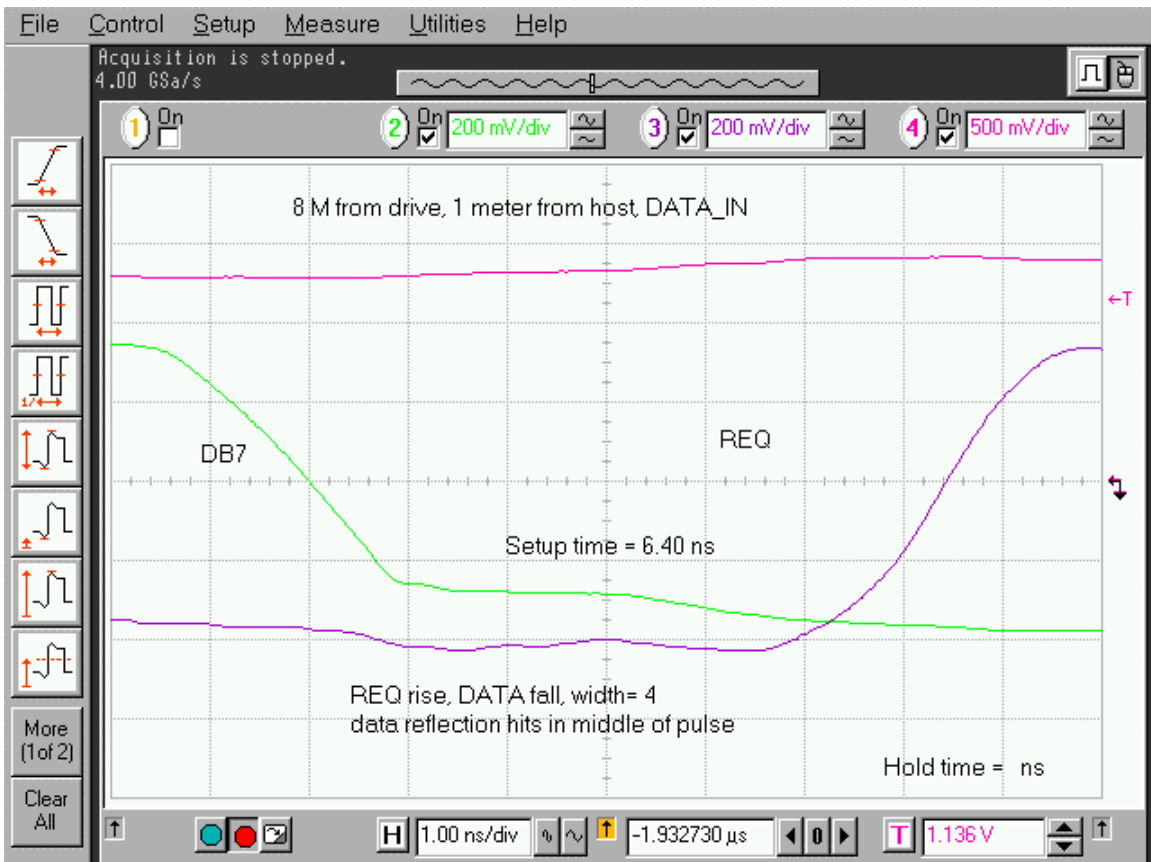
While it is possible to adjust the bias cancellation current reference to better balance the assertion and negation levels, as well as the duty cycle, we chose to not do so in order to keep all data presented here consistent.



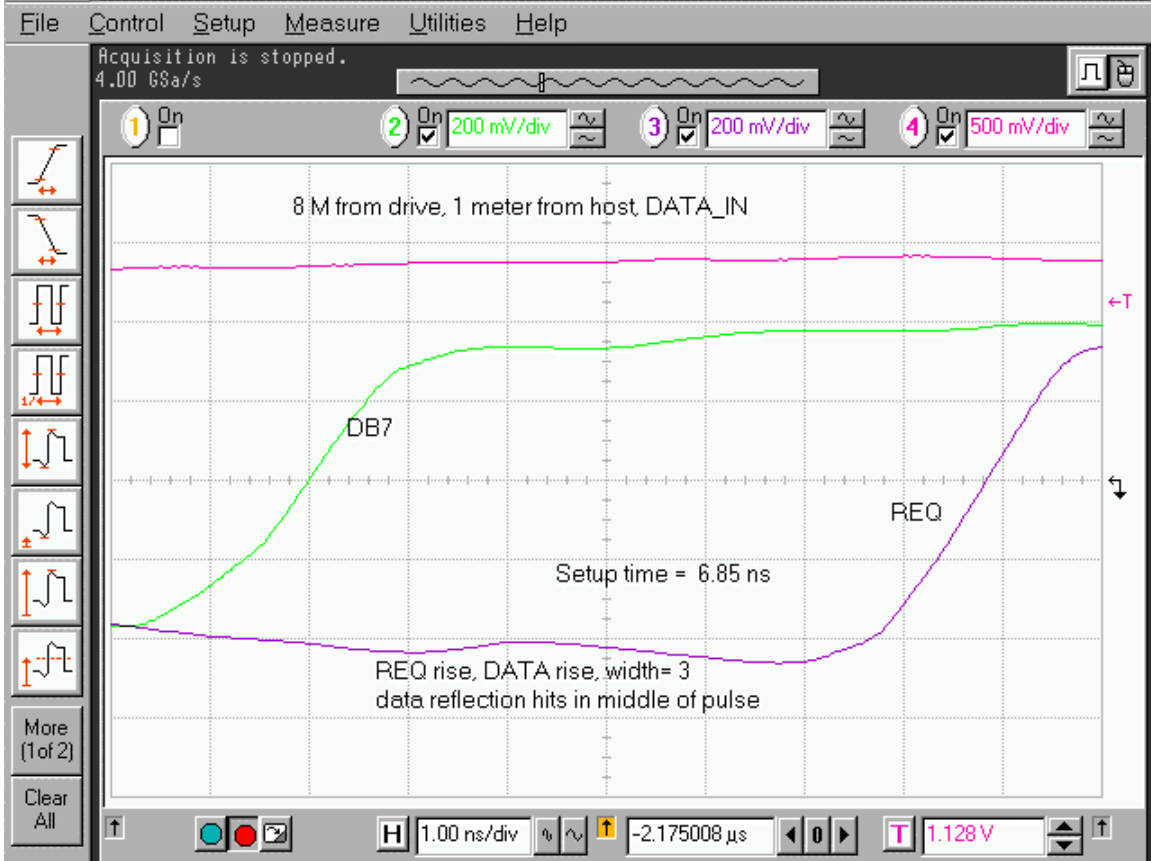
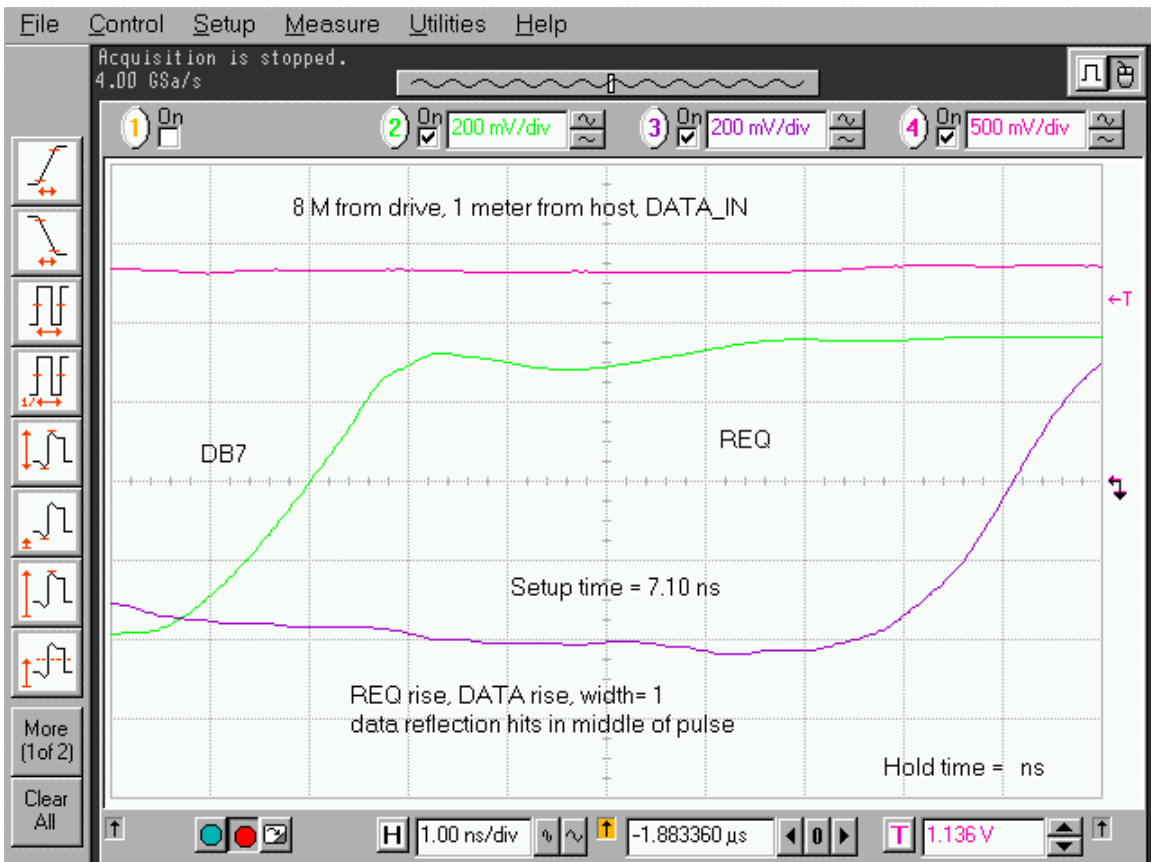
REQ fall
DATA fall



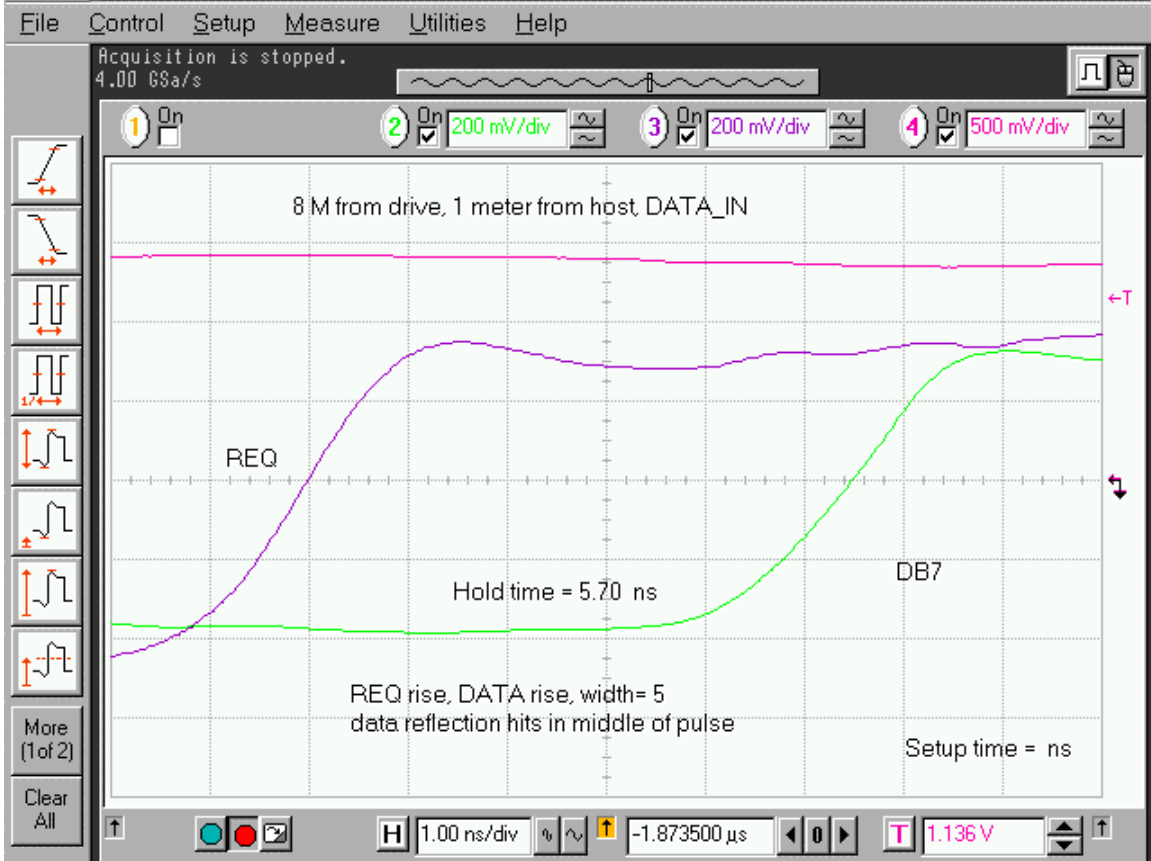
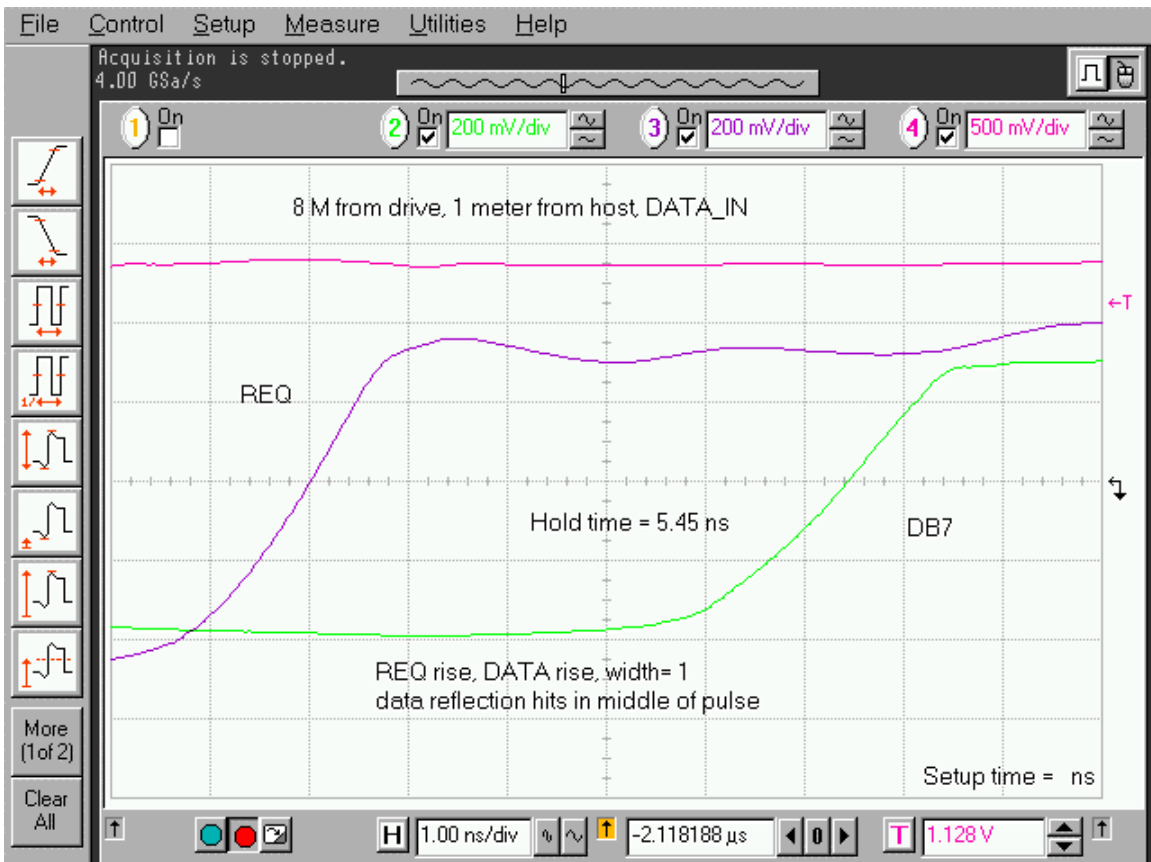
REQ fall
DATA rise



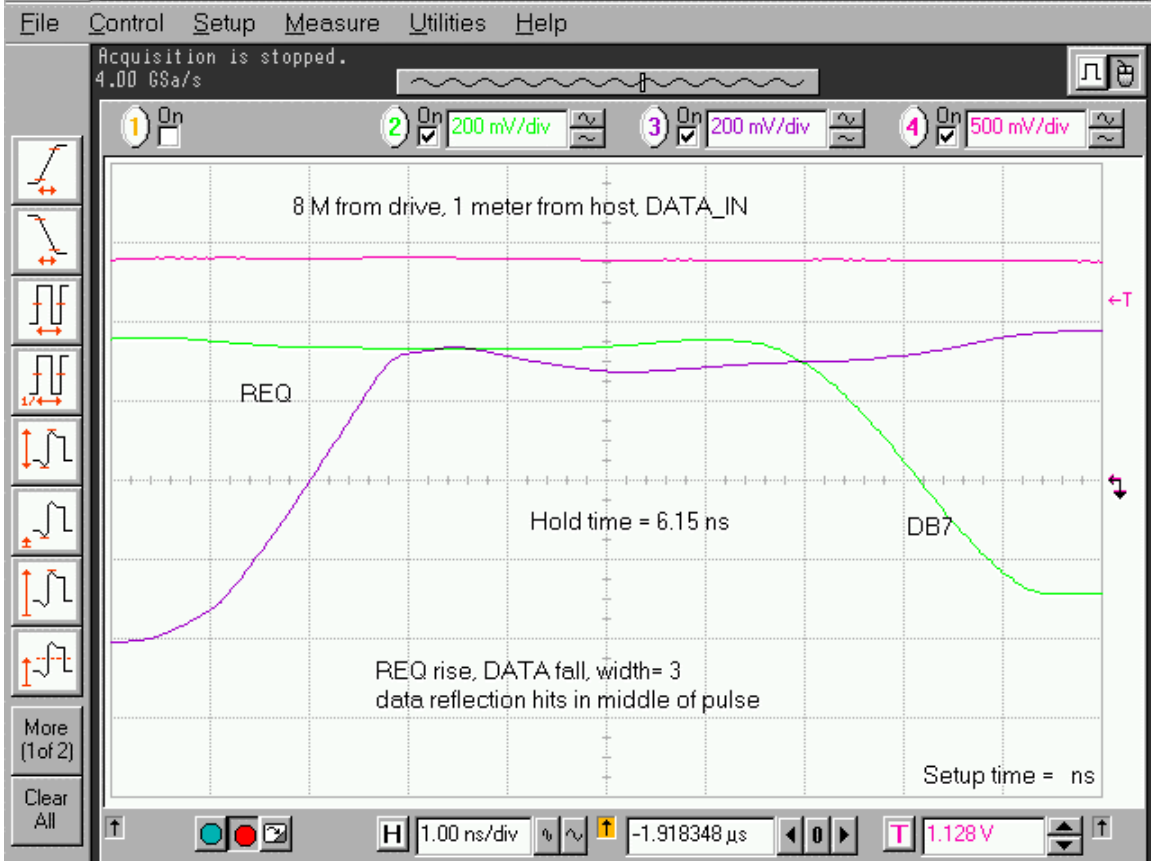
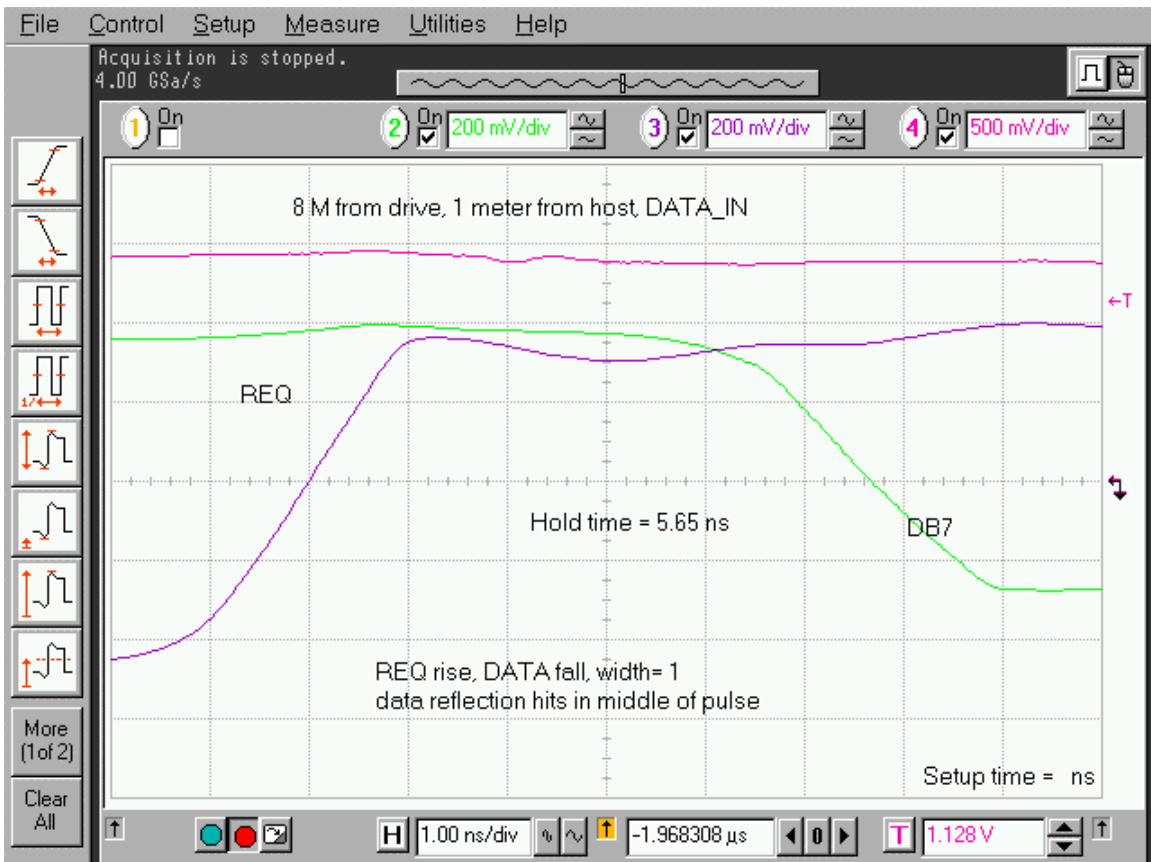
REQ rise
Data fall



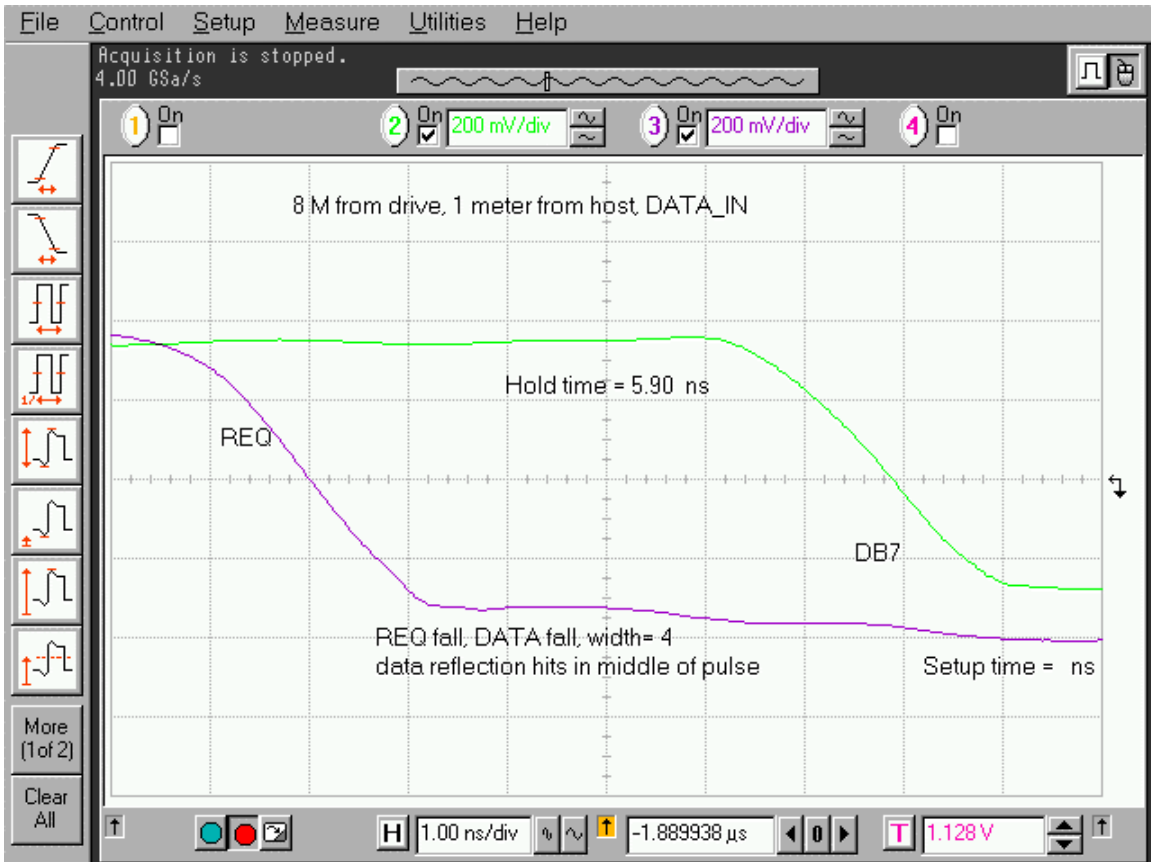
REQ rise
Data rise



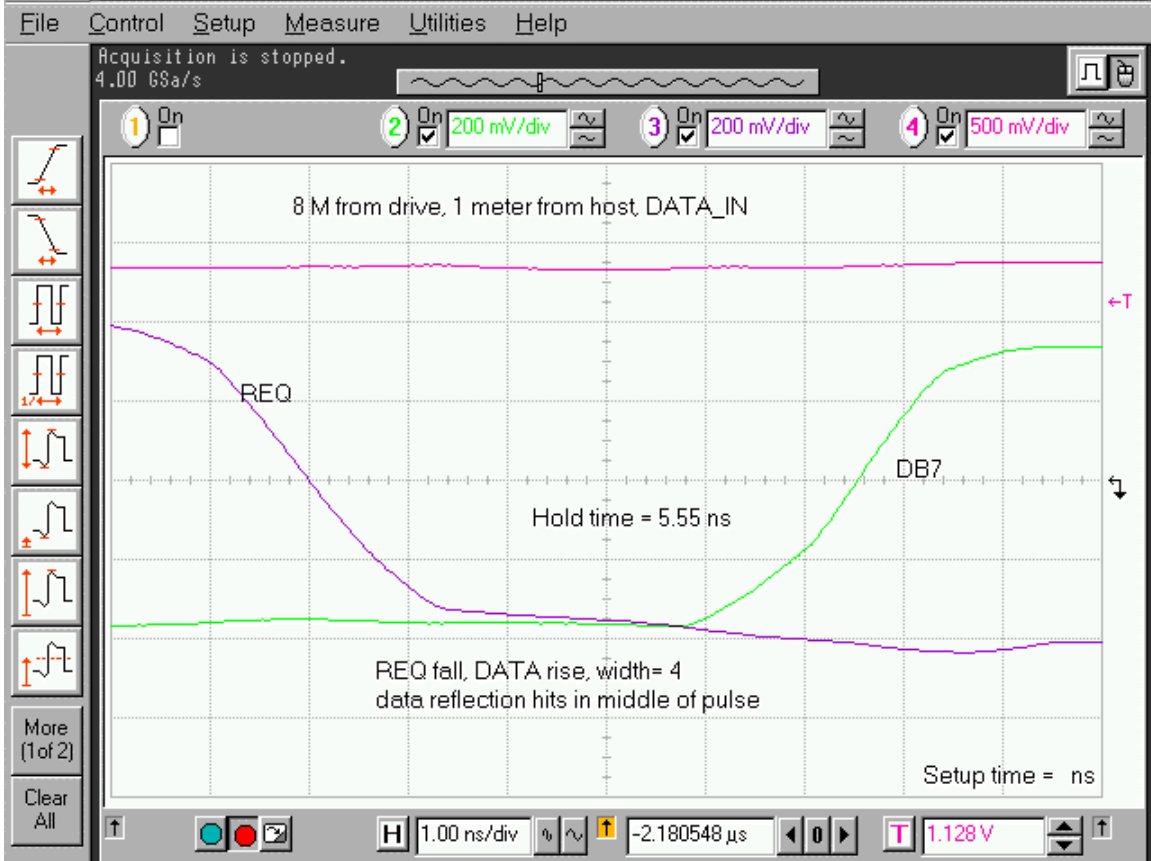
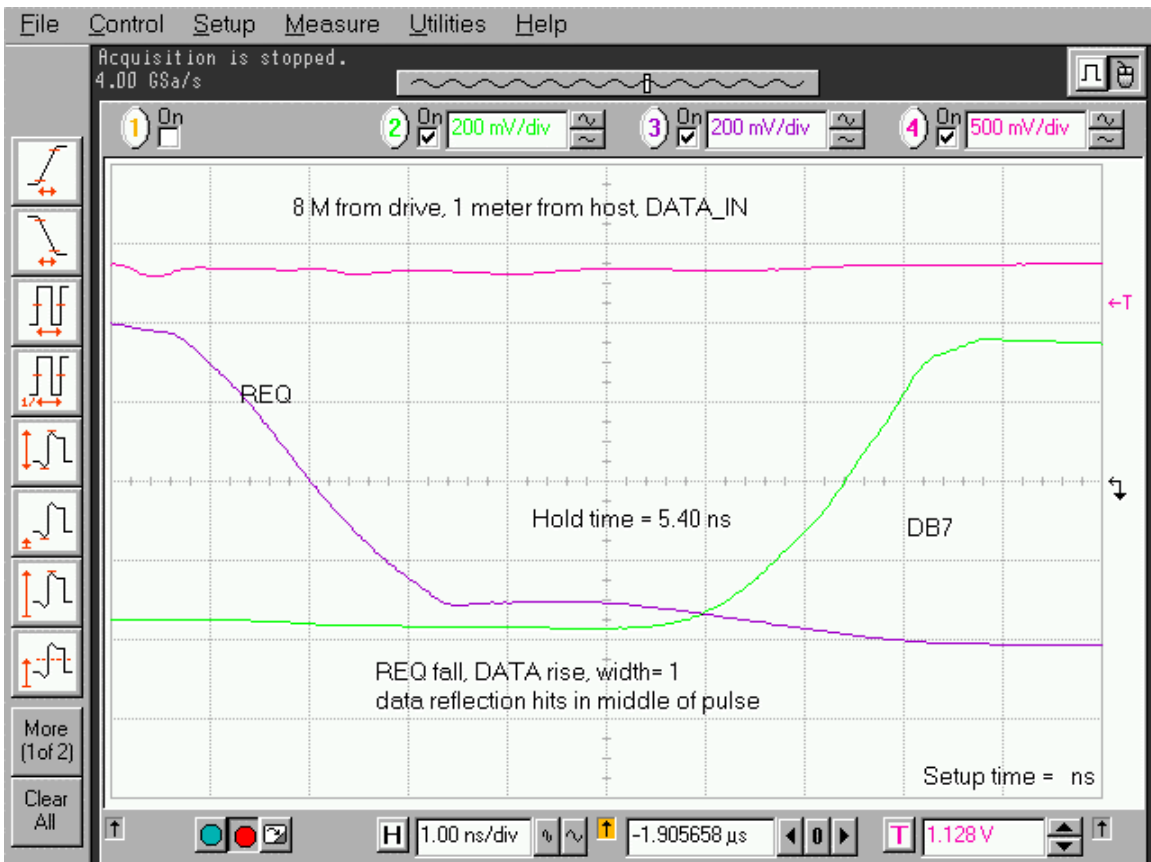
Hold
REQ rise
Data rise



Hold
REQ rise
Data fall



Hold
REQ fall
Data fall



Hold
REQ fall
Data rise

Setup / Hold time summary:

REQ	DATA	width	Setup	width	Setup	width	Hold	width	Hold
RISE	RISE	1	7.1	3	6.85	1	5.45	5	5.70
RISE	FALL	1	6.9	4	6.4	1	5.65	3	6.15
FALL	RISE	1	7.1	2	7.45	1	5.4	4	5.55
FALL	FALL	1	6.9	3	6.55	1	5.4	4	5.9

	Setup Time W=1 penalty	Hold Time W=1 penalty
RISE RISE	+ .25	- .25
RISE FALL	+ .50	- .50
FALL RISE	+ .35	- .15
FALL FALL	+ .35	- .50

Discussion:

Sounds like ISI, but is actually more reflections than ISI. Round trip through a little over 1 meter of cable to the ITECH and back is approximately 12.5ns, or one half cycle of the 40Mhz fundamental signal.

On width =1 pulses, the reflection from the high impedance cable (~130 ohms) and the terminator (~105 ohms) will have a peak of about 80 mV. In contrast, the signal has only dropped about 40mV due to attenuation. There is little capacitance at the measuring point since only a bare connector (about a half inch stub) and the scope probes are there.

Reflection waveforms are shown on the following page.

Key points:

- Understand the cable plant before looking at timings.
- Long cable runs (e.g. between boxes) should be targeted at the terminator impedance range of 100-110 ohms.

