• XMIT board sends Pseudo Random Pattern (run length of 7).
• Load boards are capacitive boards with 22 pf to ground from each side.
• Cable used is Hitachi Twisted Flat Series 23915
**HITACHI CABLE #23915**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor</td>
<td>30 AVG 7/38 Tinned</td>
</tr>
<tr>
<td>Insulation</td>
<td>PVC</td>
</tr>
<tr>
<td>Conductor Resistance</td>
<td>0.344 ohms/meter</td>
</tr>
<tr>
<td>Capacitance</td>
<td>48.3 pf/meter</td>
</tr>
<tr>
<td>Impedance</td>
<td>102 ohms</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>5.07 ns/meter</td>
</tr>
<tr>
<td>Skew (max)</td>
<td>0.146 ns/meter</td>
</tr>
</tbody>
</table>
Tests run with two drive levels.

Low drive level board output 250 mv

High level drive board output 575 mv peak

Measured at all load points.

Trigger point varied plus/minus 60 mv.

Will show only several representative points.
“Pseudo-random data for 12 meter twist/flat cable and 15 loads”
(trigger at center of clock)

Note: T is resistive termination
= 110 ohm
High Drive

“Eye pattern for 12 meter twist/flat cable and 15 loads”
(trigger +/- 60 mV from center of clock)

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5/19/98 Tariq/Vince - T10 Meeting
High Drive

Note: T is resistive termination = 110 ohm

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9.25 meter twist/flat (30AWG) cable
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Note: reduced drive level

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9.25 meter twist/flat (30AWG) cable

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5/20/98 Tariq/Vince - T10 Meeting
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Note: reduced drive level

W = 2.2 ns
\[\Delta: 2.6\, \text{ns}\]
\[\Omega: -2.4\, \text{ns}\]

C1 Freq
40.0408MHz

C1 Pk-Pk
364mV

C2 Pk-Pk
430mV
Low Drive

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9.25 meter twist/flat (30AWG) cable

Note: reduced drive level
Eye opening average value:

- High Drive Board: 8.36 ns
- Low Drive Board: 2.26 ns

Minimum eye opening:

- High Drive Board: 7.5 ns
- Low Drive Board: 0.0 ns
SUMMARY

• High drive level shows decent eye pattern.
• Drive level is important when reflections and ISI are present.
• More sensitive receiver would provide more margin.
• Offset balance becomes more of an issue.
• Driver level equalization determines how much of the eye is usable.
• Equalization (ISI compensation) at transmitter should improve patterns.
But in SCSI both the data and clock (REQ/ACK) are pseudo random.
MARGIN

\[
\text{margin} = \text{period} - (\text{eye closure} \times 2)
\]

Does not include RCV, cable skew and FF.
MARGIN

\[
\text{margin} = \text{period} - (\text{eye closure} \times 2)
\]

\[
\frac{\text{margin}}{2} = \frac{\text{period} - (\text{eye closure} \times 2)}{2}
\]

Example eye closure = 4.14 ns

\[
\text{margin} = 12.5 - (4.14 \times 2)
\]

\[
\frac{\text{margin}}{2} = \frac{12.5 - (4.14 \times 2)}{2}
\]

\[
\text{margin} = 2.11 \text{ ns}
\]

This 2.11 needs to cover cable skew (1.2 ns), RCV, and FF (setup or hold)

Pseudo-random mode of the clock is a big unknown.
ISSUES

ISI on both data and clock caused by NRZ data and non-regular clock.

Non-zero cancellation of the bias on the bus.

Cable skew increases with distances.

POSSIBLE SOLUTIONS

Use ISI compensation techniques to control ISI distortion on both data and clock.
Increased drive levels.
Feedback cancellation of the bias at the receiver.
Use circuit to cancel out cable skew.
Use scheme that provides a regular clock period.
Encoding of the data to decrease ISI problems.
<table>
<thead>
<tr>
<th>NAME</th>
<th>B/Sec (16 bit)</th>
<th>MHz</th>
<th>Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast40</td>
<td>80</td>
<td>40</td>
<td>Single Edge clocking / LVD with bias cancelled by asymmetric drive.</td>
</tr>
<tr>
<td>Fast80</td>
<td>160</td>
<td>40</td>
<td>Above plus / Dual Edge Clock / ISI compensation of data and Clock / higher min drive level / auto zero offset</td>
</tr>
<tr>
<td>Fast160</td>
<td>320</td>
<td>80</td>
<td>Above plus, / free running clock / auto cable deskew using training sequence.</td>
</tr>
<tr>
<td>Fast320</td>
<td>640</td>
<td>160</td>
<td>Above plus / encoding of data / reduced length.</td>
</tr>
</tbody>
</table>
**ISI COMPENSATION (Equalization)**

Being implemented in serial links today.

Can equalize either transmitter or receiver (National has receiver part, CLC014).

Lot of analysis and research available.

Easy to implement in transmitter. Can be very complex or simple.

**ISSUES**

How well would it work on NRZ data (serial links have limited frequency band due to encoding versus NRZ which from DC)?

Would a fairly simple equalization scheme be effective since we have 20 lines to deal with?
References to look at:

Transmitter Equalization for 4G b/s Signalling

Slides to go with above paper:
Interconnections with High-Speed Digital Systems conference
http://soliton.ucsd.edu/ihsds/santafe97/index.html
then: postscript file, John Poulton, UNCC, "Multi-gigabit ...
or http://soliton.ucsd.edu/ihsds/santafe97/slides/gbcmos_poulton.ps

Web site showing the test results for the above papers:

One other paper on subject (not found on a web site):

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive Minimum Edge to Edge</td>
<td>9.0</td>
</tr>
<tr>
<td>Receive Hold Time</td>
<td>1.8</td>
</tr>
<tr>
<td>Receive Setup Time</td>
<td>1.8</td>
</tr>
<tr>
<td>Receive Period Tolerance</td>
<td>0.75</td>
</tr>
<tr>
<td>Signal Timing Skew</td>
<td>3.2</td>
</tr>
<tr>
<td>System Deskew Delay</td>
<td>4</td>
</tr>
<tr>
<td>Transmit Minimum Edge to Edge</td>
<td>11.0</td>
</tr>
<tr>
<td>Transmit Hold Time</td>
<td>5.5</td>
</tr>
<tr>
<td>Transmit Setup Time</td>
<td>5.5</td>
</tr>
<tr>
<td>Transmit Period Tolerance</td>
<td>0.75</td>
</tr>
</tbody>
</table>

*These two items are called Receive Assertion Period and Transmit Assertion Period on Single edge clocking systems. These are redefined as above for dual edge systems.
Signal timing skew includes cable skew and signal distortion skew.

Distortion skew includes ISI (intersymbol interference) and signal crossing time through the receiver detection range.

Timing is done for internal transmitter and receiver only.