To: T10 Committee (SCSI)
From: George Penokie (IBM)
Subject: QAS timing
Date: 6/19/98
Below are the QAS numbers I believe will work if B wins (best case timing).

Time	A Action	Time	B Action	Time	C Action
0	Release IO,Msg,CD	0	Sees IO,Msg, CD Released	0	
		90	May assert ID	400	Sees IO,Msg, CD Released
		200	Must assert ID	490	May assert ID
				600	Must Assert ID
1000	IDs Stable access bus	1000	IDs stable across bus	1000	IDs stable across bus
1000	Sees SEL asserted	1000	Wins so must have SEL asserted		
1200	Deassert BSY 200 nsec after seeing SEL			1400	Lost so watches for SEL asserted or BSY deasserted
1400	SEL stable across bus	1400	SEL stable across bus	1400	SEL stable across bus
				1500	May deassert ID
				1600	Must have IDs deasserted
2000	IDs stable across bus	2000	IDs stable across bus	2000	IDs stable across bus
		2000	Start selection phase		

Below are the normal bus free/arbitration/selection numbers I believe will work if B wins (best case timing).

...me	A Action	Time	B Action		Time	C Action	
	Release BSY	0	Sees BSY released		0		
		400	Bus free validated		400	Sees BSY released	
					800	Bus free validated	
			BEST CASE	WORST CASE		BEST CASE	WORST CASE
		1200	Assert BSY and ID				
					1600	Assert BSY and ID	
		2200		Assert BSY and ID			
					2600		Assert BSY and ID
		3600	Examine for win				
		3600-4400	Assert SEL				
					3800	Examine for win	
					4000-5800	Sees SEL Release BSY and ID	
		4600		Examine for win			
		4600-5400		Assert SEL			
		4800-5600	Selection start		4800		Examine for win
					4800-5800		Sees SEL Release BSY and ID
		5800-6600		Selection start			

The above configuration assumes device A and B are no one end of the bus and device C is on the other end of the bus.

Below are the numbers I believe will work if C wins (worst case timing).

Time	A Action	Time	B Action	Time	C Action
0	Release IO,Msg,CD	0	Sees IO,Msg, CD Released	0	
		90	May assert ID	400	Sees IO,Msg, CD Released
		200	Must assert ID	490	May assert ID
				600	Must Assert ID
1000	IDs Stable access bus	1000	IDs stable across bus	1000	IDs stable across bus
		1000	Lost so watches for SEL asserted or BSY deasserted		
				1400	Wins so must have SEL asserted
1800	SEL stable across bus	1800	SEL stable across bus	1800	SEL stable across bus
1800	Sees SEL asserted	1900	May deassert ID		
2000	Deassert BSY 200 nsec after seeing SEL	2000	Must have IDs deasserted		
2400	IDs stable across bus	2400	IDs stable across bus	2400	IDs stable across bus
				2400	Start selection phase

The above configuration assumes device A and B are no one end of the bus and device C is on the other end of the bus.

Below are the normal bus free/arbitration/selection numbers I believe will work if C wins (best case timing).

Time	A Action	Time	B Action		Time	C Action	
	Release BSY	0	Sees BSY released		0		
		400	Bus free validated		400	Sees BSY released	
					800	Bus free validated	
			BEST CASE	WORST CASE		BEST CASE	WORST CASE
		1200	Assert BSY and ID				
					1600	Assert BSY and ID	
		2200		Assert BSY and ID			
					2600		Assert BSY and ID
		3600	Examine for win				
					3800	Examine for win	
					3800-4600	Assert SEL	
		4200-5400	Sees SEL Release BSY and ID				
		4600		Examine for win			
					4800		Examine for win
					4800-5600		Assert SEL
					5000-5800	Selection start	
		5200-6000		Sees SEL Release BSY and ID			
					6000-6800		Selection start

The above configuration assumes device A and B are no one end of the bus and device C is on the other end of the bus.

Below are the numbers I believe will work if no QAS device wants to arbitrate.

Time	A Action	Time	B Action	Time	C Action
0	Release IO,Msg,CD	0	Sees IO,Msg, CD Released	0	
				400	Sees IO,Msg, CD Released
2000	Deassert BSY				
2000	Start bus free phase				

The above configuration assumes device A and B are no one end of the bus and device C is on the other end of the bus.