T10/98-155r0

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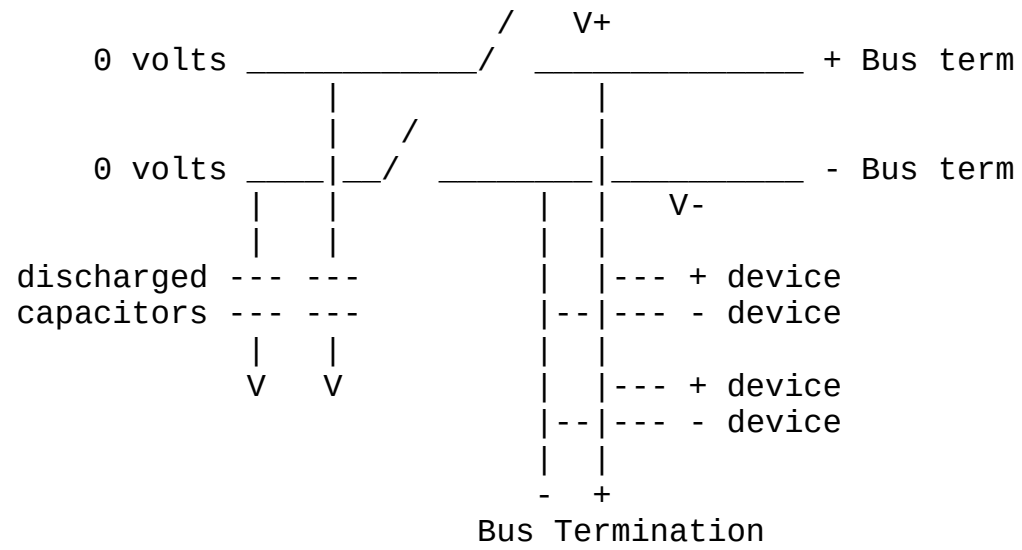
HOT SWAP TECHNICAL ISSUES

Hot insertion data has been taken on an LVD backplane. A variety of hot swap events with accompanying photos is presented.

When inserting differential drives into an active bus, it is necessary to treat the +, - signals as totally independent. When doing a mechanical insertion of a SCSI device, the time skew between top and bottom rows of contacts mating can exceed a millisecond. We cannot expect the + pins and - pins to mate within the same synchronous cycle.

SEQUENCES FOR PIN MATING



There are 4 possible mating events:
1 Mating to more positive line, with more negative line connected.

2 Mating to more positive line, with more negative line floating.

3 Mating to more negative line, with more positive line connected.

4 Mating to more negative line, with more positive line floating.

In cases 1 and 2, a really large transient can cause a reversal of the logical state of the bus.

In all 4 cases, a hot swap event can cause a timing shift of transitions on the bus.

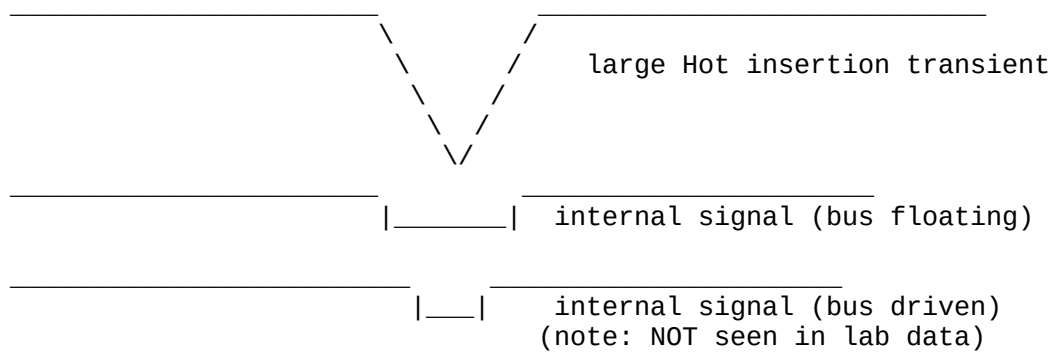
TIMING OF PIN MATING

There are 3 different timings for the mating events:
1 Bus is idle (all drivers high impedance); only 100-125mv of passive negation voltage across bus.

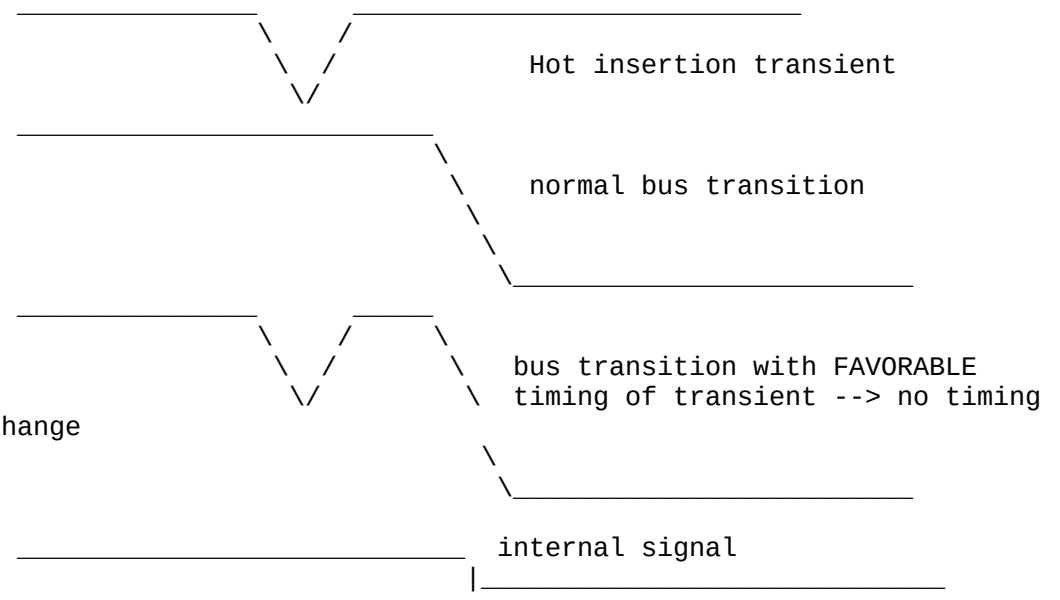
2 Bus is active and stable with full driven level for either assertion or negation, about 350-450mv difference across bus.

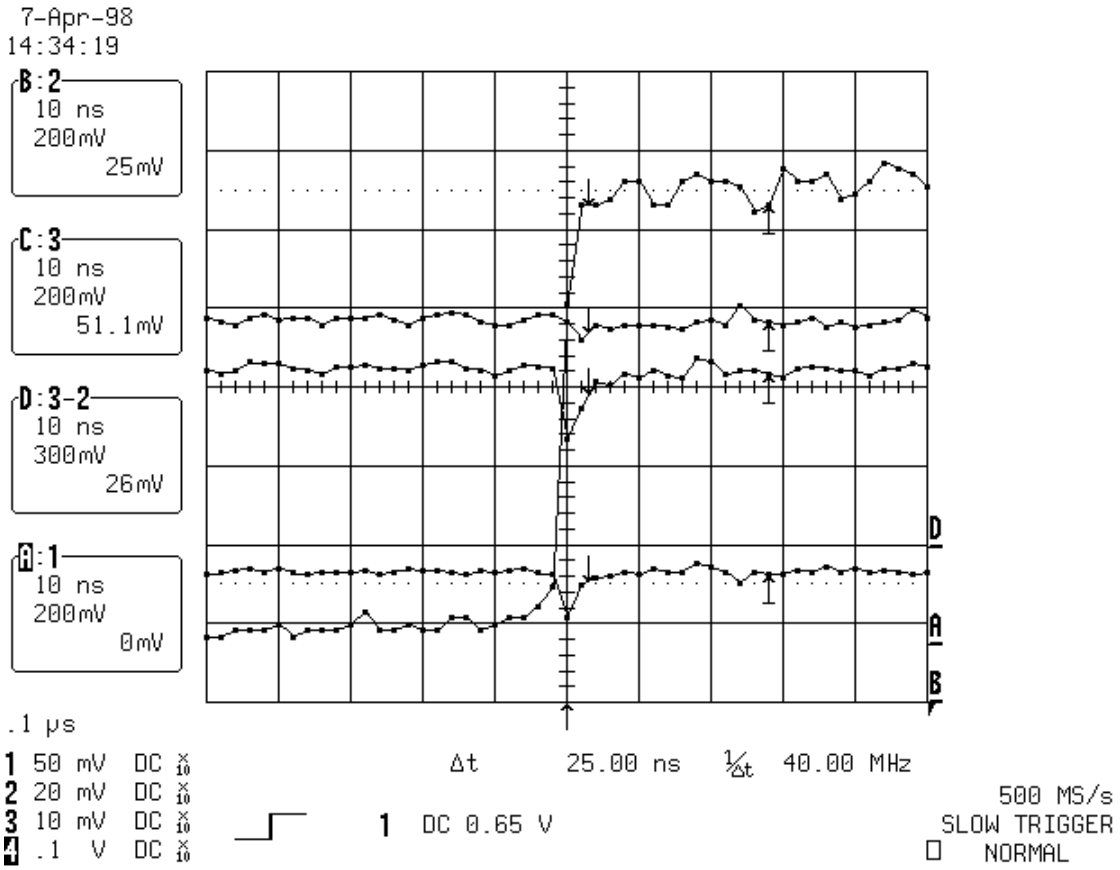
3 Bus is transitioning. The hot swap transient gets superimposed with a normal bus signal transition. The resulting transition can result in an edge either sooner than, or later than, the original pulse.

Severe glitch, not near valid bus transitions:

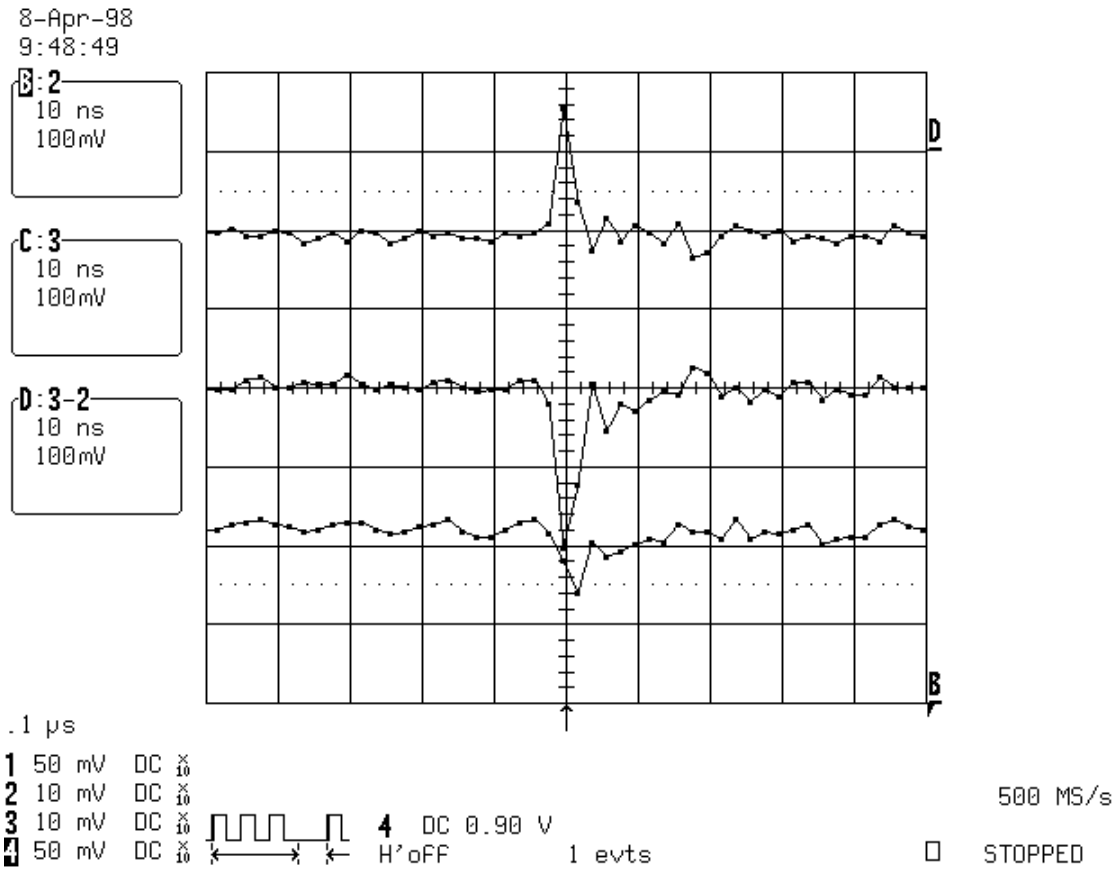


Less Severe glitch:

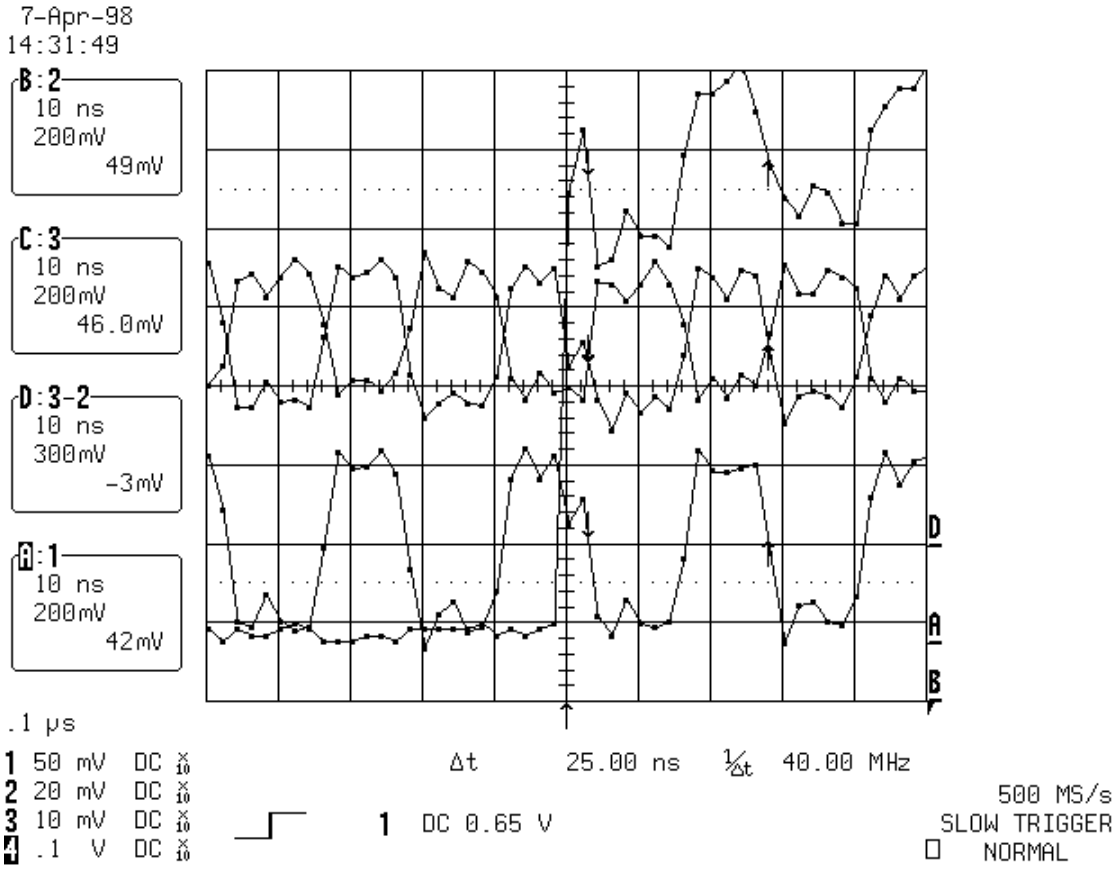




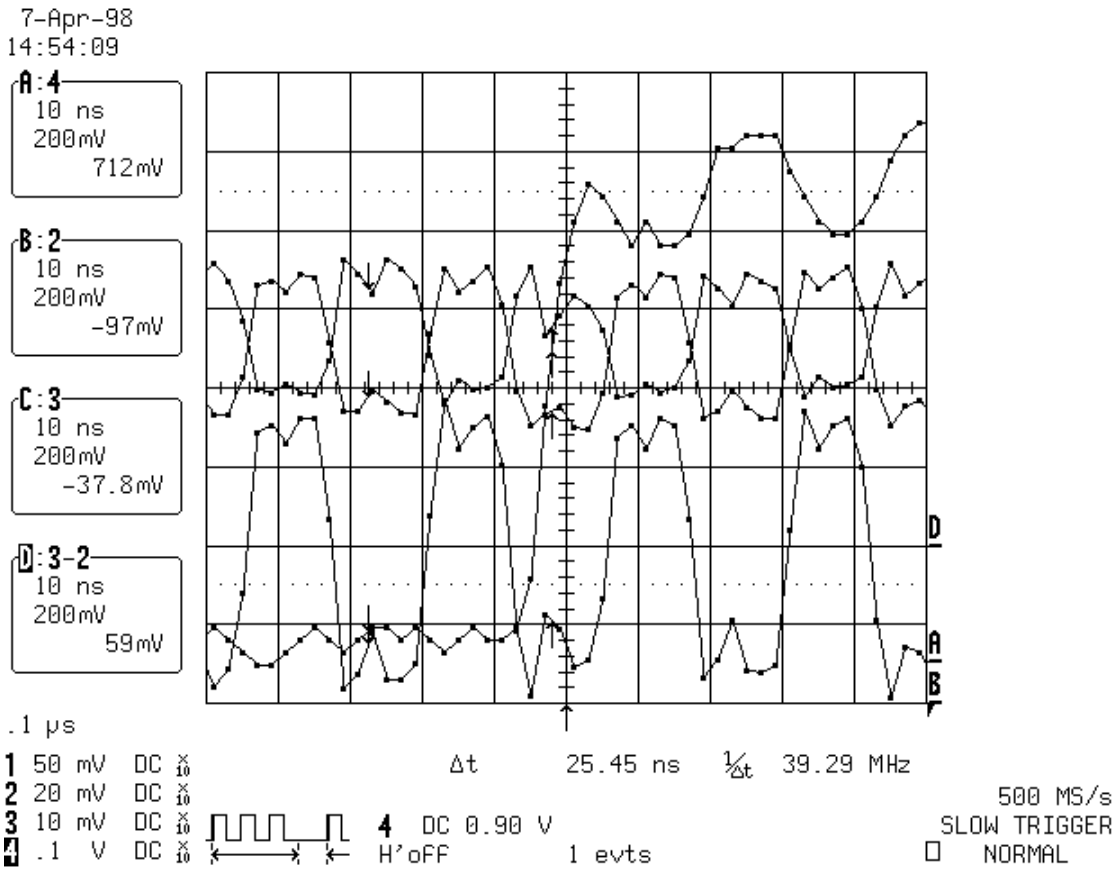
A plus pin glitch during bus free, which reinforces the negation state already present on the bus. No harm is done.



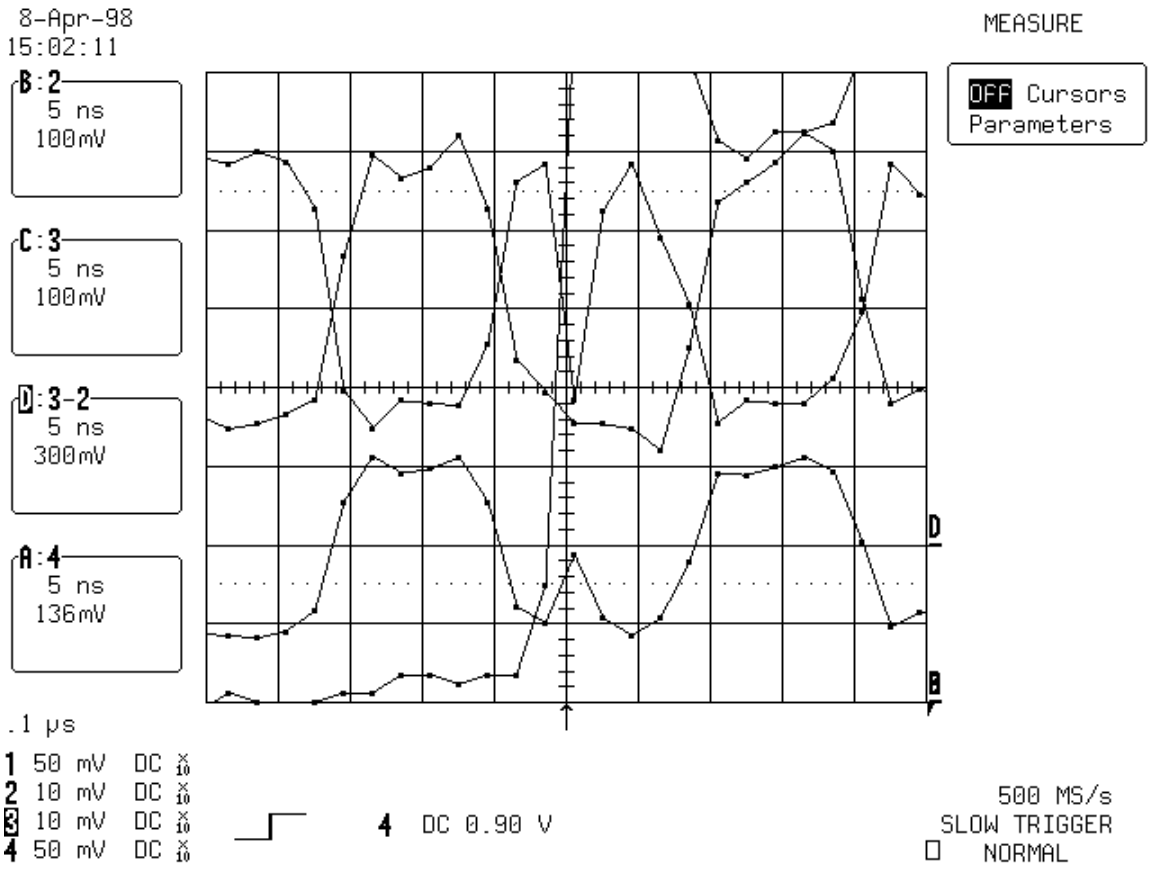
A bus free glitch on the minus pin which causes a very short assertion on the bus. Because of the bus free state, no harm is done.



A harmless glitch during a data transfer. The event is completed prior to the next transition.

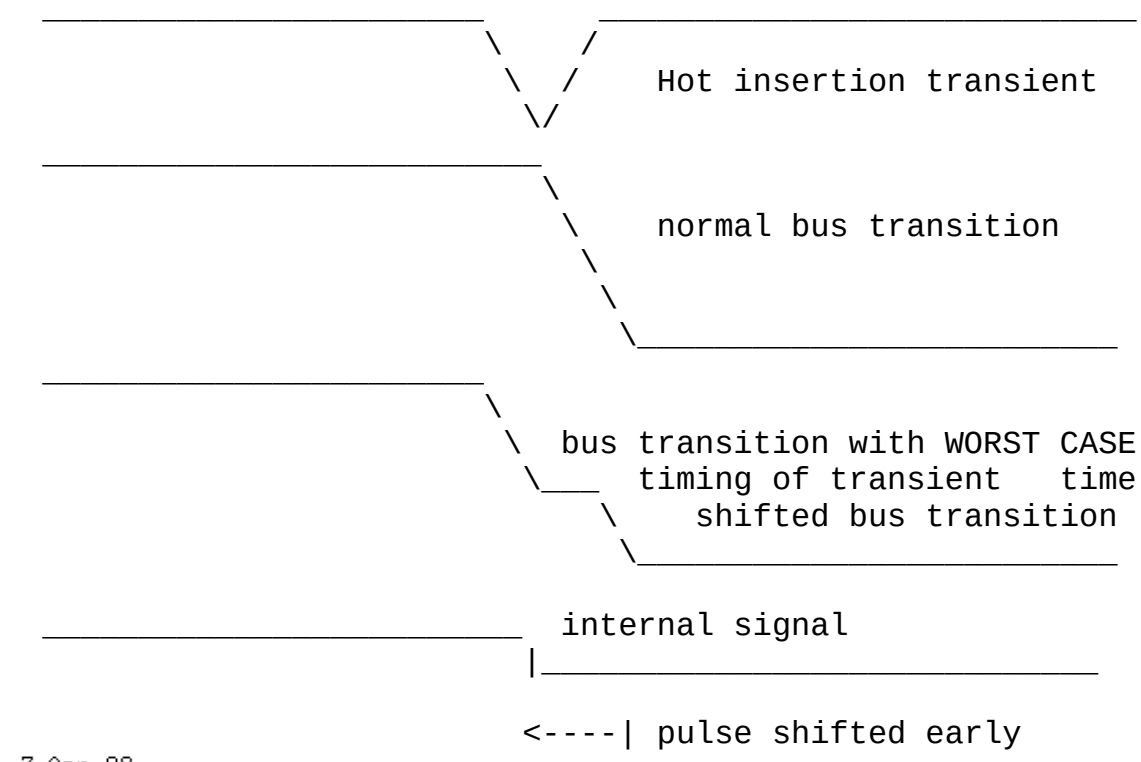


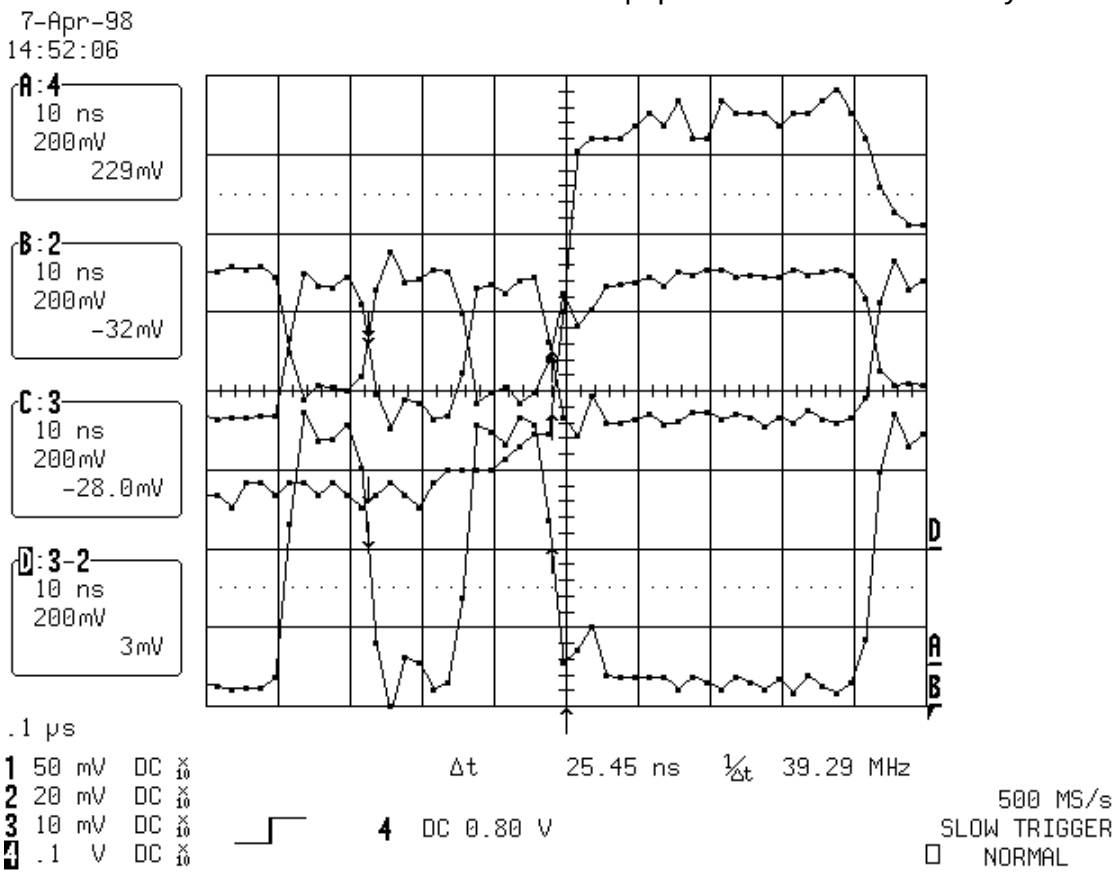
Another data transfer glitch. This event had a larger impedance on the mating contacts. The slower rise time at the inserted device results in a much lower amplitude glitch.



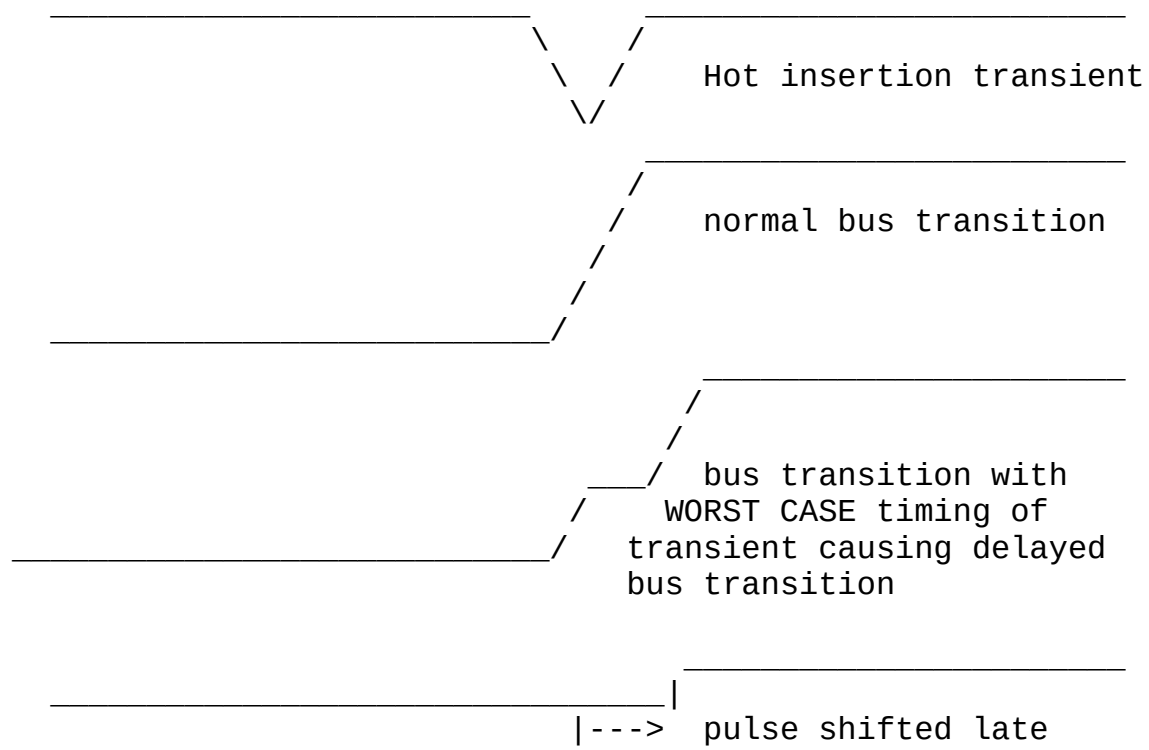
A hot insertion event observed at the insertion connector. The spike is much narrower and higher in amplitude than those other photos taken at the nearest load (potential victim).

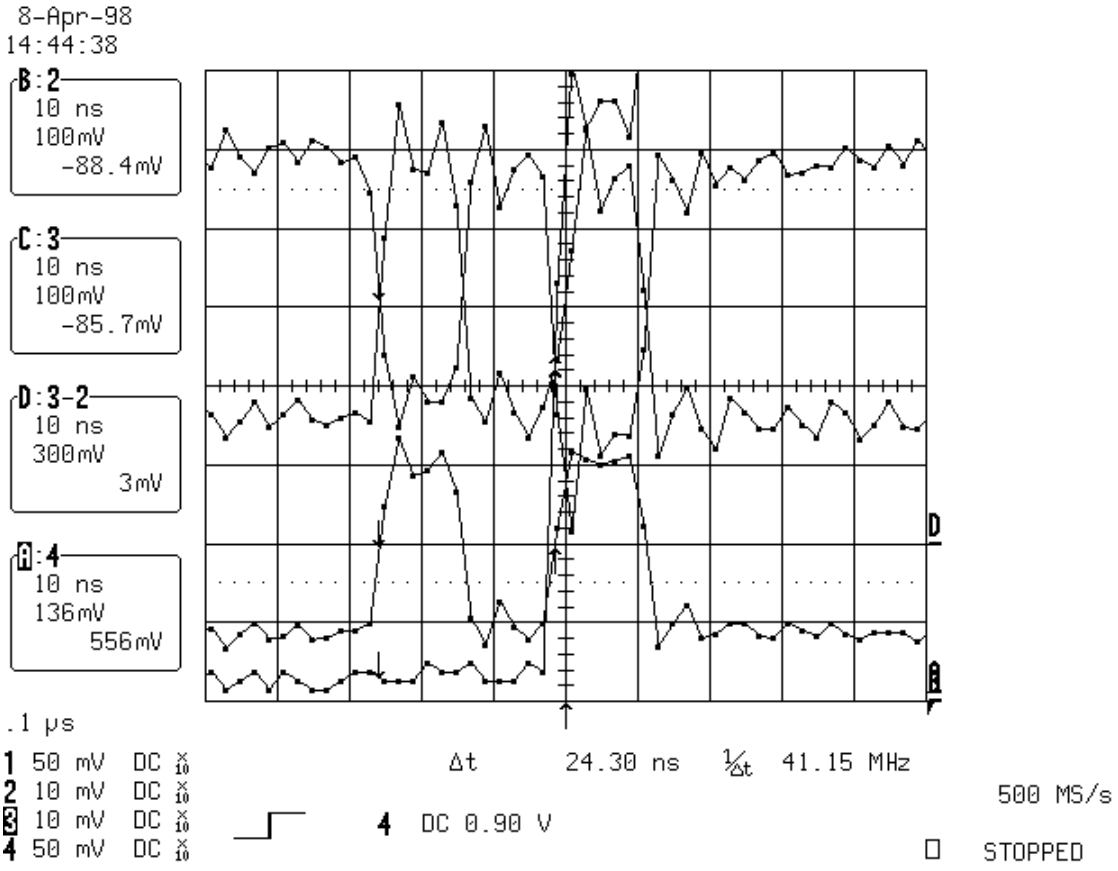
EARLY SHIFT CASE:





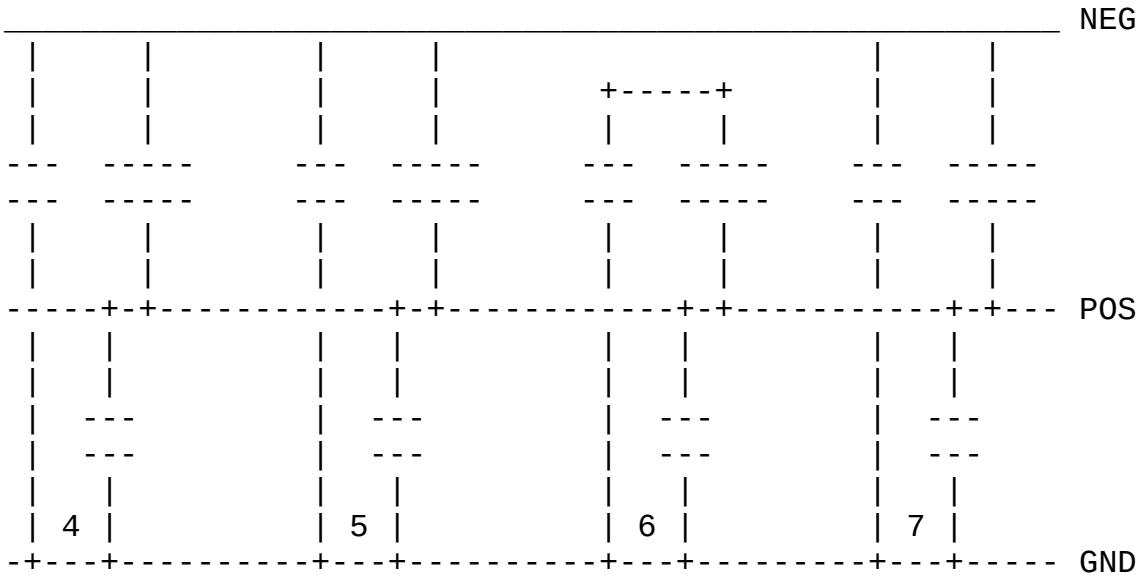
LATE SHIFT CASE:



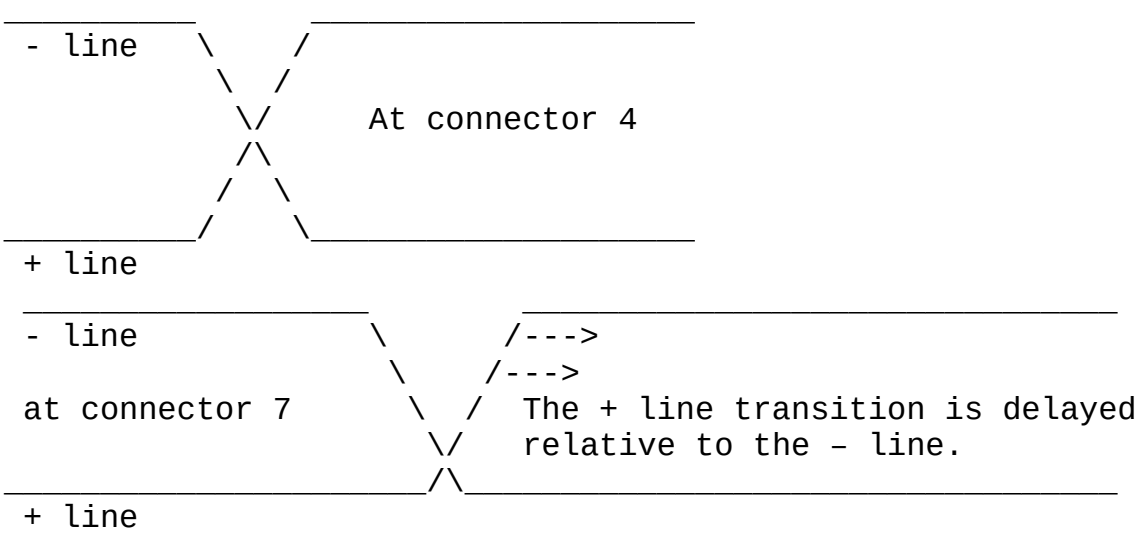


STATIC CAPACITIVE MISMATCH

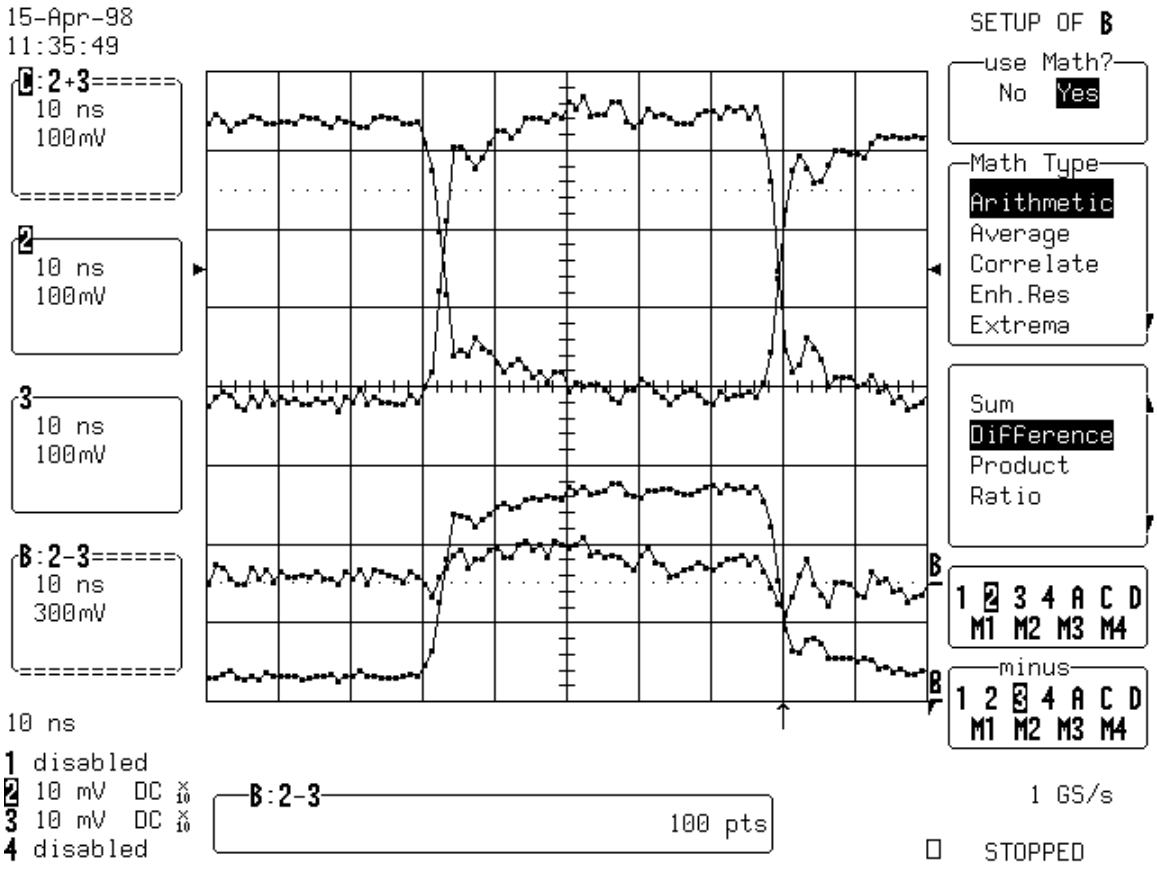
When one of the pair of differential signals has mated, but the other hasn't, there is a capacitance imbalance on the bus. This situation can easily exist for tens of microseconds, which amounts to thousands of bus data cycles. Distortion of the differential signals occurs at such a capacitance imbalance.



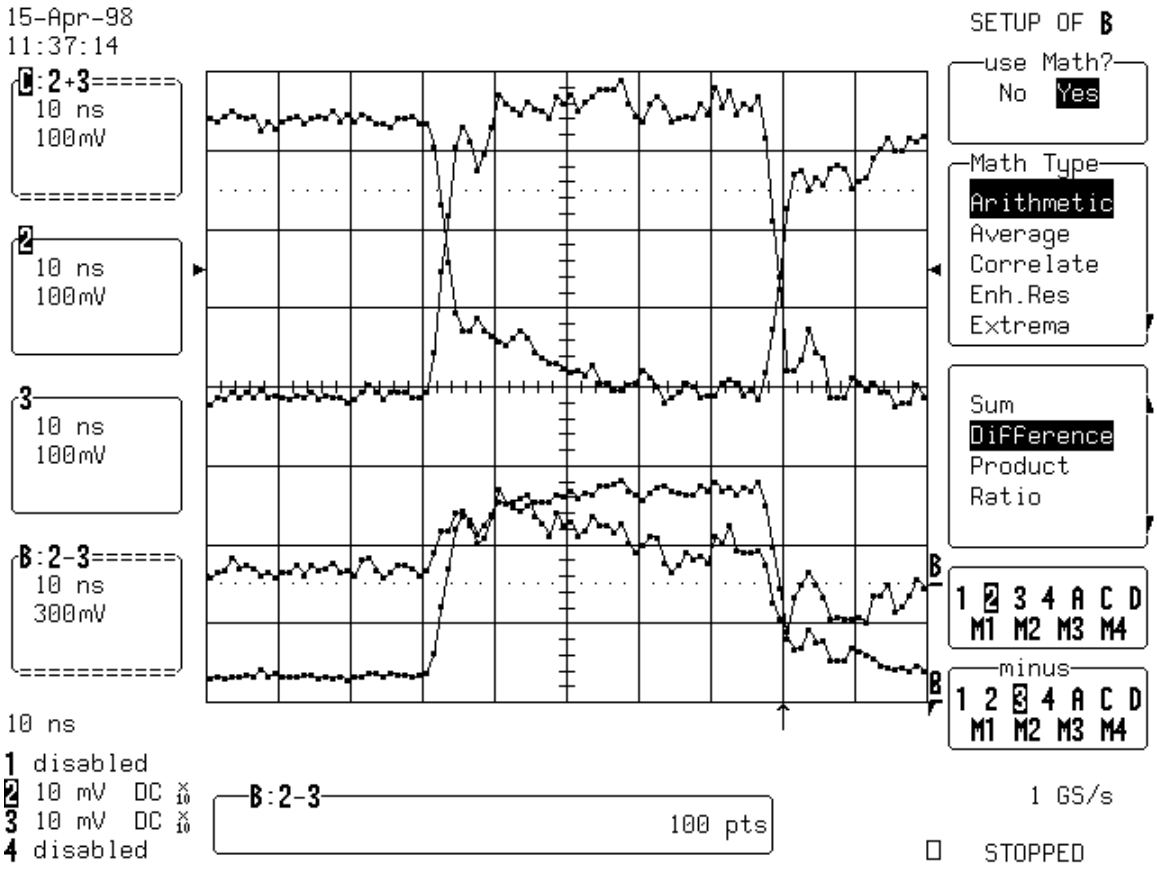
This sketch shows a bus with a partly mated drive at connector 6. The ground and + pin are connected, but the - pin is still open. The net effect is that there is an excess capacitance on the + pin.



Backplane with balanced loads. Signals being observed are the ACK lines on a backplane separated from the host by a 2 meter ribbon cable.



Same configuration, except load added to one side of the bus to unbalance the capacitance. Load consisted of a pair of 11pF scope probes.



Note the impact of the added load on the top trace, which goes high – low – high. The falling edge is delayed resulting in a higher differential crossover voltage. The rising edge is also delayed resulting in a lower differential crossover voltage.

SUMMARY:

- Hot insertion events DO NOT cause problems during bus free times.

- Hot insertion events DO NOT cause reversals of bus polarity during data transfers.

- Glitches, which are superimposed on either asserting or negating transitions, have the potential to shift the transition in time. This would cut into the set up and hold time margins.

- Because of the huge time delay between the mating of the contacts for a differential signal pair, the bus may have to operate for an extended time with a load half connected. The imbalance causes a signal distortion which can affect setup and hold time margins.

- No problems with Hot Swap Case 4 were found during this testing. However, please note that the Quantum drives used for this testing measured well under the allowed 20pF capacitance limit.

CONCLUSIONS:

- Case-4 Hot Swap has been demonstrated to work satisfactorily.

- Testing has not been exhaustive, and has used a single vendor’s backplane and only disk drives from Quantum Corp.