Seagate Technology
10323 West Reno (West Dock)
Oklahoma City, OK 73127-9705
P.O. Box 12313
Oklahoma City, OK 73157-2313
Tel: 405-324-3070
Fax: 405-324-3794
gene_milligan@notes.seagate.com

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John Lohmeyer
Chairman T10

Subject: Revision 4 of the Proposal for the Fast 80 Specifications in the SPI-3 Standard

Revision 4 implements the changes agreed to in the 7/14/98 Ad Hoc meeting. No additional changes are introduced except for including the proposed deletion of Note 2 in Table 1. The Fast-10, Fast-20, and Fast-40 timing values in Table 3 were corrected and adjusted.

Due to FrameMaker characteristics the change bars are intermittent.

Regarding clause, figure, and table numbers and related cross-references, I have purposely avoided devoting time to becoming proficient in FrameMaker and therefore warn, as does FrameMaker, that there are unresolved cross-references which in plain language should be considered for now wrong reference numbers.

Open Issues: (1) Should note 2 of Table 1 be eliminated in SPI-3? (2) The Receive Period Tolerance and the Transmit Period Tolerance of Table 3 are far too loose (depending upon the missing measurement method). What values should they be reduced to or should they be eliminated? This was again a homework assignment. (3) An editorial issue is what happened to the rest of the selection time-out delay definition.

Gene E. Milligan
Director, Development Strategy

Attachment: Fast 80 Draft for SPI-3 Revision 4 by PDF and change pages by paper.

1 SCSI parallel bus timing

Unless otherwise indicated, the delay-time measurements for each SCSI device, shown in table 1, shall be calculated from signal conditions existing at that SCSI device's port. ~~Thus, these measurements (except cable skew) may be made without considering delays in the cable.~~ The timing characteristics of each signal are described in the following paragraphs. Timing requirements relating to glitches are defined in clause 7.2.4.1.

Table 1 - SCSI bus control timing values

Timing description	Timing values
Arbitration Delay	2,4 µs
Bus Clear Delay	800 ns
Bus Free Delay	800 ns
Bus Set Delay	1,6 µs
Bus Settle Delay	400 ns
Cable Skew (note 1)	4 ns
Data Release Delay	400 ns
Disconnection Delay	200 us
Power on to Selection ~~(note 2)~~	10 s
Reset Hold Time	25 µs
Reset to Selection ~~(note 2)~~	250 ms
Selection Abort Time	200 µs
Selection Time-out Delay ~~(note 2)~~	250 ms
System Deskew Delay	45 ns

Notes:

1 Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew.

~~2 This is a recommended time. It is not mandatory.~~

Table 2 - SCSI bus data & information phase Single Transition timing values

Timing description	Timing values (note 5)				
	Asynch	**Fast-5**	**Fast-10**	**Fast-20**	**Fast-40**
Cable Skew (note 1)	4 ns	4 ns	4 ns	3 ns	2.5 ns
Receive Assertion Period (note 2)	N/A	70 ns	22 ns	11 ns	6,5 ns
Receive Hold Time (note 2 and note 3)	N/A	25 ns	25 ns	11,5 ns	4,75 ns
Receive Negation Period (note 2)	N/A	70 ns	22 ns	11 ns	6,5 ns
Receive Setup Time (note 2 and note 3)	N/A	15 ns	15 ns	6,5 ns	4,75 ns
Receive Period Tolerance	N/A	1.1 ns	1.1 ns	1.1 ns	1.1 ns
Signal Timing Skew ~~(note 1)~~	8 ns	8 ns	8 ns	5 ns	4,5 ns
Transfer Period during Synchronous Data Transfer Phases (note 4)	N/A	200 ns	100 ns	50 ns	25 ns
Transmit Assertion Period (note 2)	N/A	80 ns	30 ns	15 ns	8 ns
Transmit Hold Time (note 2 and note 3)	N/A	53 ns	33 ns	16,5 ns	9,25 ns
Transmit Negation Period (note 2)	N/A	80 ns	30 ns	15 ns	8 ns
Transmit Setup Time (note 2 and note 3)	N/A	23 ns	23 ns	11,5 ns	9,25 ns
Transmit Period Tolerance	N/A	1 ns	1 ns	1 ns	1 ns

Notes:

1 Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew.

2 See 1.2 for measurement points for the timing specifications.

3 See 1.3 for examples of how to calculate setup and hold timing.

4 The transfer period is measured from an assertion edge of the REQ/REQQ (ACK/ ACKQ) signal to the next assertion edge of the REQ/REQQ (ACK/ACKQ) signal.

5 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

Table 3 - SCSI bus data & information phase Double Transition timing values

Timing description	Timing Values (note 5)			
	Fast-10	**Fast-20**	**Fast-40**	**Fast-80**
Cable Skew (note 1)	4 ns	3 ns	2.5 ns	2.5 ns
Receive Assertion Period (note 2)	80 ns	40 ns	20 ns	10 ns
Receive Hold Time (note 2 and note 3)	25 ns	11,5 ns	4,75 ns	1,45 ns
Receive Negation Period (note 2)	80 ns	40 ns	20 ns	10 ns
Receive Setup Time (note 2 and note 3)	25 ns	11,5 ns	4,75 ns	1,45 ns
Receive Period Tolerance	1,1 ns	1,1 ns	1,1 ns	1,1 ns
Signal Timing Skew ~~(note 1)~~	26,3 ns	13.3 ns	6,8 ns	3,1 ns
Transfer Period during Synchronous Data Transfer Phases (note 4)	200 ns	100 ns	50 ns	25 ns
Transmit Assertion Period (note 2)	90 ns	45 ns	22,5 ns	11,5 ns
Transmit Hold Time (note 2 and note 3)	37 ns	18,5 ns	9,25 ns	4,55 ns
Transmit Negation Period (note 2)	90 ns	45 ns	22,5 ns	11,5 ns
Transmit Setup Time (note 2 and note 3)	37 ns	18,5 ns	9,25 ns	4,55 ns
Transmit Period Tolerance	1 ns	1 ns	1 ns	1 ns

Notes:

1 Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew.

2 See 1.2 for measurement points for the timing specifications.

3 See 1.3 for examples of how to calculate setup and hold timing.

4 The transfer period is measured from an assertion edge of the REQ/REQQ (ACK/ACKQ) signal to the next assertion edge of the signal. The nominal data transfer period is half that of the transfer period since data is qualified on both the assertion and negation edges of the REQ/REQQ (ACK/ACKQ) signal.

5 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

1.1 Timing description

1.1.1 Arbitration delay

The minimum time an SCSI device shall wait from asserting the BSY signal for arbitration until the DATA BUS is examined to see if arbitration has been won. There is no maximum time.

1.1.2 Bus clear delay

The maximum time for an SCSI device to release all SCSI bus signals after:

a) the BUS FREE phase is detected (the BSY and SEL signals are both false for a bus settle delay);
b) the SEL signal is received from another SCSI device during the ARBITRATION phase;
c) the transition of the RST signal to true.

For item a) above, the maximum time for an SCSI device to release all SCSI bus signals is 1200 ns from the BSY and SEL signals first becoming both false. If an SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall release all SCSI bus signals within a bus clear delay minus the excess time.

1.1.3 Bus free delay

The minimum time that an SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of the BSY signal in preparation for entering the ARBITRATION phase.

1.1.4 Bus set delay

The maximum time for an SCSI device to assert the BSY signal and its SCSI ID after it detects a BUS FREE phase for the purpose of entering the ARBITRATION phase.

1.1.5 Bus settle delay

The minimum time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

1.1.6 Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

1.1.7 Data release delay

The maximum time for an initiator to release the DATA BUS signals following the transition of the I/O signal from false to true.

1.1.8 Disconnection delay

The minimum time that a target shall wait after releasing BSY before participating in an ARBITRATION phase when honoring a DISCONNECT message from the initiator.

1.1.9 Power on to selection

The ~~recommended~~ maximum time from power application until an SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI-3 Primary Commands Standard).

1.1.10 Receive assertion period

The minimum time required at a SCSI device receiving a REQ or REQQ signal for the signal to be asserted while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK or ACKQ signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. The timings for the REQQ and ACKQ signals only apply to wide data transfers.

1.1.11 Receive hold time

The minimum time required at the receiving SCSI device between the assertion of the REQ or REQQ signal or the ACK or ACKQ signals and the changing of the DATA BUS while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit-wide data transfers.

1.1.12 Receive negation period

The minimum time required at a SCSI device receiving a REQ or REQQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK or ACKQ signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. The timings for the REQQ and ACKQ signals only apply to wide data transfers.

1.1.13 Receive period

The receive period is the average time between assertion edges of the REQ/REQQ (ACK/ACKQ) signal measured without offset interruptions.

1.1.14 Receive setup time

The minimum time required at the receiving SCSI device between the changing of DATA BUS and the assertion of the REQ or REQQ signal or the ACK or ACKQ signal while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit-wide data transfers.

1.1.15 Receive period tolerance

The minimum tolerance that an SCSI device shall allow to be subtracted from the negotiated synchronous period.

1.1.16 Reset hold time

The minimum time that the RST signal is asserted. There is no maximum time.

1.1.17 Reset to Selection

The ~~recommended~~ maximum time from after a reset condition until an SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI-3 Primary Commands Standard).

1.1.18 Selection abort time

The maximum time that an SCSI device shall take from its most recent detection of being selected or reselected until asserting a the BSY signal in response. This time-out is required to ensure that a target or initiator does not assert the BSY signal after a SELECTION or RESELECTION phase has been aborted.

1.1.19 Selection time-out delay

The minimum time that an initiator or target should wait for ~~a~~ the assertion of the BSY signal in response during the SELECTION or RESELECTION phase before starting the time-out procedure. ~~Note that this is only a recommended time period.~~?????

1.1.20 Signal Timing Skew

The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ/REQQ (ACK/ACKQ) signal. The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 1, figure 2, figure 1, and figure 2.

The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 1.2)

1.1.21 System deskew delay

The minimum time that a SCSI device should wait after receiving an SCSI signal to ensure that any signals transmitted at the same time are valid. The system deskew delay shall not be applied to the synchronous data transfers.

1.1.22 Transmit assertion period

The minimum time that a target shall assert the REQ or REQQ signal while using synchronous data transfers. Also, the minimum time that an initiator shall assert the ACK or ACKQ signal while using synchronous data transfers. The timing for the REQQ and ACKQ signals only apply to 32-bit-wide data transfers.

1.1.23 Transmit hold time

The minimum time provided by the transmitting SCSI device between the assertion of the REQ or REQQ signal or the ACK or ACKQ signal and the changing of the DATA BUS while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

1.1.24 Transmit negation period

The minimum time that a target shall negate the REQ or REQQ signal while using synchronous data transfers. Also, the minimum time that an initiator shall negate the ACK or ACKQ signal while using synchronous data transfers. The timing for the REQQ and ACKQ signals only apply to 32-bit -wide data transfers.

1.1.25 Transmit period

The transmit period is the average time between assertion edges of the REQ/REQQ (ACK/ACKQ) signal measured without offset interruptions.

1.1.26 Transmit setup time

The minimum time provided by the transmitting SCSI device between the changing of DATA BUS and the assertion of the REQ or REQQ signal or the ACK or ACKQ signal while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit -wide data transfers.

1.1.27 Transmit period tolerance

The maximum tolerance that an SCSI device may subtract from the negotiated synchronous period.

1.2 Measurement points

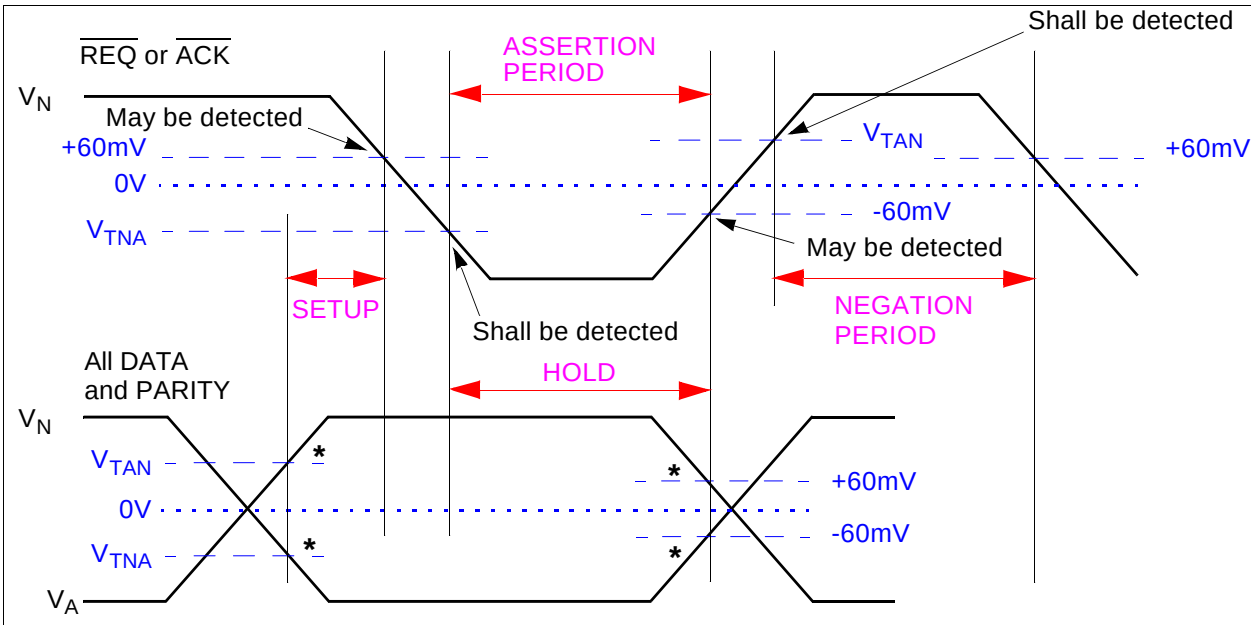
The measurements points for SE and differential ACK, REQ, DATA, and PARITY signals are defined in this clause.

1.2.1 SE fast-10 data transfer rates

SE SCSI devices with data transfer rates up to and including fast-10 shall use the measurement points defined in figure 1 for the measurement of the timing values. The rise and fall times for the SE REQ/ACK signals shall be nominally the same as for the SE DATA/PARITY signals.

1.2.2 LVD ~~=<40 MT/s~~ Single Transition

LVD SCSI devices with a single transition agreement shall use the measurement points defined in figure 1 for the measurement of the timing values. The rise and fall times for the LVD REQ/ACK signals shall be nominally the same as for the LVD DATA/PARITY signals.



* Use the crossing that yields the shorter SETUP and HOLD time

V_{TNA} = - max [60 mV or (0,25 x V_N)]
V_{TAN} = max [60 mV or (-0,25 x V_A)]
1,0 V ≥ V_N ≥ 60 mV
-1,0 V ≤ V_A ≤ -60 mV
Differential voltage signals in all cases

Notes:
1 V_N and V_A are measured at the start of a transition.
2 V_{TNA} - Voltage threshold negation to assertion.
3 V_{TAN} - Voltage threshold assertion to negation.

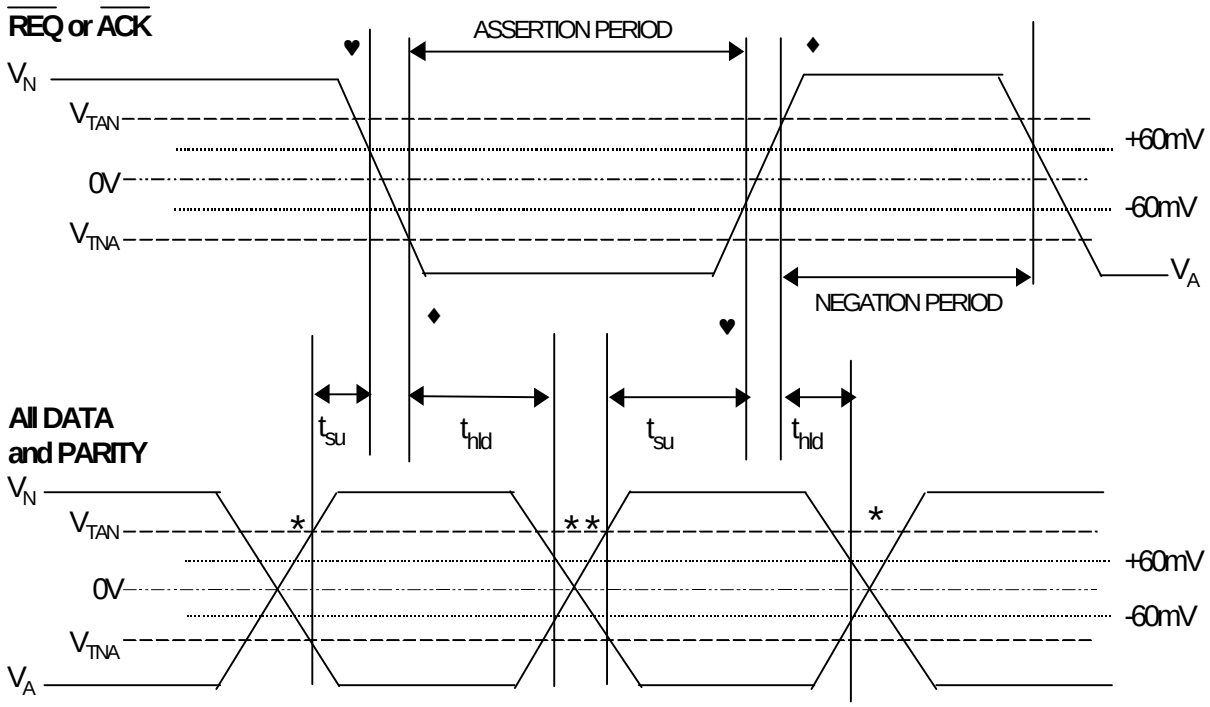
Figure 1 - Fast 40 LVD timing measurement points

Figure 1 illustrates that receivers may require a larger LVD signal to overcome a strongly asserted or negated state than required for a weakly asserted or negated state. With the maximum assertion level of V_A it requires a signal that crosses the zero differential level by at least 0,25 x V_A (but at least by 60 mV in all cases) to guarantee detection of a negation for fast signals. The same relationship applies for the maximum negated level V_N. Conditions exist with longer loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 1 are used in the measurement of timing parameters.

Measurement of driver timing parameters shall be performed using the circuit and test conditions defined in A.2.5 applied to the device connector. Receiver timing parameters are defined by the waveforms existing at the connector of the receiving SCSI device. The receiver timing parameters include the effects of data pattern. The receiver data pattern is therefore not defined.

1.2.3 LVD ~~>40 MT/s~~ Double Transition

LVD SCSI devices, which have a ~~transfer~~ double transition agreement ~~in the Fast-80 range~~ shall use the measurement points defined in figure 1 for the measurement of the timing values. The rise and fall times for the LVD REQ/ACK signals shall be nominally the same as for the LVD DATA/PARITY signals.



⁎ Use the crossing that yields the shorter SETUP and HOLD time
♦ Shall be detected
♥ May be detected

V_{TNA} = -max[60mV or (0,25 x V_N)]
V_{TAN} = max [60 mV or (-0,25 x V_A)]
1,0 V ≥ V_N ≥ 60 mV
-1,0 V ≤ V_A ≤ -60 mV
Differential voltage signals in all cases

Notes:
1 V_N and V_A are measured at the start of a transition.
2 V_{TNS} - Voltage threshold negation to assertion.
3 V_{TAN} - Voltage threshold assertion to negation.
4 t_{su} - Setup time.
5 t_{hld} - Hold time.

Figure 2 - Fast 80 LVD timing measurement points

1.2.4 Fast-40 data transfer rates

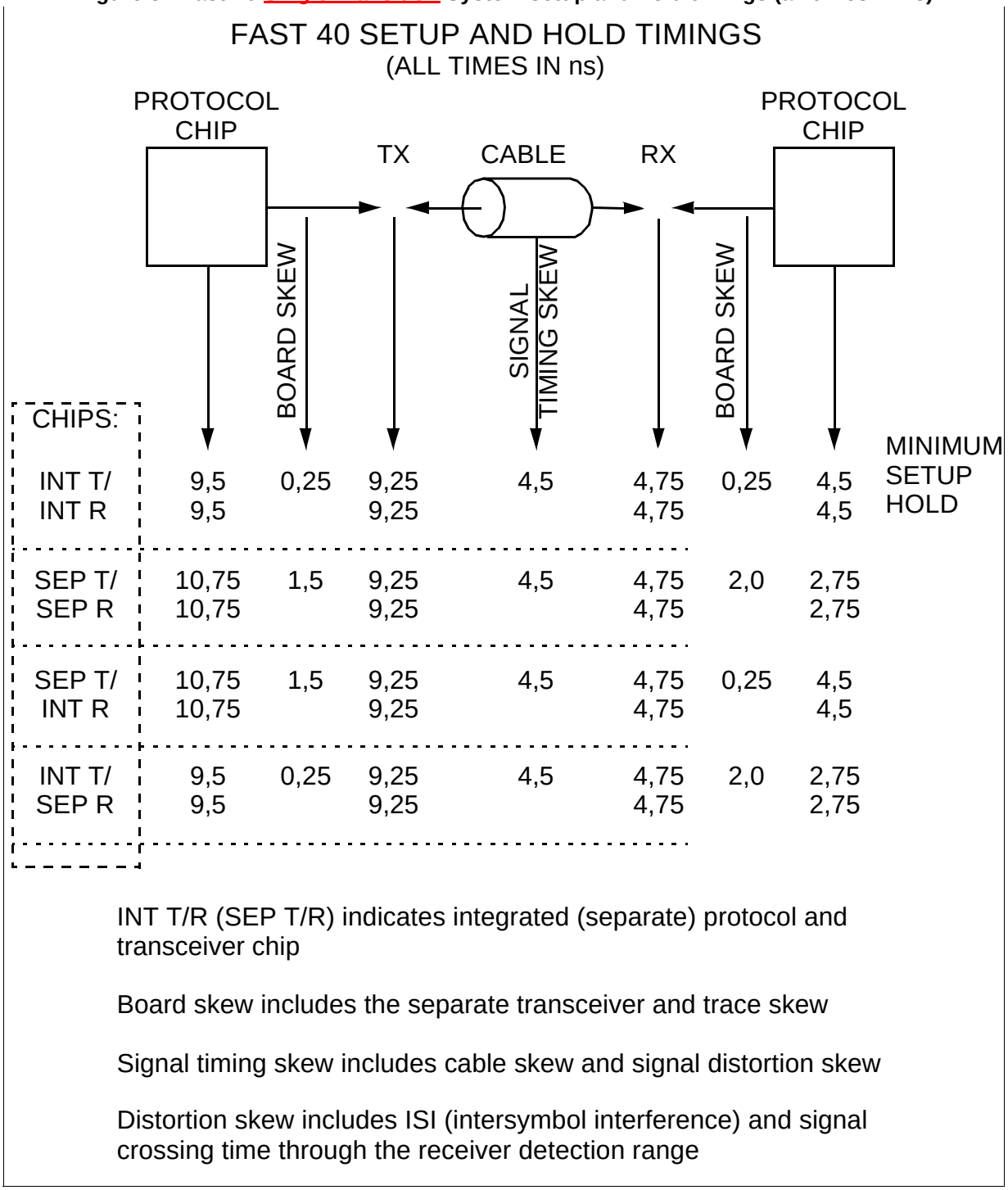
Figure 3 shows how the setup and hold times are calculated for various physical configurations on SCSI devices that support up to and including fast-40 data transfers. The minimum set up and hold timings specified in figure 3 shall be used. Note that these values are different for the driver and the receiver but that the receiver sensitivity provides the threshold points for both. This is required because both extreme cases of attenuation need to be covered:

a) receivers connected to drivers with very short interconnect, and
b) receivers connected to drivers through worst case interconnect.

Fast-40 Single Transition setup and hold times shall apply if a transfer rate >20 and up to 40 MT/S is

negotiated.

Figure 3 - Fast-40 Single Transition System setup and hold timings (all times in ns)



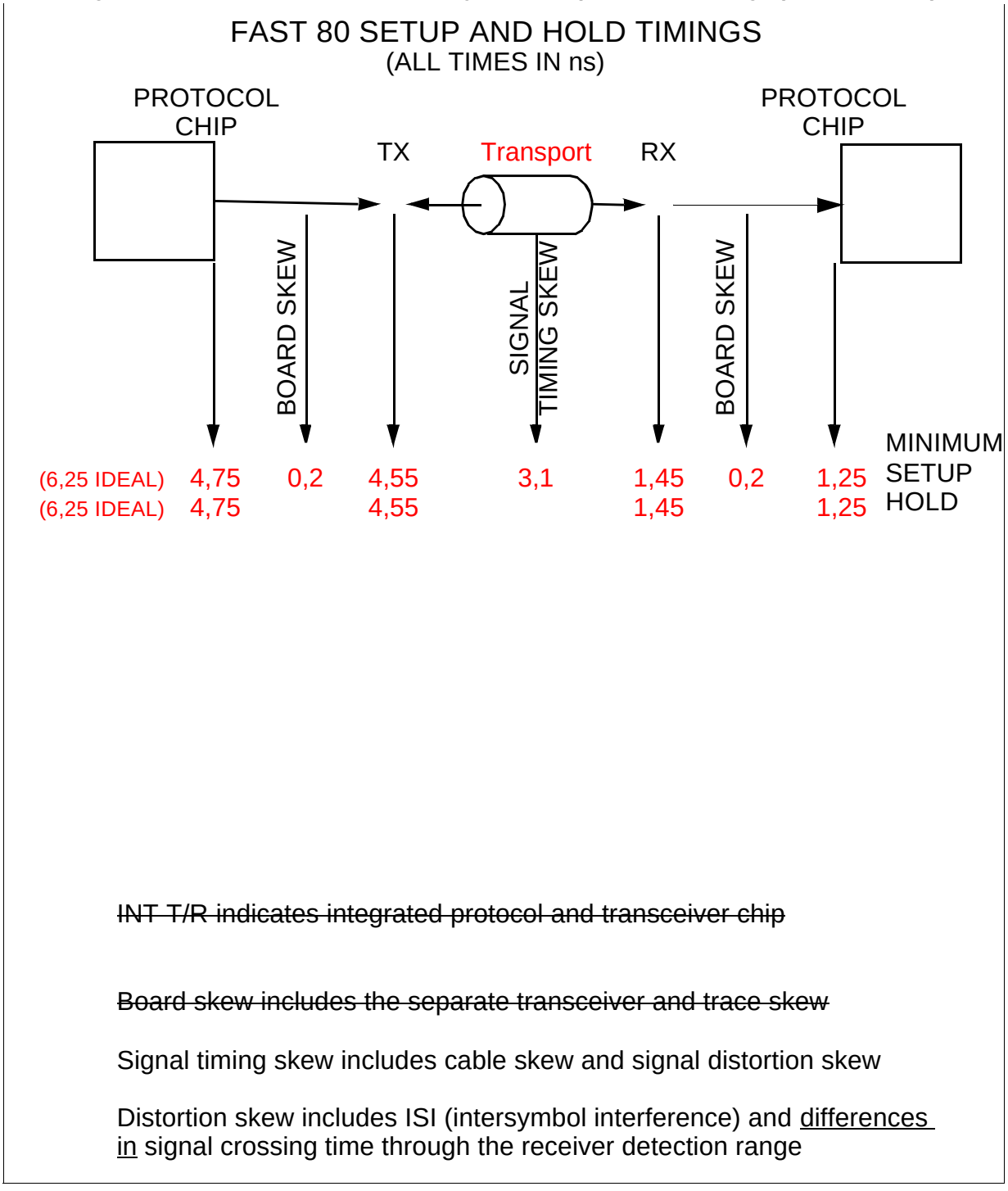
1.2.5 Fast-80 data transfer rates

Figure 5 shows how the setup and hold times are calculated for various physical configurations on SCSI devices that support up to and including fast-80 data transfers. The minimum set up and hold timings specified in figure 5 shall be used. Note that these values are different for the driver and the receiver but that the receiver sensitivity provides the threshold points for both. This is required because both extreme cases of attenuation need to be covered:

a) receivers connected to drivers with very short interconnect, and
b) receivers connected to drivers through worst case interconnect.

Fast-80 Double Transition setup and hold times shall apply if a transfer rate >40 and up to 80 MT/S is negotiated.

Figure 4 - Fast-80 Double Transition System setup and hold timings (all times in ns)



~~INT T/R indicates integrated protocol and transceiver chip~~

~~Board skew includes the separate transceiver and trace skew~~

Signal timing skew includes cable skew and signal distortion skew

Distortion skew includes ISI (intersymbol interference) and differences in signal crossing time through the receiver detection range

2 SCSI parallel interface electrical characteristics

SPI-3 devices may use the following transmitter implementations:

a) SE active negation;
b) LVD.

LVD/MSE transmitters support SE active negation. LVD/MSE device may be damaged if exposed to SE passive negation voltages.

If a transceiver fully complies with the requirements of more than one of the above transmitter implementations then it may interoperate with those transceiver types.

For each transmitter implementation one or more different receiver and capacitance specifications may apply.

For measurements in this clause, SCSI bus termination is assumed to be external to the SCSI device. See 6.4 for the terminating requirements for the RESERVED lines. SCSI devices may have provision for allowing optional internal termination provided the internal termination conforms with 7.1.1, 2.1.1, 2.2.1 or 7.4.1 when enabled and the SCSI device, including the disabled termination, conforms with 7.1.4, 2.1.4, or 7.4.3 when the internal termination is disabled.

In addition to the device electrical requirements defined in the remaining subclauses of this clause, devices shall meet the requirements specified in table 4 and table 5 at the device connector.

Table 4 - Electrical input requirements at the device connector

Value	Minimum	Maximum	Notes
SE (active negation) and MSE input voltage	-0,5 V D.C.	4,1 V D.C.	Absolute maximum at all operating conditions, including the DIFFSENS connection for SE (active negation), and LVD/MSE SCSI devices, for SCSI devices meeting the fast-20 requirements in table 24.
LVD input voltage (D.C. V + or - signal to local ground)	-0,5 V D.C.	4,1 V D.C.	Absolute maximum at all operating conditions all signals except DIFFSENS.

Table 5 - Input current requirements at the device connector for lines not being driven by the device

Value	Maximum	Notes
MSE current magnitude	20 µA D.C.	Measured from + or - signal V_{IN} 0 to 4,1 V to local ground each signal pin.
LVD current magnitude	20 µA D.C.	Measured from + or - signal V_{IN} < 2,5 V to local ground each signal pin.

2.1 LVD alternative

2.1.1 LVD termination

The electrical characteristics of LVD bus termination shall be as specified in this subclause. Figure 5 shows the V_B and V_A measurement points, referenced to local ground, for the differential LVD bus terminator.

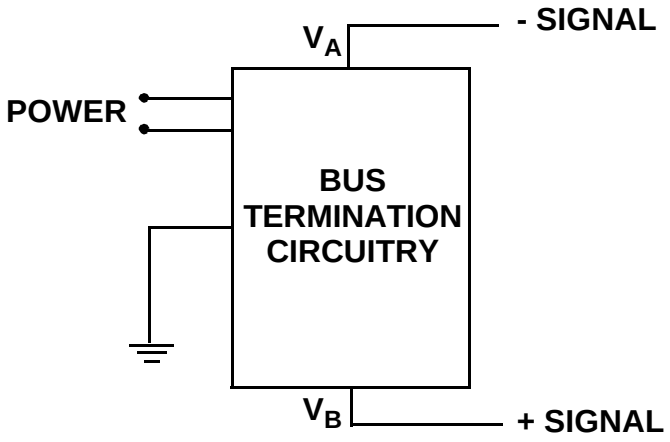


Figure 5 - Differential LVD bus terminator

Figure 5 through figure 10 define the measurement points for the LVD terminators. Electrical characteristics shall meet the requirements in table 6 and table 7.

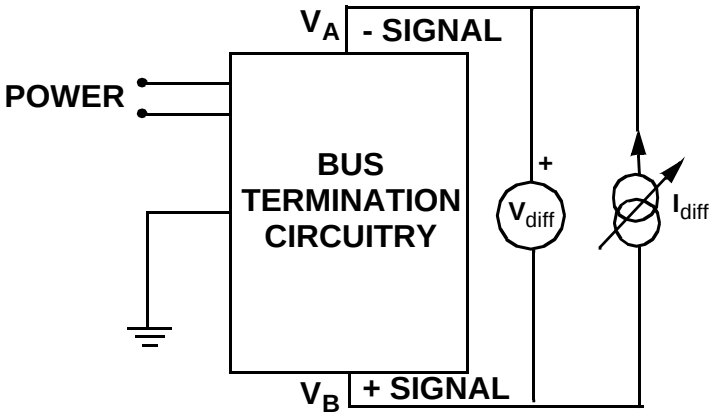


Figure 6 - Test circuit for terminator differential impedance

The requirements on the LVD bus termination that relate to differential impedance are specified in figure 6 and table 6. Figure 7 and table 6 show the allowed ranges for I_{diff} and V_{diff} in figure 6. The requirements that relate to differential impedance are specified in figure 7 and table 6. Table 6 specifies the allowed ranges for I_{diff} and V_{diff} in figure 6. The terminator bias voltage V_{BIAS} (V_{BIAS} is the voltage measured when I=0 in figure 27) shall have the values measured between V_1 and V_2 as measured at V_{diff} in figure 6 with the range values defined in table 6 in the LVD impedance and V_{BIAS} tests column.

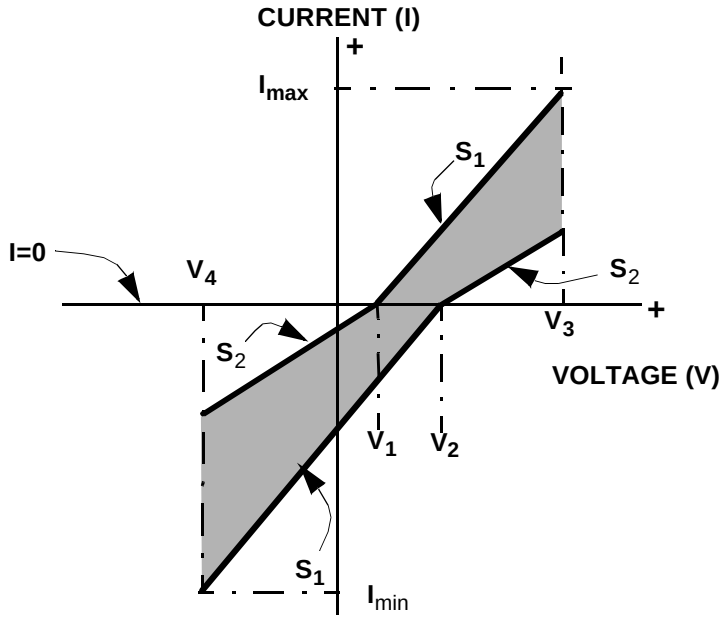


Figure 7 - Termination I-V characteristics for differential and common mode impedance tests

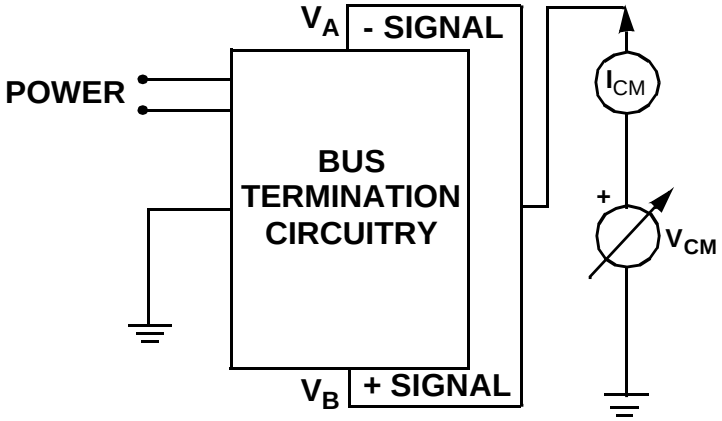


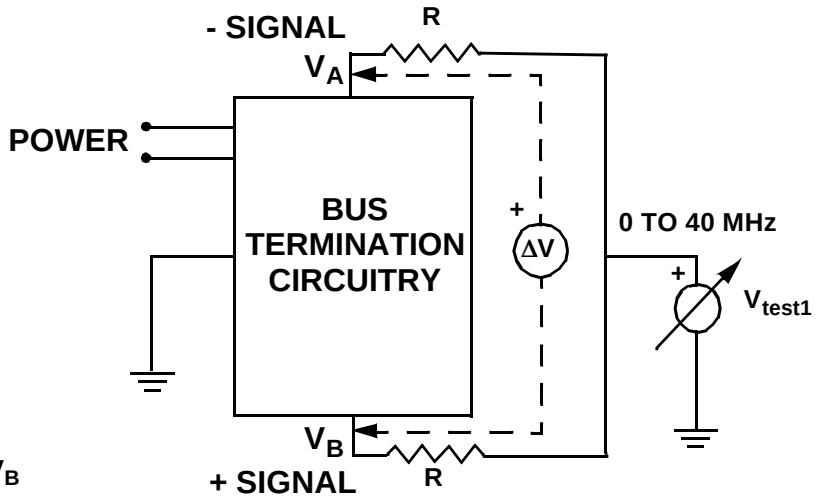
Figure 8 - Test circuit for termination common mode impedance test

The requirements that relate to common mode impedance are specified in figure 7 and table 6. Table 6 specifies the allowed ranges for I_{CM} and V_{CM} in figure 8. The terminator bias voltage V_{BIAS} (V_{BIAS} is the voltage measured when I=0 in figure 27) shall have the values measured between V_1 and V_2 as measured at V_{CM} in figure 8 with the range values defined in table 6 in the common mode impedance and V_{BIAS} tests column.

Table 6 - I-V requirements for LVD impedance, common mode impedance, and V_{BIAS} tests

Values (figure 7)	LVD impedance and V_{BIAS} tests (note) (figure 6)	Common mode impedance and V_{BIAS} tests (figure 8)
V_1 (mV)	100	1125
V_2 (mV)	125	1375
V_3 (V)	1,0	2,0
V_4 (V)	-1,0	0,5
I_{max} (mA)	9,00	N/A
I_{min} (mA)	-11.25	N/A
S_1 (ohms)	100	100
S_2 (ohms)	110	300
Measurement	D.C.	D.C.
Note: $V_A + V_B = 2,5 \pm 0,2$ V (figure 6)		

The requirements on termination that relate to electrical balance are specified in figure 9, figure 10, and table 7. The voltage V_{test1} in figure 9 is varied over frequencies of 0 to 40 MHz with amplitude varied over the range V_{MIN} to V_{MAX} specified in table 7 while the voltage named ΔV in figure 9 is measured. The maximum difference between values of ΔV (ΔV in figure 9) measured during this test shall be as specified in table 7.



Note: $\Delta V = V_A - V_B$

Figure 9 - Termination balance test configuration

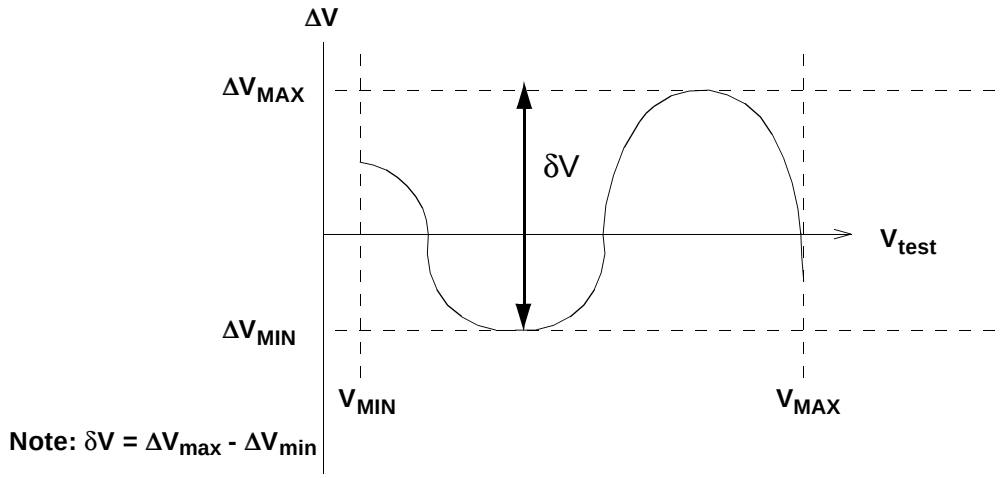


Figure 10 - Termination balance test data definition

Table 7 - Values for LVD termination balance test

Value	LVD
V_{MIN} (V_{test1} peak)	0,7
V_{MAX} (V_{test1} peak)	1,8
R (ohms)	100 ± 0,01%
δV	20 mV max
Note: ΔV - Input impedance for instrumentation > 10 Kohms V_{test1} swept through all values between V_{MIN} and V_{MAX}	

2.1.2 LVD driver characteristics

The LVD driver shall provide balanced asymmetrical sources that provide current from positive supply voltage to one signal line while sinking the same current to ground from the other signal line as shown in figure 11. Diagonally opposite sources operate together to produce a signal assertion or a signal negation. An assertion is produced when positive supply voltage current is sourced from source 4 to the +signal line and source 2 sinks the same current from the -signal line to ground. A negation is produced when positive supply voltage current is sourced from source 1 to the -signal line and source 3 sinks the same current from the +signal line to ground.

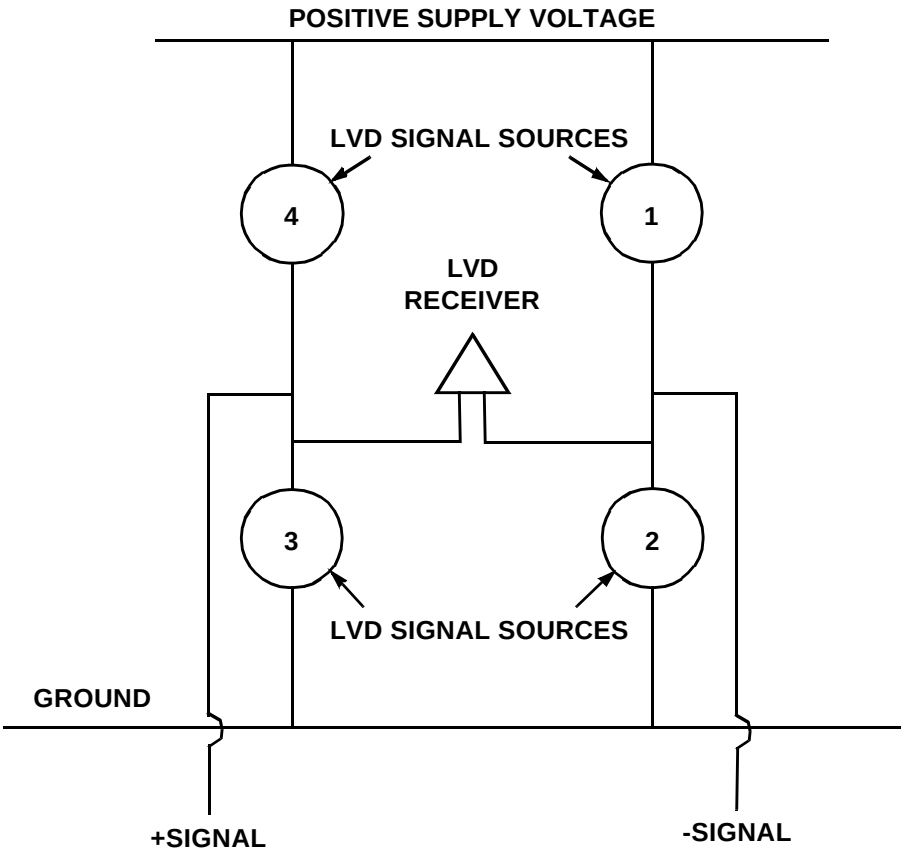


Figure 11 - LVD transceiver architecture

Balanced transmissions occur when the changes in +SIGNAL current and the changes in the -SIGNAL current precisely cancel each other. The balance is important to reduce EMI and common mode signals. Asymmetry occurs when the intensity of the source 2 and 4 assertion pair is different from the source 1 and 3 negation pair. To compensate for the negation biasing effect of the terminators, the 2 and 4 assertion pair is stronger than the 1 and 3 negation pair.

LVD drivers shall meet the specifications in annex A.

2.1.3 LVD receiver characteristics

LVD receivers shall be connected to the +signal and -signal as shown in figure 11. An example of an LVD receiver is shown in figure 12. LVD receivers shall meet the requirements in annex A.

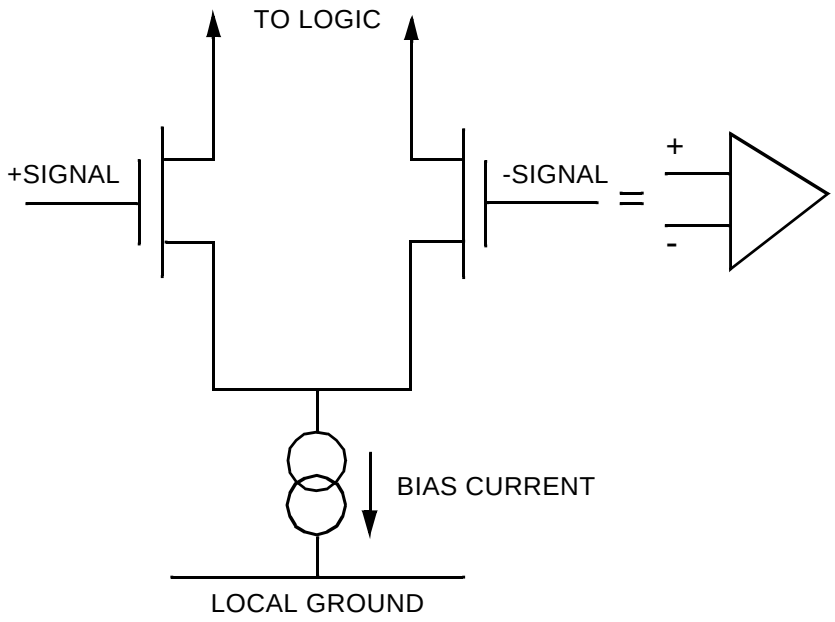


Figure 12 - LVD receiver example

2.1.4 LVD capacitive loads

Capacitive loads on differential SCSI busses shall meet the requirements specified in this section.

There are three components to differential SCSI bus capacitive loading: -Signal to local ground (C1), +Signal to local ground (C2), and -signal to +signal (C3) as shown in figure 13. The values C1, C2, and C3 represent measurements between the indicated points and do not represent discrete capacitors. Capacitance measurements shall be made with a nominal 1MHz source with the same nominal D.C. level on the +signal and the -signal as specified in table 8. The driving source from the instrumentation shall apply an A.C. signal level less than 100 mV rms.

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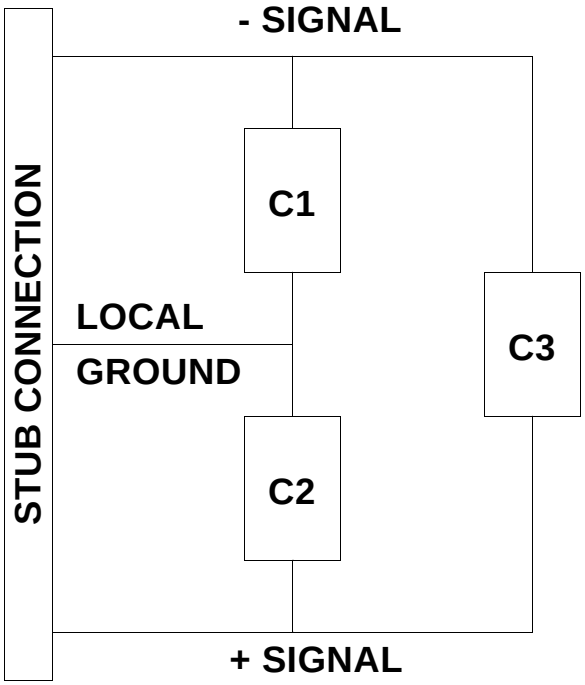


Figure 13 - Capacitive loads

Table 8 - Values for LVD capacitive loads

Capacitance measurement	Maximum (1)	Notes
C1 (pF)	15	@V=0,7 to 1,8 V D.C. -sig/gnd REQ, ACK, DATA and PARITY
C2 (pF)	15	@V=0,7 to 1,8 V D.C. +sig/gnd REQ, ACK, DATA and PARITY
C3 (pF)	8	@V=0,7 to 1,8 V D.C. both - and +sig/gnd V is the same for both sigs ±100mV REQ, ACK, DATA and PARITY
C1 (pF)	25	@V=0,7 to 1,8 V D.C. -sig/gnd all other signals
C2 (pF)	25	@V=0,7 to 1,8 V D.C. +sig/gnd all other signals
C3 (pF)	13	@V=0,7 to 1,8 V D.C. both - and +sig/gnd V is the same for both sigs ±100mV all other signals
| C1 - C2 | (pF)	1,5	REQ, ACK, DATA and PARITY (same signal)
| C1 - C2 | (pF)	3	all other signals (same signal)
| C1(i) - C1(REQ) | (pF)	2	For DATA(i) i = 0-15 and PARITY (i) i = 0,1
| C2(i) - C2(REQ) | (pF)	2	For DATA(i) i = 0-15 and PARITY (i) i = 0,1
| C1(i) - C1(ACK) | (pF)	2	For DATA(i) i = 0-15 and PARITY (i) i = 0,1
| C2(i) - C2(ACK) | (pF)	2	For DATA(i) i = 0-15 and PARITY (i) i = 0,1
note: It is recommended that implementors design capacitive loads to be as small as practical.		

Devices containing the enabled bus termination shall have maximum values 1,5 times the maximums listed in table 8. Differential bus termination circuitry that is not part of a device shall have maximum values 0,5 times the maximums listed in table 8.

2.1.4.1 Management of LVD release glitches

Under some conditions, an LVD signal that transitions from actively negated to released may cause brief pulses to the true signal state. These pulses are called “release glitches” and may last up to a bus settle delay. Requirements are defined in this subclause to avoid adverse affects from release glitches.

SCSI devices shall incorporate the requirements specified in table 9 when using LVD drivers and optionally may incorporate the requirements when using other drivers. The usage of active negation increases cross

talk noise margin and increases the true-to-false transition speed as compared to passive negation.

Table 9 - Glitch management requirements for devices using LVD drivers

Signals	Mode	Active negation	Transmitting device	Receiving device
BSY, SEL, RST	I,T	P		
ACK, ATN	I	R	The initiator shall wait for a BUS FREE phase (note) before releasing the ACK and ATN signals from the actively negated state.	Starting no later than a Bus Settle Delay after releasing the BSY signal, the target shall ignore the ACK and ATN signals until a subsequent connection.
REQ	T	R	The target shall wait 2,5 x (Bus Settle Delay) after releasing the BSY signal before releasing the REQ signal from the actively negated state.	The initiator shall begin to ignore the REQ signal within 1,5 x (Bus Settle Delay) of the transition of the BSY signal from true to false
C/D, I/O, MSG	T	R	After a selection or reselection phase, these signals shall not be released until the BSY signal is released.	No glitch management required.
DATA BUS (SELECTION and RSELECTION phases)	I,T	P	The transmitting device shall release all false data bits during these phases.	No glitch management required.
DATA BUS (During information transfers)	I,T	R	No glitch management required.	No glitch management required.
Key: I = initiator; P = prohibited; R = required; T = target				
Note: BUS FREE phase starts a Bus Settle Delay after the BSY and SEL signals are both false.				

2.1.5 SE/HVD transmission mode detection

Transmission mode detection by LVD SCSI devices of SE and HVD SCSI devices is accomplished through the use of the DIFFSENS line. Requirements for devices and terminators for DIFFSENS are not the same as for "signal" lines because DIFFSENS is driven and detected using its own SE transmission and detection scheme.

LVD termination shall drive the DIFFSENS line as specified in 2.1.5.1 and LVD SCSI devices shall sense the DIFFSENS signal as specified in 2.1.5.2.

Devices and terminators connected to the DIFFSENS line shall comply with the requirements in table 4 and table 5.

2.1.5.1 LVD DIFFSENS driver

The LVD DIFFSENS driver sets a voltage level on the DIFFSENS line that uniquely defines a LVD transmission mode. LVD terminators and multimode terminators (see 2.2.1) shall provide a LVD DIFFSENS driver according to the specifications in table 10.

Table 10 - LVD DIFFSENS driver specifications

Value	max.	nominal	min.	notes
V_O (volts) when I_O = 0 (shorted to ground) to 5 mA	1,4	1,3	1,2	
I_{OS} (mA)	15	5		With TERMPWR at operational levels and V_O = 0.
| Input current D.C.| (µA)	10			With terminator disabled.
Input sink current D.C. (µA) at V_O = 2,75V	200		20	Required to prevent the line from floating and to ensure the HVD DIFFSENS drivers dominate the LVD DIFFSENS drivers.

Note:
- All requirements apply at the terminator bussing connection (see figure 4).
- All measurements per figure 14.

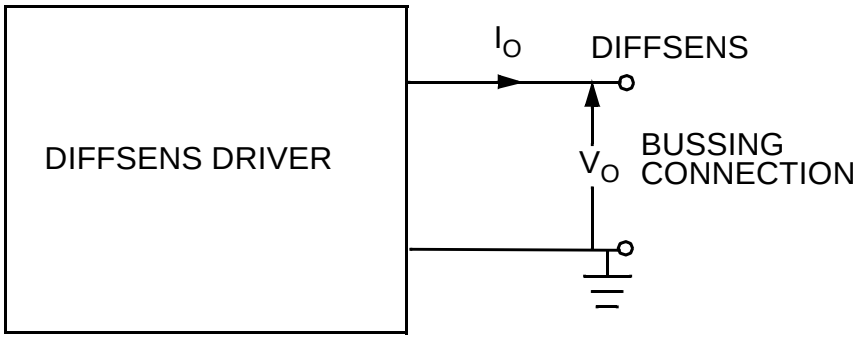


Figure 14 - LVD DIFFSENS driver signal definitions

2.1.5.2 LVD DIFFSENS receiver

LVD SCSI devices shall incorporate a LVD DIFFSENS receiver that detects the voltage level on the DIFFSENS line for purposes of informing the device of the transmission mode being used by the bus. The LVD DIFFSENS receiver shall be capable of detecting SE, LVD, and HVD SCSI devices. Table 11 and figure 15 define the receiver input levels for each of the three modes.

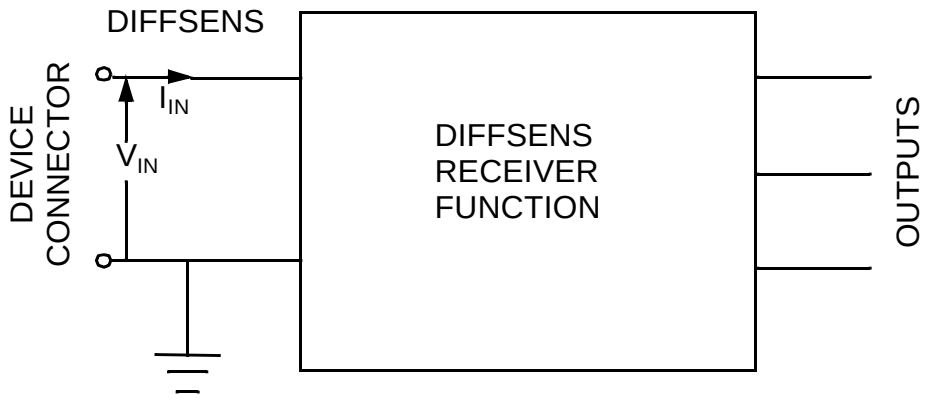


Figure 15 - DIFFSENS receiver function

Table 11 - DIFFSENS receiver operating requirements

V_{in} range	**Sensed differential driver type**
-0,35V to +0,5V	SE
> +0,5V to < 0,7V	indeterminate for detecting a driver type
0,7V to 1,9V	LVD
> 1,9V to < 2,4V	indeterminate for detecting a driver type
2,4V to 5,5V	HVD
Note: Input resistance (Vin/Iin) shall be 200 Kohms to 250 Kohms @ Vin < 2,7V under all conditions of power supply (i.e., power on, power off, power transients) All voltages measured at the device connector with respect to local ground.	

The input resistance requirement is for purposes of providing ground reference if no DIFFSENS drivers are connected to the bus and to ensure that the DIFFSENS receivers do not load the DIFFSENS drivers excessively and to ensure that SE mode is detected.

Devices shall not allow the signal drivers to leave the high impedance state during initial power on until both of the following conditions are satisfied:

a) the device is capable of logical operation for at least 100 ms, and

NOTE 1 - Note: The 100 ms delay allows time for the DIFFSENS pin to connect after the initial power connection (in the case of insertion of a device into an active system), or allows time for the power distribution system to settle.

b) the DIFFSENS mode detected has remained stable for an additional 100 ms after a) is achieved.

A device shall not change its present signal driver or receiver mode based on the DIFFSENS voltage level

unless a new mode is sensed continuously for at least 100 ms.

An example implementation of an LVD DIFFSENS receiver is shown in figure 16. The reference voltage tolerance is greater on the higher voltage reference. This allows a simple resistor divider between V_{CC} and ground for the references. The 100 ms requirement is implemented in logic in this example and is not shown in the figure 16.

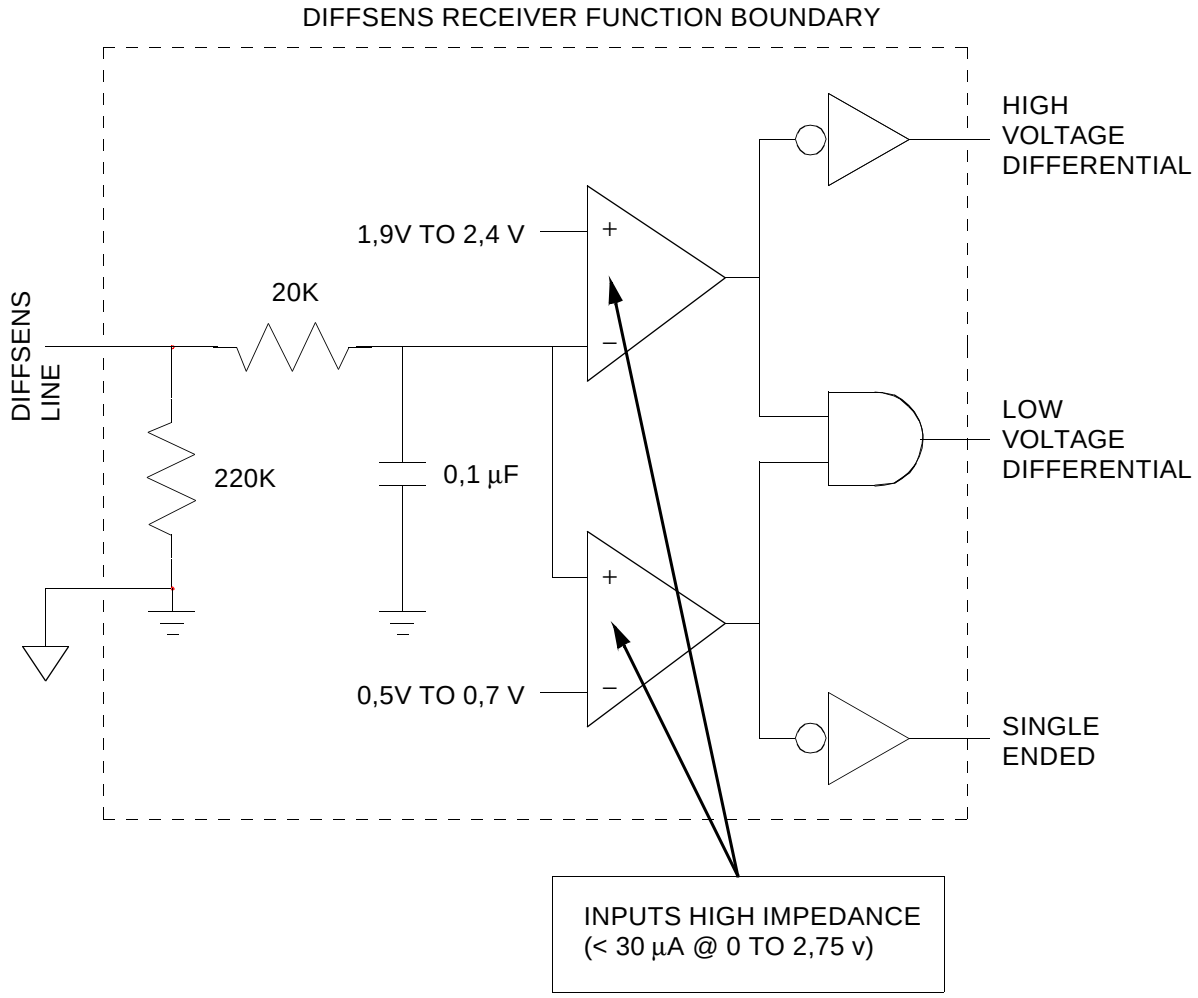


Figure 16 - LVD DIFFSENS receiver example

2.2 LVD/MSE multimode alternative

2.2.1 LVD/MSE multimode termination

Figure 17 shows the architecture of the multimode terminator.

Multimode terminators sense the DIFFSENS line while sourcing the DIFFSENS signal with the LVD levels (see table 10). The DIFFSENS line being grounded indicates that one or more SE SCSI devices or SE terminators are attached to the bus. A multimode terminator shall switch to the termination mode that is appropriate for the bus based on the value of the DIFFSENS input voltage. The appropriate mode is indicated in table 11.

When operating in the LVD mode the requirements in 2.1 and LVD requirements in table 4 shall apply.

When operating in the MSE mode SE termination requirements in 7.1 and MSE requirements in table 4 shall apply.

Multimode terminators are required to provide a ground driver (similar to that described for multimode transceivers) for purposes of establishing a ground reference for the SE transmission lines. The ground driver shall turn on and remain on while the DIFFSENS line indicates SE operation. When turned on ground drivers shall appear resistive with the following performance requirements:

<0,5V @ +5 mA, > -0,5V @ -5 mA.

The requirements for the multimode terminator ground driver are different from those for the multimode transceiver ground driver (see 2.2.4) because the devices provide the bulk of the grounding. Devices may be located far from the ends of the bus where ground references are more important.

NOTE 2 - There is at least one hard ground on the +SIGNAL line when operating in MSE mode (caused by the devices and/or terminators that are single-ended). This hard ground provides a return path for any low frequency currents in the +SIGNAL line.

NOTE 3 - The disabled ground driver capacitance should match the capacitance of the disabled assertion and negation drivers.

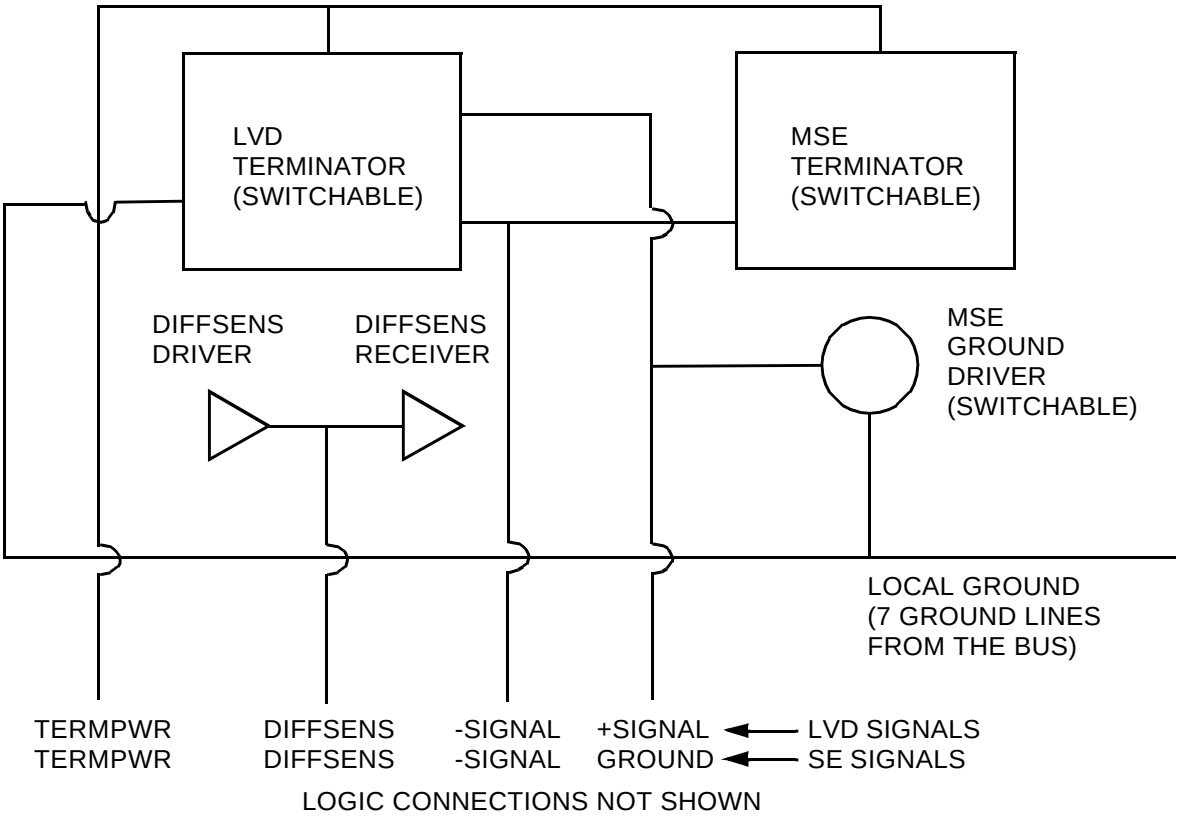


Figure 17 - Multimode terminator architecture

2.2.2 LVD/MSE multimode transceiver characteristics

The architecture for the multimode transceiver is shown in figure 18.

The contact assignments in table 8, table 7, table 6, and table 13 provide compatible alignment of the pins between SE and LVD for all connector alternates. This alignment allows a single interface to supply MSE

and LVD transceivers within the same device. It is not the intent to define a dynamically changing transmission mode but rather to prevent incompatible devices from attempting to interoperate.

The LVD/MSE multimode transceiver shall meet the requirements in 2.1.5.2.

LVD/MSE multimode transceivers shall be set to the appropriate mode by sensing the output of the DIFFSENS receiver. If the DIFFSENS receiver indicates SE the LVD/MSE multimode transceiver shall follow the SE requirements in 7.1 and MSE requirements in table 4. If the DIFFSENS line indicates LVD mode the LVD/MSE multimode transceiver shall follow the requirements in 2.1. If HVD operation is indicated by the DIFFSENS receiver all signals (except DIFFSENS) shall be set to a high impedance state (> 100K ohms to the local ground) (see 2.2.5).

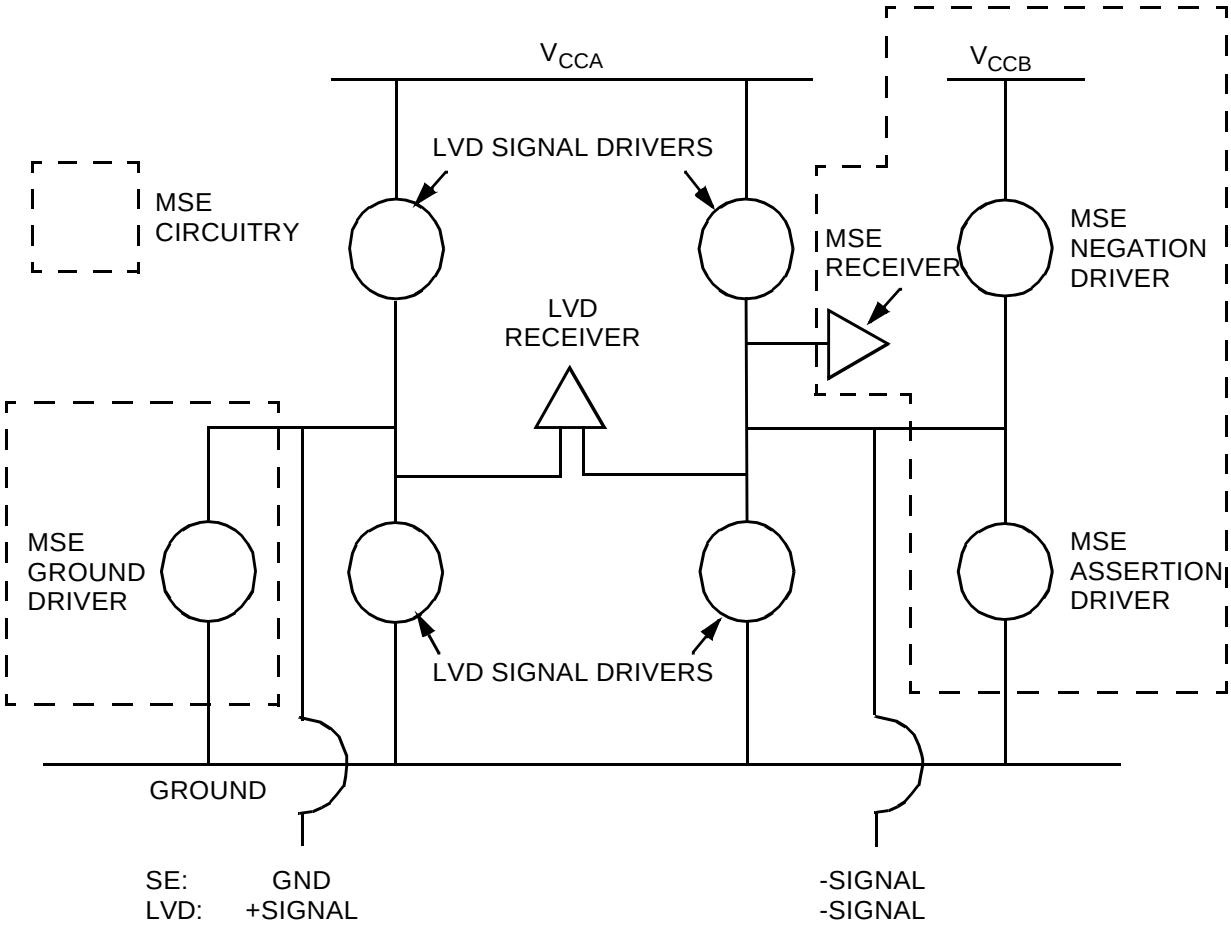


Figure 18 - Multimode transceiver architecture

2.2.3 Power for LVD/MSE multimode transceivers

Power for the differential transceivers may be supplied from a different source than the power for the MSE transceivers. This enables the MSE voltage levels while allowing the differential transceivers to have lower voltages to reduce chip power or for compatibility with low voltage logic levels.

2.2.4 Ground drivers

When using the multimode driver architecture described in figure 18 a MSE driver is required for the ground side of the driver. The ground driver provides the connection to ground for the SE ground line

associated with the SE -signal line. When the MSE alternate is implemented the signal ground connections should be through the ground drivers to allow switching to LVD mode.

When turned on, ground drivers shall appear resistive with the following performance requirements: <0,5V @ +25 mA, > -0.5V @ -25 mA. Ground drivers shall remain on for the entire time the device is powered and is sensing a SE transmission mode from the DIFFSENS receiver. Ground drivers are not required to implement any slew rate controls.

2.2.5 Terminator power

Provision shall be made to provide power from one or more sources to the TERMPWR lines of the SCSI bus. Terminator power shall be supplied through a low forward drop diode or similar semiconductor that prevents backflow of power if one of the sources of TERMPWR is powered-off.

Bus terminators shall be powered from at least one source of termination power (TERMPWR). The TERMPWR lines in the cable are available for distribution of termination power. Direct connection between the TERMPWR source and the individual terminators without using the TERMPWR line is also allowed.

If the TERMPWR source is connected to the cable TERMPWR line, the source shall be isolated in a manner that prevents sinking of current from the TERMPWR line into the TERMPWR source (for example if the TERMPWR source voltage falls below the voltage existing on the TERMPWR line, the TERMPWR source will sink current unless unidirectional isolation is present in the TERMPWR source).

Regulatory agencies may require limiting maximum (short circuit) current to the TERMPWR lines. These requirements generally mandate the use of current limiting circuits and may restrict the number of sources provided for TERMPWR.

The terminator power characteristics, for each terminator, at the terminator shall be as defined in table 12.

Table 12 - Terminator power characteristics at the terminator

Terminator power characteristics	Terminator type						
	SE			LVD	SE/LVD (Multimode)		
	A cable	P cable/Q cable					
		0,2 V dropout regulator					
I_{min} (A) @ V_{min}	0,35	0,6	0,6	0,5	0,65		
V_{min} (V) @ I_{min}	4,0	2,7	4,0	3,0	3,0		
V_{max} (V) @ all conditions	5,25	5,25	5,25	5,25	5,25		
Note: The recommended TERMPWR current limiting is 2,0 amps.							

NOTE 4 - SCSI devices connected with a SE A cable (table 3) are not able to meet the source current

requirements in table 12 unless the TERMPWR conductor size is 0,080 98 mm^2 (28 AWG) minimum because the SE A cable contains only one TERMPWR line.

NOTE 5 - It is recommended that an SCSI device connected with the nonshielded alternative 2 connectors (see 5.1.2) that provide terminator power use keyed connectors to prevent accidental grounding or the incorrect connection of terminator power.

3 LVD System level requirements

The requirements for LVD drivers and receivers in this annex are based on the system level requirements stated in table 13. Some of these requirements are specifically called out in other subclauses while others are derived from bus loading conditions and trade-offs between competing parameters.

Table 13 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V_A (mV)	-115		note 1
V_N (mV)		115	note 1
differential receiver input (mV)	$-V_N$ x 0,25	$-V_A$ x 0,25	figure 45
attenuation (%)		15	note 2
loaded media impedance (ohms)	85	135	note 3
unloaded media impedance (ohms)	110	135	subclause 6.2
terminator bias (mV)	100	125	subclause 7.2.1
terminator impedance (ohms)	100	110	subclause 7.2.1
device leakage (µA)	-20	20	table 23
number of devices	2	16	subclause 4.1.7
ground offset level (mV)	-355	355	note 4

Note:
1 -These limits allow 60 mV base A.C. level and a maximum 55 mV for crosstalk and other non-common mode noise.
2 -Measured from the driver to the farthest receiver.
3 -Caused by the addition of device capacitive load (see annex G for calculations).
4 -This is the difference in voltage signal commons for devices on the bus (see figure 2).

3.1 Driver requirements

The fundamental requirement for a LVD driver is the generation of a first-step differential output voltage magnitude at the driver connections to the balanced media to achieve required minimum differential signals at every receiver connection to the bus. Other characteristics that affect overall noise margin are the common-mode output voltage, the maximum differential output voltage, the driver output impedance, and the output signal wave shape.

The driver requirements are defined in terms of the voltages and currents depicted in figure 41.

3.2 Differential output voltage, V_S

This subclause does not specify requirements for drivers with source impedances less then 1000 ohms.

To assure sufficient voltage to define a valid logic state at any device connection on a fully loaded LVD bus at least a minimum differential output voltage shall be generated. This value shall be large enough that, after allowance for attenuation, reflections, and differential noise coupling, V_S is at least $\pm$60 mV at the device connector to the LVD bus.

The SCSI device shall also comply with the upper limits for the differential output voltages and to the symmetry of the differential output voltage magnitudes between logic states in order to assure a first-step transition to the opposite logic state.

With the test circuit of figure 19 and the test conditions V1 and V2 in table 14 applied, the steady-state magnitude of the differential output voltage, V_S, for an asserted state (V_A), shall be greater than or equal to 270 mV and less than or equal to 780 mV. For the negated state, the polarity of V_S shall be reversed (V_N) and the differential voltage magnitude shall be greater than or equal to 260 mV and less than or equal to 640 mV. The relationship between V_A and V_N specified in table 14 and shown graphically in figure 20 shall be maintained.

The assertion drivers and negation drivers require different strengths to achieve the near equality in V_A and V_N shown in figure 20 because the applied V1 and V2 simulate the effects of the bus termination bias.

Figure 20 shall only apply to drivers with source impedances greater than 1000 ohms.

Table 14 - Driver steady-state test limits and conditions

Test parameter	Test conditions (figure 19)	Minimum (mV)	Maximum (mV)
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted) (note)	V_1 = 0,957 V V_2 = 0,535 V	270	780
	V_1 = 1,949 V V_2 = 1,527V	270	780
$\lvert V_N \rvert$ Differential output voltage magnitude (negated) (note)	V_1 = 0,957 V V_2 = 0,535 V	260	640
	V_1 = 1,949 V V_2 = 1,527V	260	640
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted)	All four above conditions	0,69 x $\lvert V_N \rvert$ + 50	1,45 x $\lvert V_N \rvert$ - 65
Note: The test circuit (figure 20) is approximately equivalent to two terminators creating the normal system bias.			

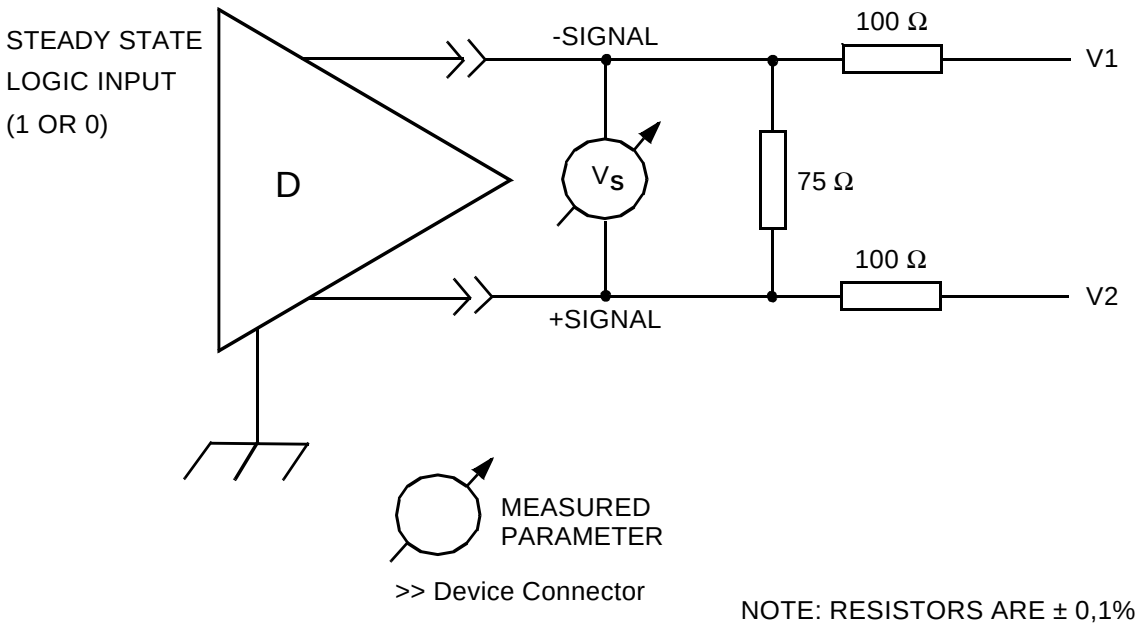


Figure 19 - Differential steady-state output voltage test circuit

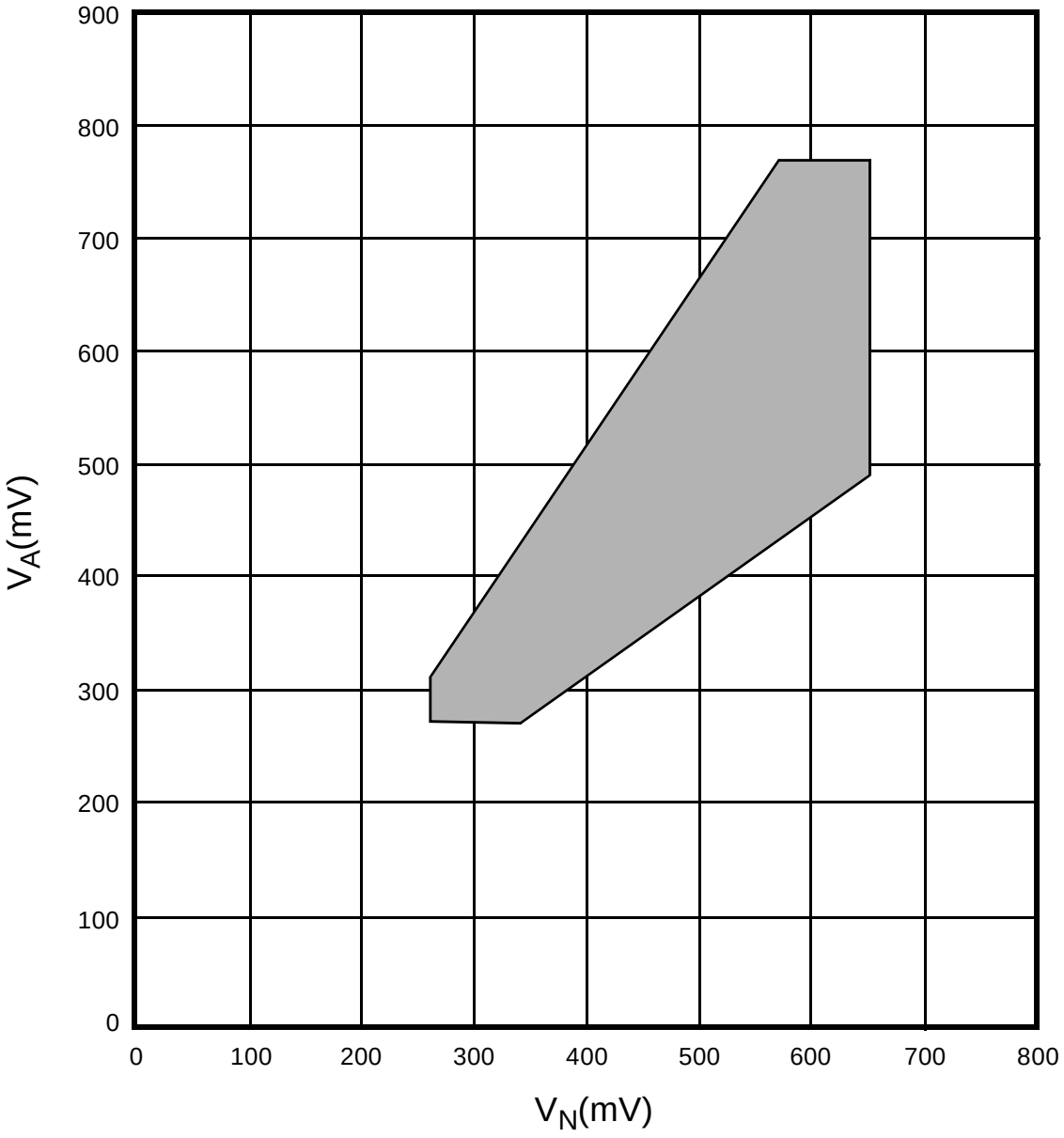


Figure 20 - Domain for driver assertion and negation levels

3.2.1 Offset (common-mode output) voltage, V_{CM}

The steady-state magnitude of the driver offset voltage (V_{CM}), measured with the test load of figure 21 shall be greater than or equal to 0,700 V and less than or equal to 1,800 V for either binary state. The steady-state magnitude of the difference of V_{CM} for one logical state and for the opposite logical state, $\Delta V_{CM,}$ shall be 120 mV or less for all $V_{applied}$ in the range: $0{,}700 \leq V_{applied} \leq 1{,}800$. See figure 22.

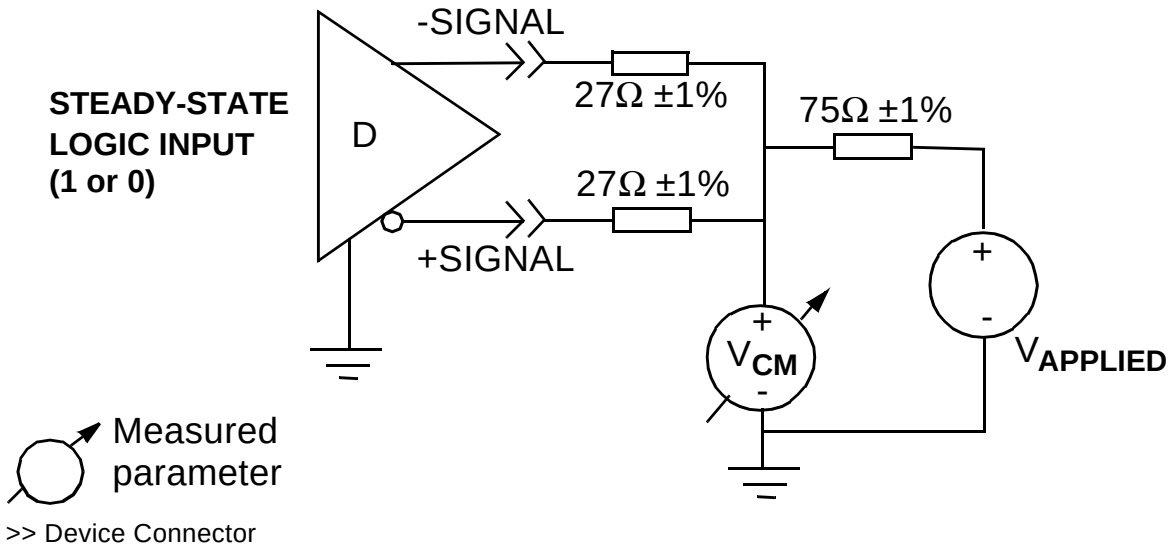


Figure 21 - Driver offset steady-state voltage test circuit

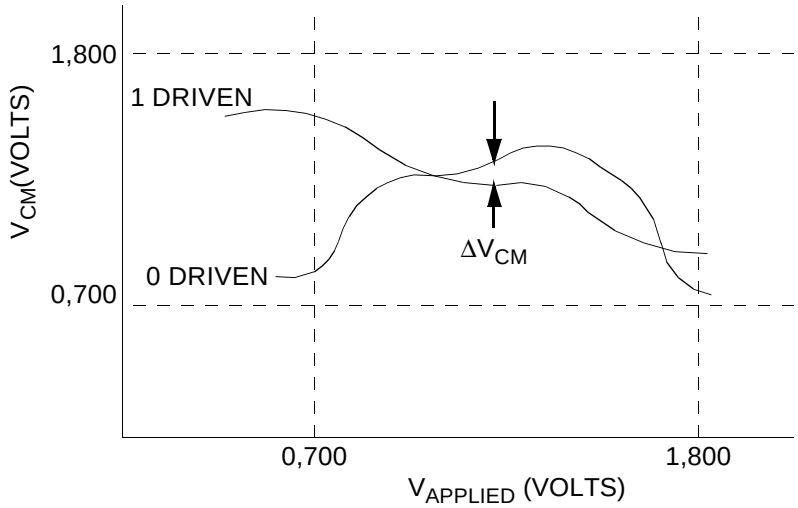


Figure 22 - Common mode output voltage test

0.0.1 Short-circuit currents, I_{O-S} and I_{O+S}

Since an LVD bus allows multiple drivers, the possibility of contention requires a restriction on the power that may be sourced to the bus by a device. This is accomplished with a maximum allowable current from the driver.

With the driver output terminals short-circuited to a variable voltage source, the magnitudes of the currents (I_{O-S} and I_{O+S}) shall not exceed 24 mA for either logical state over the range $0 \leq V_{applied} \leq 2,5$ V. (see figure 23).

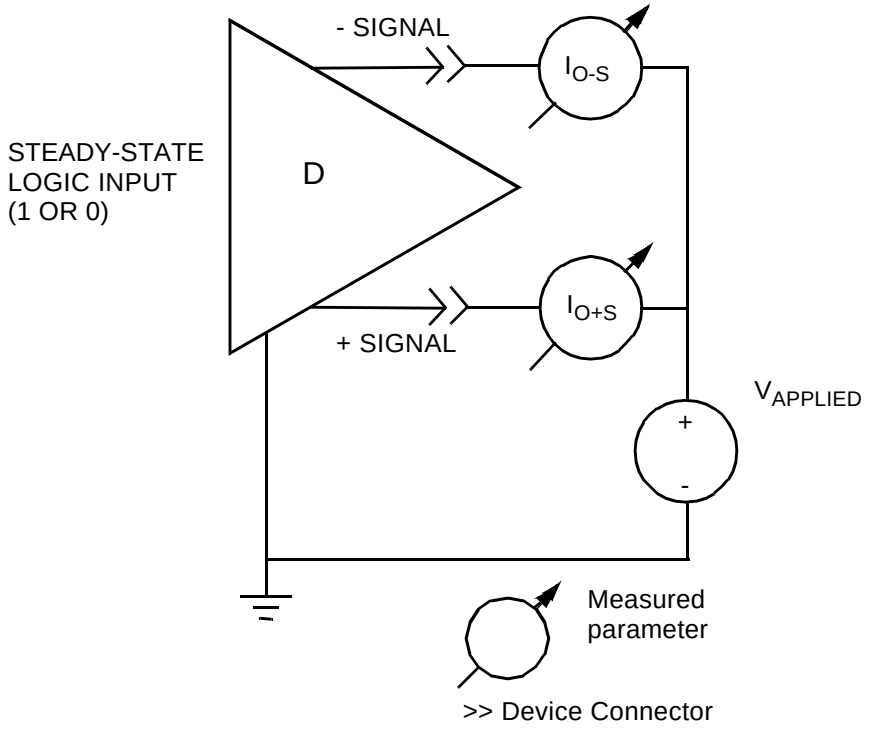


Figure 23 - Driver short-circuit test circuit

3.3 Open-circuit output voltages, $V_{O-(OC)}$ and $V_{O+(OC)}$

To limit the maximum steady-state voltage at any device connector, the voltage between each output terminal of the driver circuit and its common shall be between 0 V and 3,6 V when measured in accordance with figure 24. This requirement shall be met in all logical or high impedance states (0 V $\leq$ $V_{O-(OC)}$ $\leq$ 3,6V and 0 V $\leq$ $V_{O+(OC)}$ $\leq$ 3,6 V). The highest output voltage occurs with no output current.

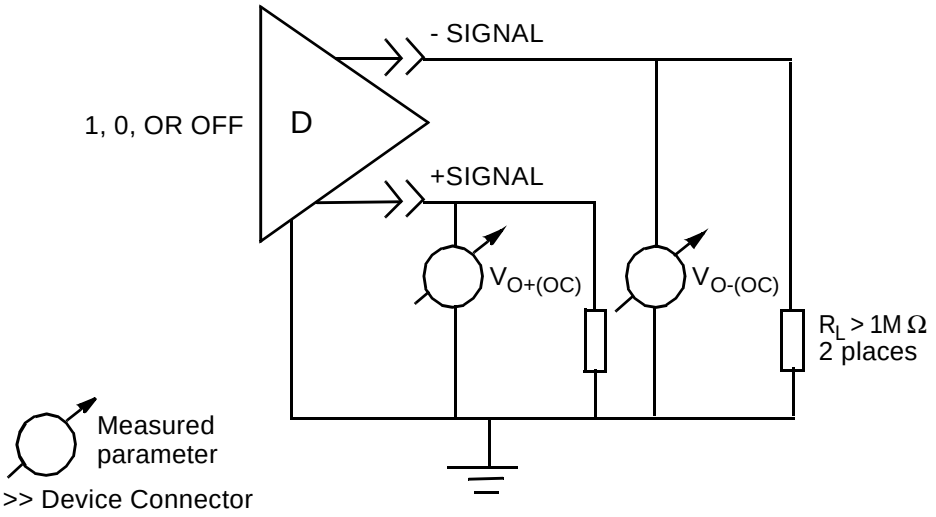


Figure 24 - Open-circuit output voltage test circuit

3.4 Output signal waveform

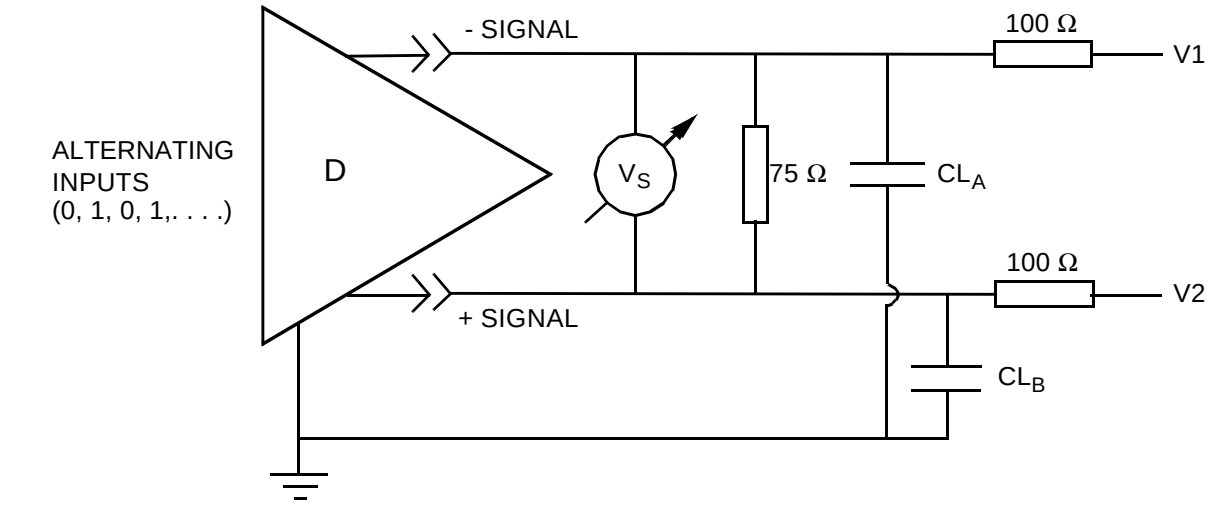
The differential output rise or fall time of a driver is specified since they influence the timing measurements and stub lengths of an LVD interface. Excessive over and under shoot of the output signal may cause electromagnetic emissions or false logic state changes.

During transitions of the driver output between alternating logical states (one - zero, zero - one, one - off, off - one, zero - off, off - zero), the differential voltage measured with the test circuit of figure 25 and table 15, shall be such that the voltage monotonically changes between 0,2 and 0,8 of the steady-state output, V_{SS}. V_{SS} is defined as the voltage difference between the two steady-state values of the driver output (V_{SS} = $|V_A| + |V_N|$) (See figure 26 and table 14). V_{SS} is expected to be different for different transitions.

The output signal rise or fall times (see t_r in figure 26) between 0,2 and 0,8 of V_{SS} shall be greater than or equal to 1 ns.

The slew rates specified above are requirements for a driver when using the LVD test circuit in figure 25. They are not the observed rise or fall rates on an actual SCSI bus.

Measurement equipment used for rise and fall rate testing shall provide a bandwidth of 2 GHz minimum.



Notes:

a) Resistors are ±1% and surface-mount metal film type.

b) CL_A and CL_B are 5 pF ±0,2 pF and include the instrumentation capacitance.

c) The longest physical dimension between the device connector pins and any test circuit component shall be no greater than 0,1 meter.

d) V1 and V2 are applied voltages from a source having a source impedance of less than 5 Ω from 0 Hz to 40 MHz.

Figure 25 - Differential output switching voltage test circuit

Table 15 - Driver switching test circuit parameters

Test condition (see figure 25)	V1	V2
Low common-mode voltage	1,375 V	0,807 V
High common-mode voltage	1,693 V	1,125 V

The signal voltage shall comply with the requirements shown in figure 26.

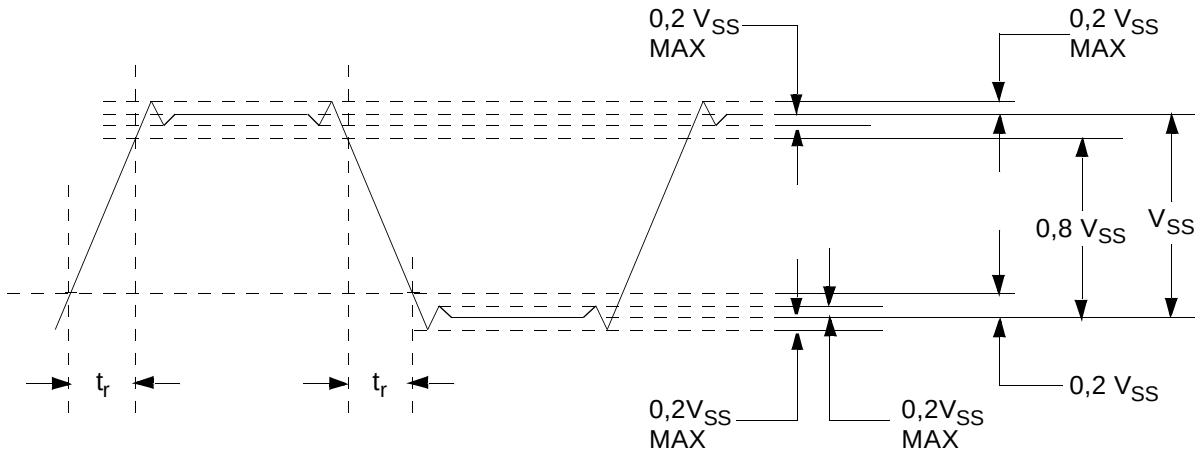


Figure 26 - Driver output signal waveform

3.4.1 Dynamic output signal balance, $V_{CM(PP)}$

A mismatch in the magnitude of rate at which the voltage changes at the - signal and + signal connector pins, results in a common-mode AC signal. This may cause electromagnetic emissions from the media, excursions outside the receivers' common-mode input voltage range, and/or differential noise.

During transitions of the driver output between any state transition of high-to-low, low-to-high, high-to-off, off-to-high, low-to-off, or off-to-low, the voltage (V_{CM}) measured with the test circuit shown in figure 27, shall not vary more than specified in table 16 as $V_{applied}$ is varied over the range $0,700 \leq V_{applied} \leq 1,800$. Measurement equipment used for dynamic signal output balance testing shall provide a bandwidth of 400 MHz minimum. The requirements in this subclause apply only to the applicable state transitions.

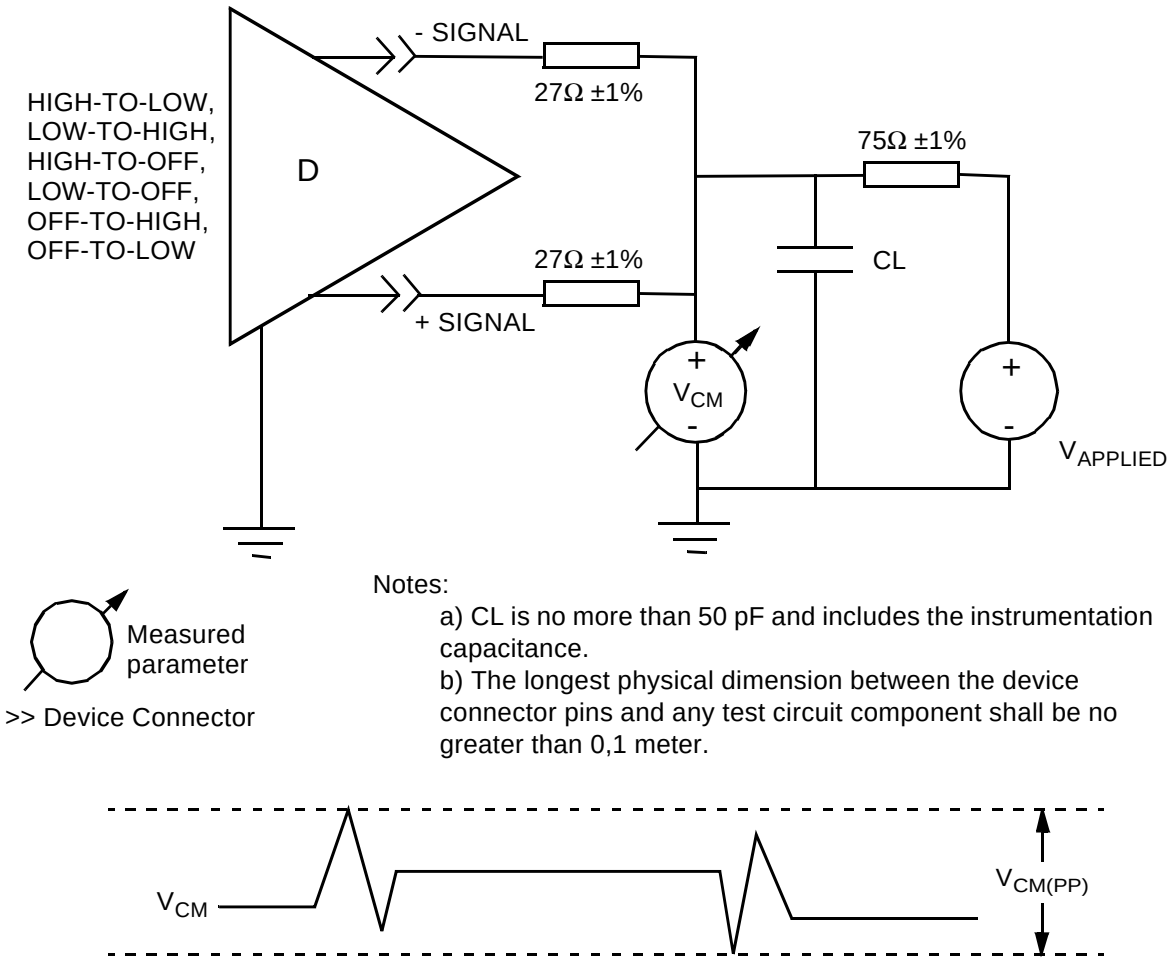


Figure 27 - Driver offset switching voltage test circuit

Lower values of $V_{CM(PP)}$ have lower EMI risk.

Table 16 - Dynamic output balance limits

Transition	$V_{CM(PP)}$ mV max
high-low	120
low-high	120
high-off	400
low-off	400
off-high	400
off-low	400

4 Receiver characteristics

A receiver indicates the logical state of the LVD bus as defined by the differential voltage that exists at the device connector. A minimum steady state differential voltage defines the logic state. The receiver shall detect this difference over the allowable common-mode input voltage range as determined by the driver and terminator output offsets and ground difference voltages.

Table 17 defines the voltages and currents for the requirements in this subclause.

4.1 Receiver steady state input voltage requirements

Within the common-mode input voltage range (V_{CM}), (figure 42) 0,700 V $\leq V_{CM} \leq$ 1,800 V a LVD receiver shall indicate the logical states shown in table 17 with V_{IN} within the ranges shown in table 17.

Table 17 - Receiver steady state input voltage ranges

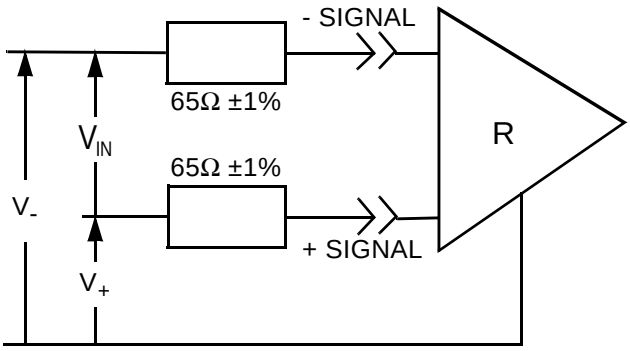
Input voltage range steady state (V_{IN})	Receiver detects
-3,6 V $\leq V_{IN} \leq$ -0,030 V	1
0,030 V $\leq V_{IN} \leq$ 3,6V	0

4.2 Compliance test

Compliance to the requirements in 4.1 shall be verified with the input voltages of table 18 and the circuit of figure 28.

Table 18 - Receiver minimum and maximum input voltages.

Applied voltages (input voltage referenced to circuit common) (see figure 28)		Resulting differential input voltage	Resulting common-voltage input voltage
V_-	V_+	V_{IN}	V_{CM}
0,715	0,685	0,030	0,700
0,685	0.715	-0.030	0,700
1,815	1,785	0,030	1,800
1,785	1,815	-0.030	1,800
3,600	0,000	3,600	1,800
0,000	3,600	-3,600	1,800
3,955	-0,355	4,310	1,800
-0,355	3,955	-4,310	1,800



>> Device Connector

Figure 28 - Receiver input voltage threshold test circuit

0.0.2 Receiver setup and hold times

Figure 45 and figure 51 define the receiver setup and hold times.

NOTE 6 - Dynamic testing is required to verify these timings.

4.3 Transceiver characteristics

4.4 Transceiver output/input currents, I_{I-L} and I_{I+L}

The requirements in this clause apply as a test method to ensure compliance with table 22 and table 23. With the transceiver in an off condition (i.e., not transmitting) and the + and - signals connected to a variable voltage source, $V_{applied}$, the output leakage currents I_{I-L} and I_{I+L} shall not exceed the applicable values in table 23 over the range 0,00 V ≤ $V_{applied}$ ≤ 3,6 V (see figure 29). The maximum applicable current from table 23 is I_{max}.

These measurements apply with the transceiver's power supply in both power-on and power-off conditions.

$| I_{I-L} | < I_{max}$

$| I_{I+L} | < I_{max}$

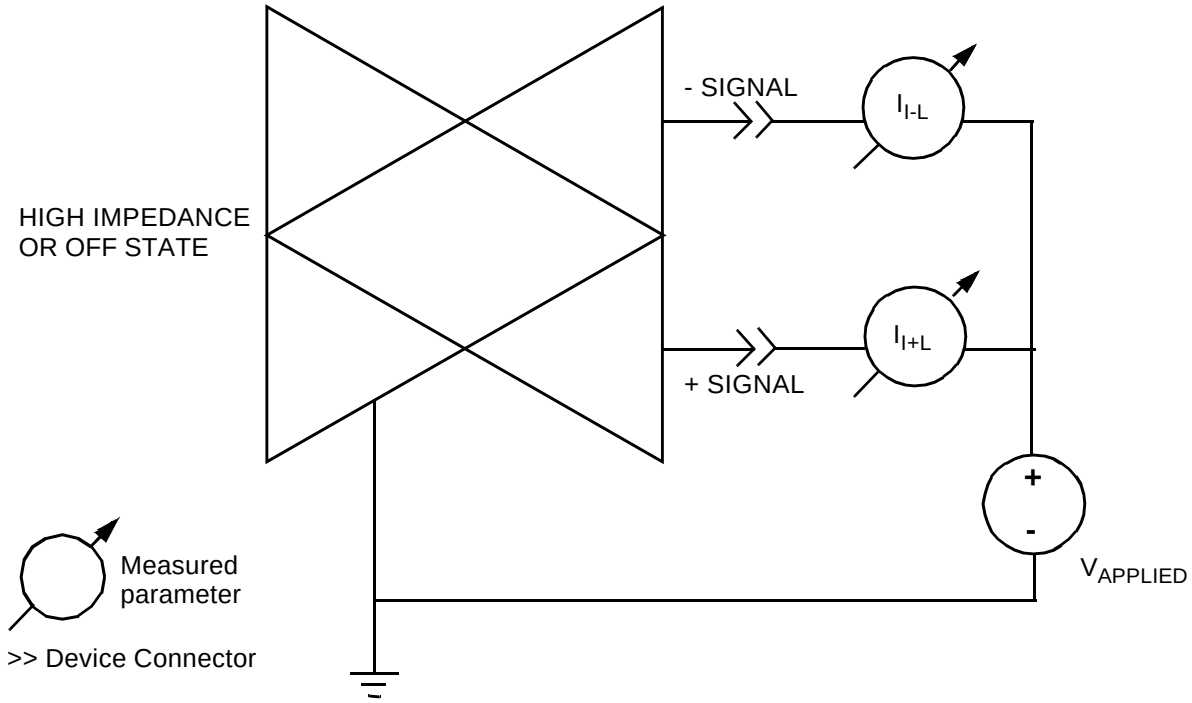


Figure 29 - Transceiver off-state output current test circuit

4.5 Transceiver maximum input voltages

See table 22 and table 23.