# Fast 80ish Proposal

- Completes major items for SPI-3

  but leaves a lot of detailed technical work to finish

- Assumes FDDI / FC / Packetized CRC algorithm if enabled by negotiation (See 98-144 CRC for Data Phases)
- Uses Double Clocking
- Maintains compatibility with LVD cable plant
- Maintains downward compatibility
- Evolutionary step for the silicon design

# Fast 80ish Proposal

- Allows additional options for higher transfer rates and/or additional margin
- Optional pre-emphasis for ISI compensation
- Optional one way mode for reduced crosstalk if enabled by negotiation

# Optional One-Way Mode

- For Data IN uses REQ to clock the data

  Initiator uses ACK as a pause signal

  Offset negotiation applies after ACK asserted for pause

  ACK resumes prior definition after last byte transferred

- For Data OUT uses ACK to clock the data

  Target uses REQ as a pause signal

  Offset negotiation applies after REQ asserted for pause

  REQ resumes prior definition after last byte transferred