

Date: Jan 14, 1998

To: T10 Committee (SCSI)

From: George Penokie (IBM)

Subject: CRC on Existing SCSI Parallel Protocol

This proposal is for a method of incorporating CRC on the existing SCSI parallel protocol. The CRC proposal incorporates the following:

- a) The existing 32-bit fibre channel CRC generation algorithm.
- b) The CRC is attached to the end of each CRC interval of data transferred during read/write commands.
- c) A target device shall disconnect only at CRC interval boundaries if CRC is enabled.
- d) Parameter and sense data has the CRC attached at the end of transfer.
- e) The use of CRC and CRC interval is negotiated with the IUTR message.
- f) For fixed block devices the number of pad bytes at the end of the CRC interval is negotiated with the IUTR message
- g) Errors detected by CRC are handled by the detecting device prior to releasing the bus. Except in cases where data transfers are ended by a phase change in which case the any errors must be detected before the next phase begins.
- h) The allocation length field and transfer length field in the CDB does not include the CRC bytes.
- i) CRC intervals are multiples of four.

The CRC interval is the data length for read and write operations over which the CRC is calculated and transmitted. The interval value is a multiple of four to work correctly with 16-bit double-clocked implementations. The CRC interval is negotiated with the IUTR message if the CRC is enabled. A 2-byte field in the IUTR message would be used with the value in the field multiplied by four to get the CRC interval. For fixed block devices the interval should be equal to the block size.

The CRC for parameter and sense data includes all the data transferred with the CRC being attached at the end of the data.

Data that is not a multiple of four is padded with bytes of zero value. For fixed block devices the number of pad bytes is a negotiated with the IUTR message.

For variable block devices in which the data transfer does not end on a CRC interval should have the CRC bytes attached on a divisible four boundary at the end of the transfer.

Example: A REQUEST SENSE command is issued with an ALLOCATION LENGTH of 64 bytes. The target returns 18 bytes of sense data, 2 pad bytes, and 4 bytes of CRC. The initiator knows that there are 18 valid bytes of data out of the 20 returned because of the ADDITIONAL SENSE LENGTH in the sense data.

Example: A READ command is issued to a tape device with the SILI bit set. If the target ends the data transfer on a CRC interval no further action is taken. If the target ends the transfer with a non-divisible by four number of bytes transferred it will send an IGNORE WIDE RESIDUE message to inform the initiator of the number of pad bytes.

If the target detects a CRC error then the target shall do the same error recovery currently defined for parity errors.

If no error is detected, the target shall complete the current command if all data has been transferred, resume the current transfer, or issue a SAVE DATA POINTERS-DISCONNECT message sequence and transition to bus free phase.

If the initiator detects a CRC error then the initiator shall do the same error recovery currently defined for parity errors.

During the DATA OUT phase, a target shall complete the CRC check before changing to a new phase. During DATA IN phase, an initiator shall complete the CRC check before asserting the ACK signal for the first REQ after leaving the DATA IN phase. The initiator shall assert ATN by this time to indicate its intent to send an INITIATOR DETECTED ERROR message. It is recommended that the initiator receiving data perform the CRC check before releasing the ACK signal of the last byte(s) transferred of a DATA IN phase.

Note: The initiator can perform the CRC check before releasing ACK in cases where the number of bytes transferred is known and the transfer ends on a CRC interval boundary. In the case where the initiator has requested an Allocation Length of data or is transferring data with the SILI bit set (in a tape device) the initiator doesn't know the end of data until the phase change occurs.