To: T10 Membership
From Walter Bridgewater
Subject: Bias Reduction - 3/98
Date: March 16, 1998

Rule 1: All fast-40 drivers will be for asymmetrical, as is.
Rule 2: All fast-80 drivers will be symmetrical for fast-80 to fast-80 device transfers during data phase. Drivers will be asymmetrical whenever talking to an fast-40 device.
QUESTION? Should fast-80 devices transferring data between each other in data phase switch back to asymmetrical mode if they end up running at slower speeds? Is this a speed based thing or an fast-80 based ability? We can do whatever works out the best.
Proposition: Remove the bias from the terminators for fast-80 and have the host or the target supply the bias, and be able to turn it off for data phase.

Table 1: Convert fast-80 terminators to non-biased

TAR-GET	HOST	MEGA TRANS-FERS SPEED	BOTH BIASED	ONE BIASED	NONE BIASED
fast-40	fast-40	40mhz	original format	very problematic	very problematic
fast-40	fast-80	40mhz	original format	host adds 1x additional bias	host adds 2x additional bias
fast-80	fast-40	40mhz	original format	target adds 1x additional bias	target adds 2x additional bias
fast-80	fast-80	80mhz	may limit speed 40mhz, host adds bias cancella-tion	may limit speed 40mhz, host adds 1/2x bias can-cellation	host adds 2x bias when not in sync mode, full speed operation

Rule 3: Keeping Rules 1 & 2 and biased termination, all fast-80 receivers, at the fast-80 speed of 80 mega-transfers per second, will take care of the bias during data phase, since for Rule 2, the drivers will be symmetrical. Note: can this apply to fast-80 to fast-80 transfers at any speed or will apply only at top speed. The drivers and receivers need to have the same rules on this.

The receivers may cancel the bias, just the same as an output driver can do it. Other means may also be possible. In an adaptive approach to bias cancellation, the receiver input offset voltage can be nulled out. Also, some means of having an offset in the receiver may be possible.

Proposition:

It will be the job of the receiver to counter-act the termination bias.

Table 2: fast-80 receivers do bias cancellation

TARGET	HOST	MEGA TRANSFERS SPEED	BOTH BIASED
fast-40	fast-40	40mhz	original format, driver may use bias cancellation
fast-40	fast-80	40mhz	original format, driver may use bias cancellation
fast-80	fast-40	40mhz	original format, driver may use bias cancellation
fast-80	fast-80	80mhz	symmetrical driver, receiver adds bias cancellation

Advantages

- Remove power from the driver, as receivers are generally <40% of driver power. Allows driver to operate at higher voltage swing to bias voltage ratios
- Frees up the bias cancellation circuit in the driver so that it can be used to make a variable strength driver. Note: variable strength drivers may suffer from some of the same disadvantages as an asymmetrical driver.
- Allows innovation in the way bias cancellation is done, such that you could possibly achieve the same results if bias was removed from the terminator.

Issues

- Setting aside time for adaptive bias cancellation. This time could also be used in the future for cable de-skewing and capacitance balancing. This could be done by only selecting yourself on the bus.
- When exactly do you turn on the bias cancellation for the receiver? One way, require that ACK & REG go from Z-state to negated 100ns after any command phase that leads to data-in phase, then 200ns after that, turn on the bias cancellation. You would have at least 100ns before data in phase begins. Bias cancellation could be turned on at this time too, or earlier if you wanted.

Open circuit LVD driver voltage reduction to 2.5 volts

- 3.6 volts will be too high for future IC process.
- Lower voltages reduce power or allow larger voltage swings for the same power or both. Larger voltage swings minimizes the termination bias/driver-receiver cancellation mismatch offsets. Since we can't find any reasonable way to eliminate the termination bias, this is still an important issue.

OR, reduce to 2.2 volts and move the common mode center from 1.25 volts to 1.1 volts.

- Still has common mode range overlap with fast-40

Create policy of reducing common mode center point and open circuit voltage every generation so that only 1 generation at a time is obsoleted each time a new lower voltage generation is introduced. i.e. slowly crank it down.
Wouldn't it be nice if we didn't have to use "high" transistors in the interface circuits!

Table 3: IC feature size & voltages, possible future SCSI speeds

SCSI generation	Mega-transfers speed	Last voltage compatible generation	Doable IC feature size / Vcc voltage	Open circuit voltage
fast-40	40 MT		0.5u / 5.0v	3.6
fast-80	80 MT		0.35u / 3.3v	2.2 / 1.5
f160	160 MT	fast-40[1]/ fast-80	0.25u / 2.5v	2.0[1] / 1.5
f240	240 MT	fast-40[1]/ fast-80	0.18u / 1.8v	1.8[1] / 1.5
f320	320 MT	fast-80[1]/ fast-80	0.15u / 1.5v	1.5[1] / 0.8
f480	480 MT	f160[1] / f320	0.12u / 1.2v	1.2[1] / 0.8
f640	640 MT	f240[1] / f320	0.10u / 1.0v	1.0[1] / 0.8
f960	960 MT	f320[1] / f320	0.08u / 0.8v	0.8

NOTE 1, requires high voltage transistors for LVD input receiver or output driver, or both