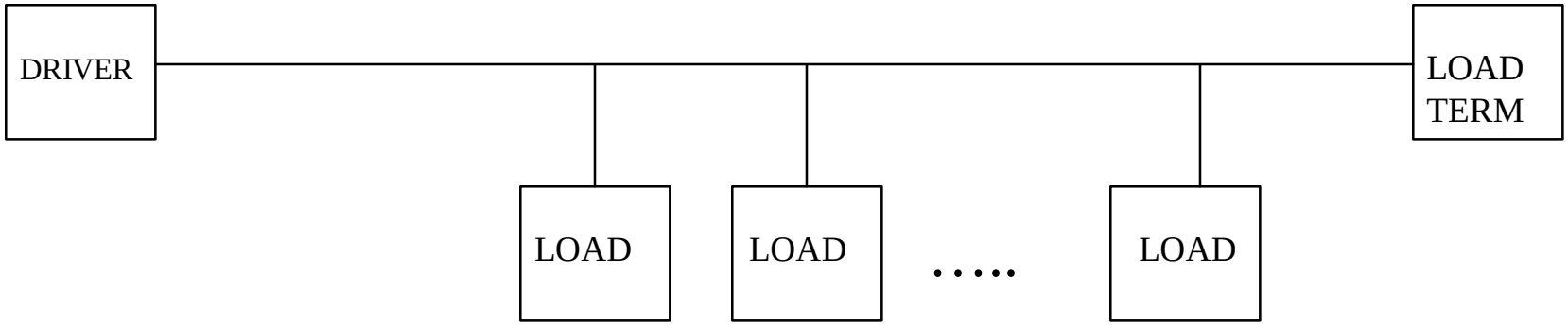
To: **SPI-3 Physical Working Group**
From: **Vincent Bastiani (**vince_bastiani@corp.adaptec.com**)**
Subject: **Initial test results on dual-edge clock signals**
Date: **Tuesday, December 02, 1997**

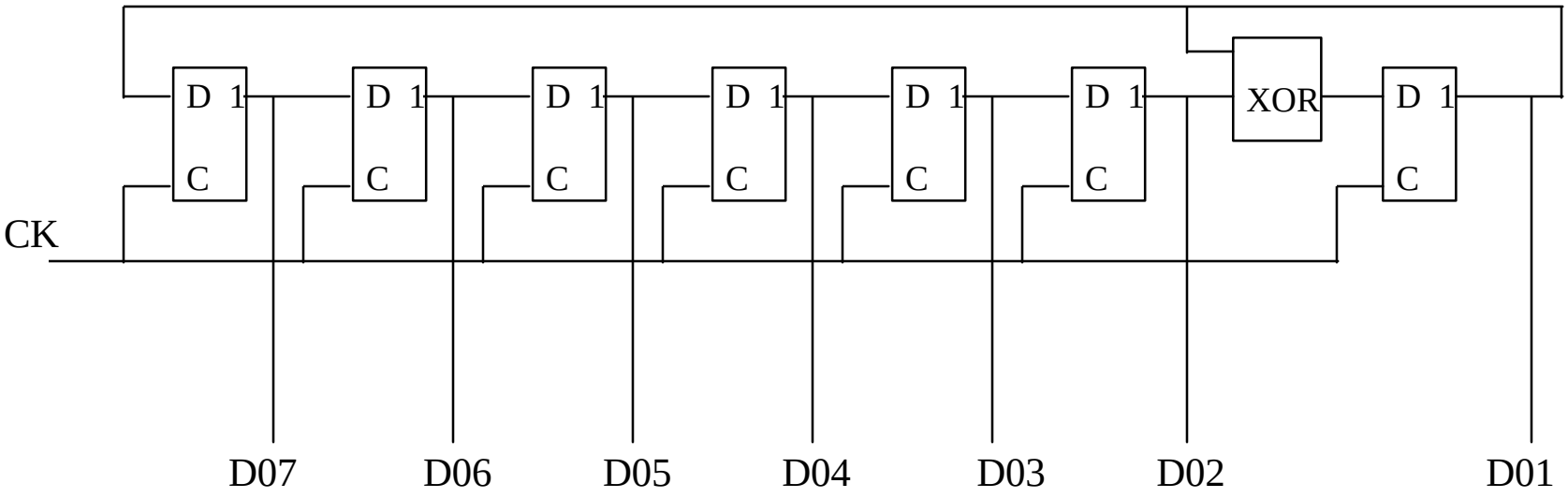
The presentaion on dual-edge clock signals follows.

TEST SETUP

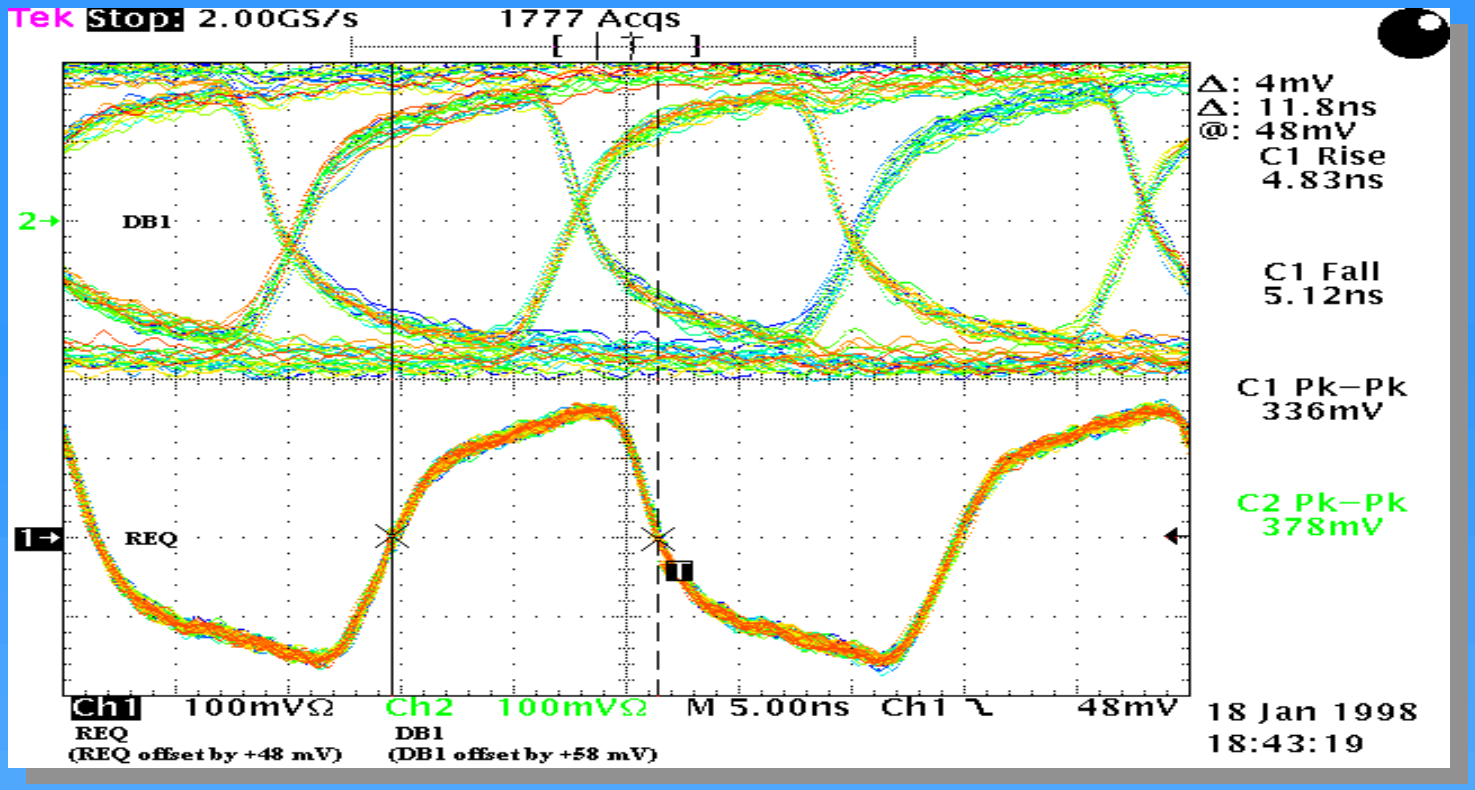
- Data and Req signal driven as in dual edge
- Data is pseudo random pattern of 127 bits with run length of 7
- All lines driven with same pattern but different phase (except D0)
- Various loaded cables used
- Signal monitered at different positions
- Data not checked if received correctly but observed eye pattern at each device.

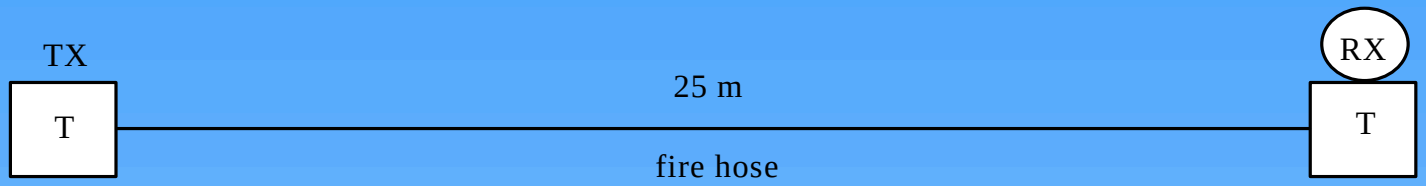


- REQ and DATA Monitered
- Driver is 0.35 micron design used in Adaptec Target Ultra 2 chip
- Drive and Bias level nominal



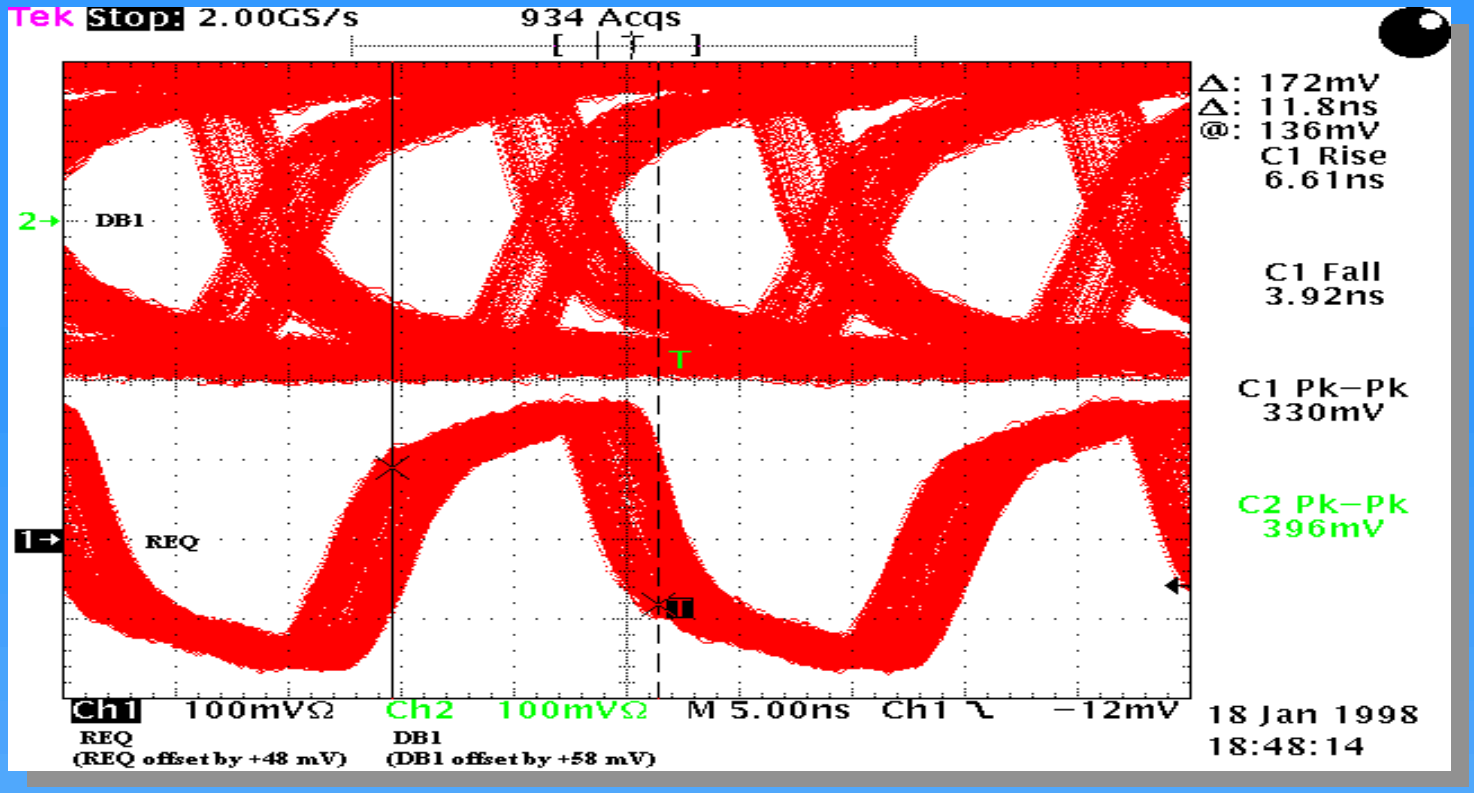
D00 IS SQUARE WAVE AT BIT RATE

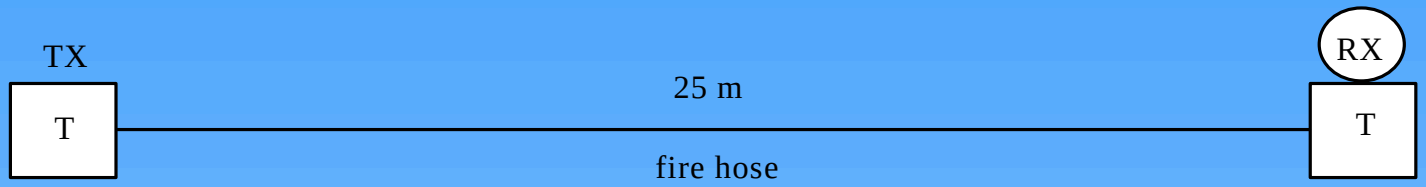




Note:
1) Termination =100
2) DB1 is psuedo-random data

"Eye pattern for 25 m point-to-point configuration"
(trigger at center of REQ)





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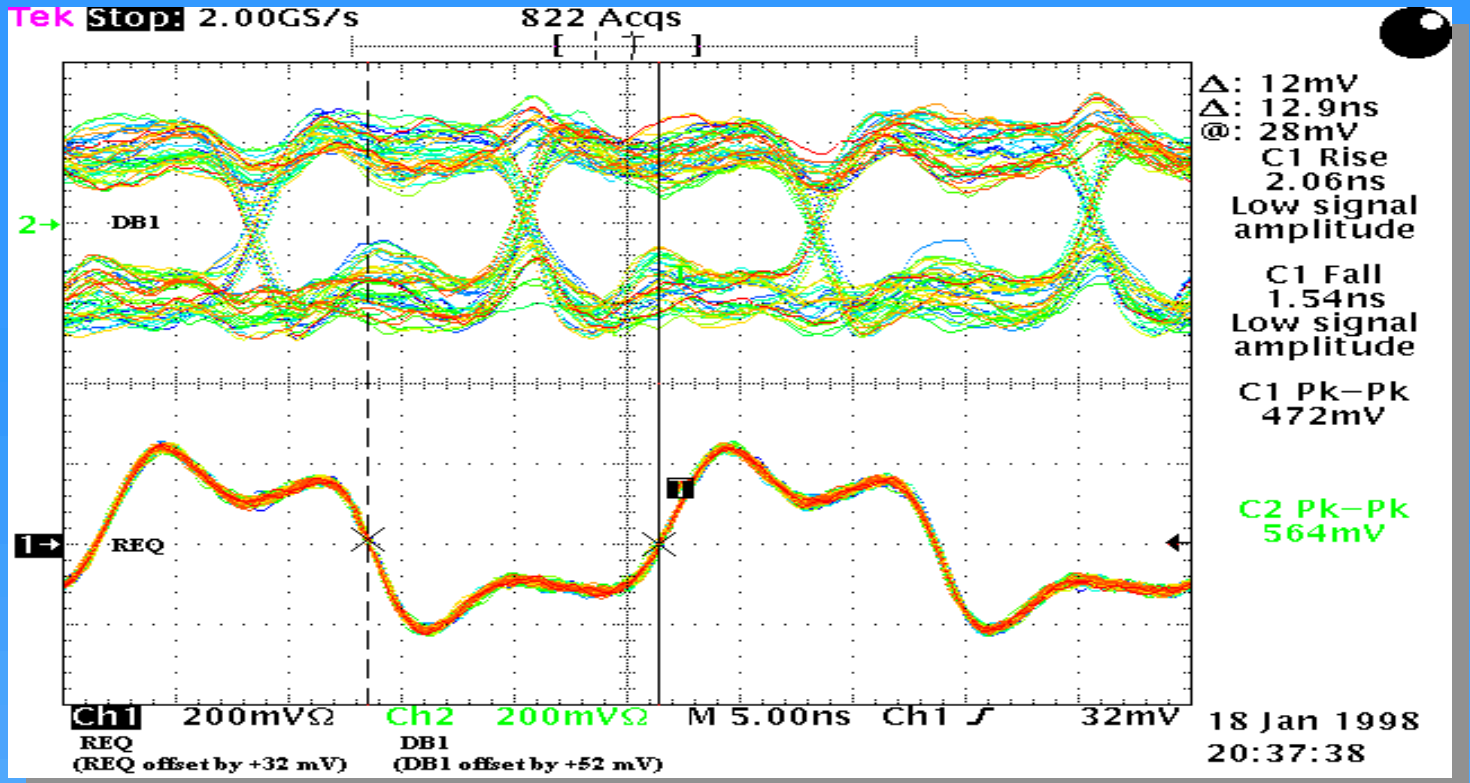
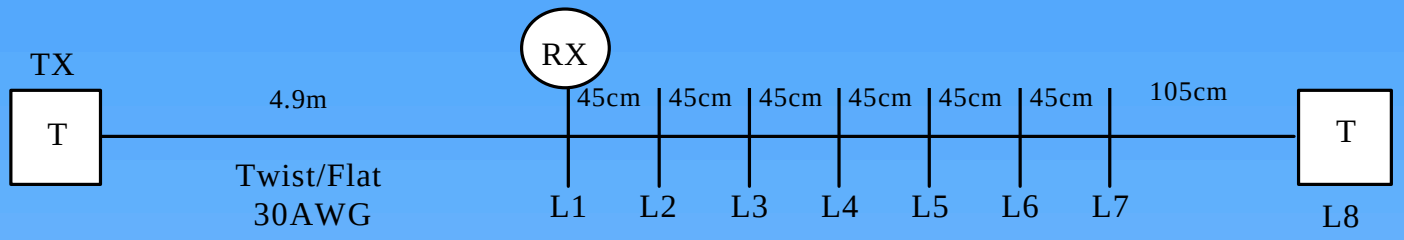
"Eye pattern for 25 m point-to-point configuration"
(trigger +/- 60 mV from center of REQ)





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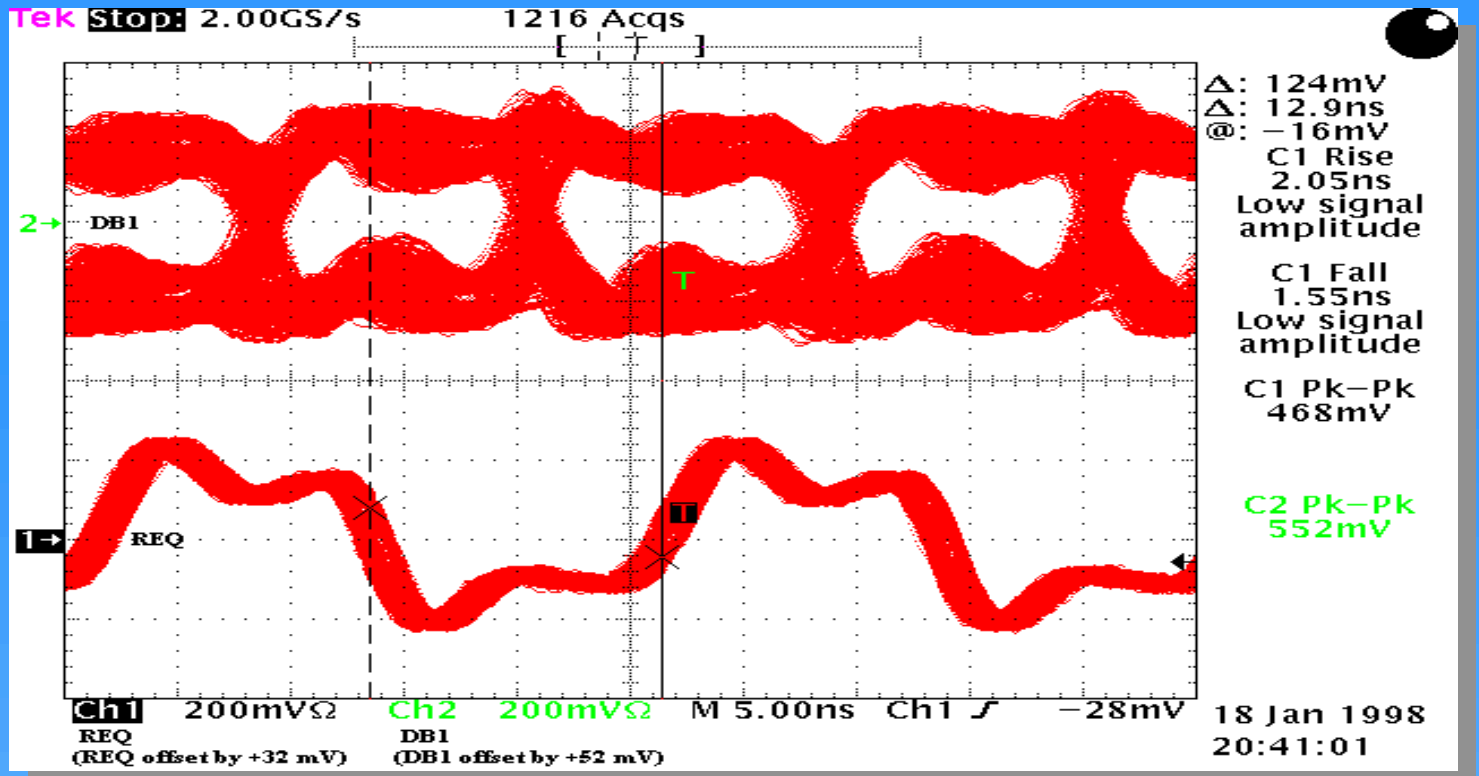
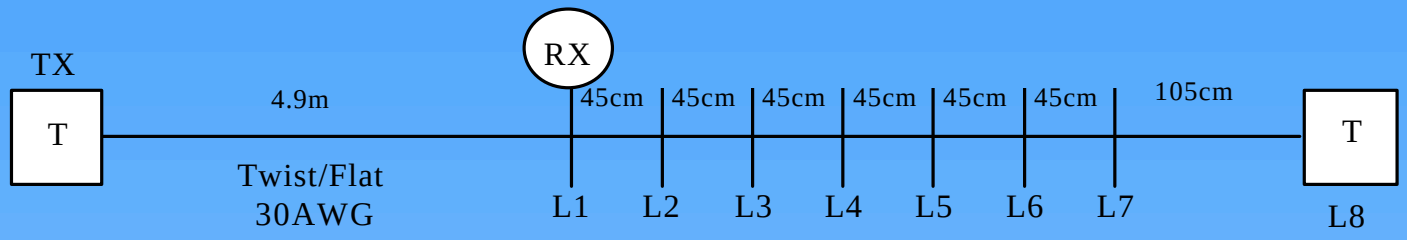
"Eye pattern for 8 m multi-drop configuration"
(trigger at center of REQ)





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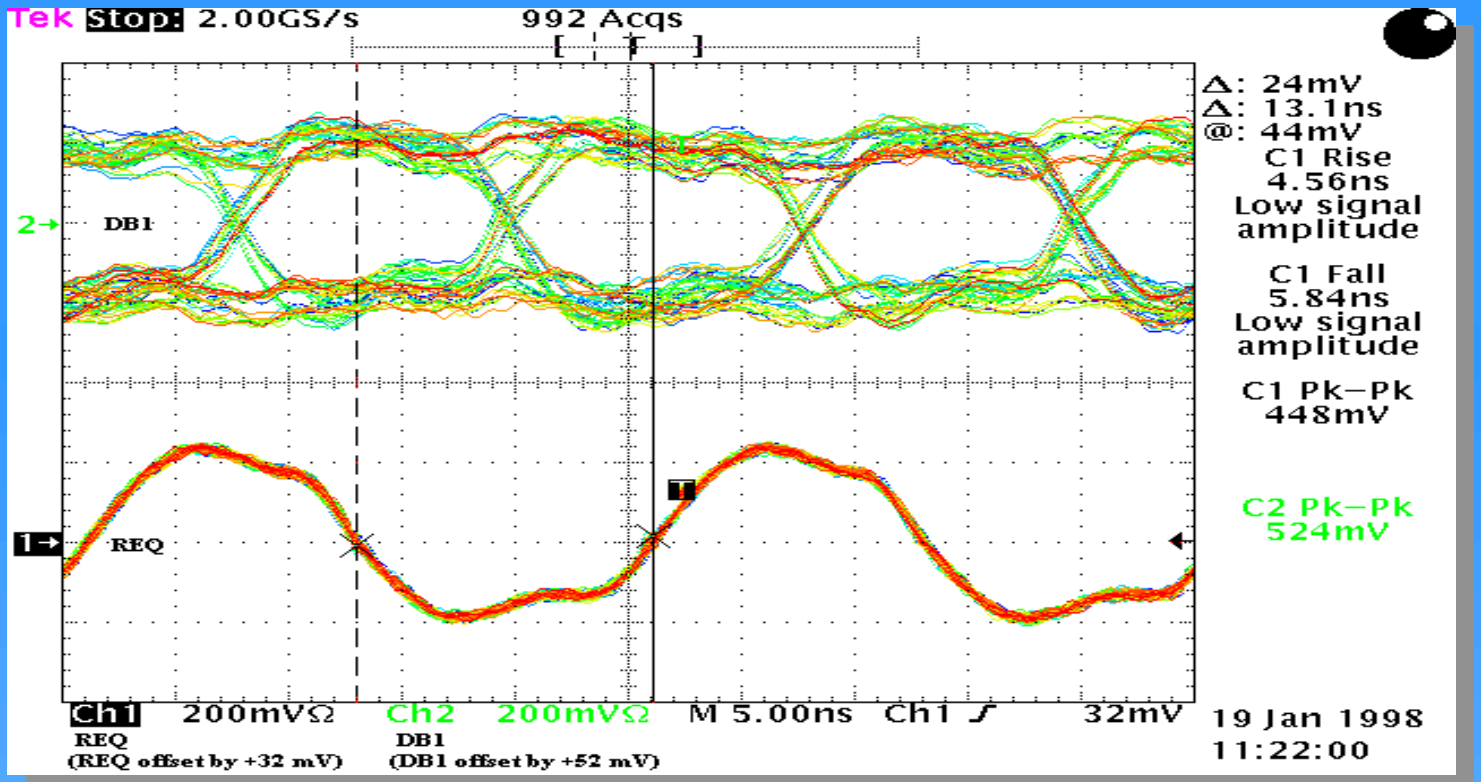

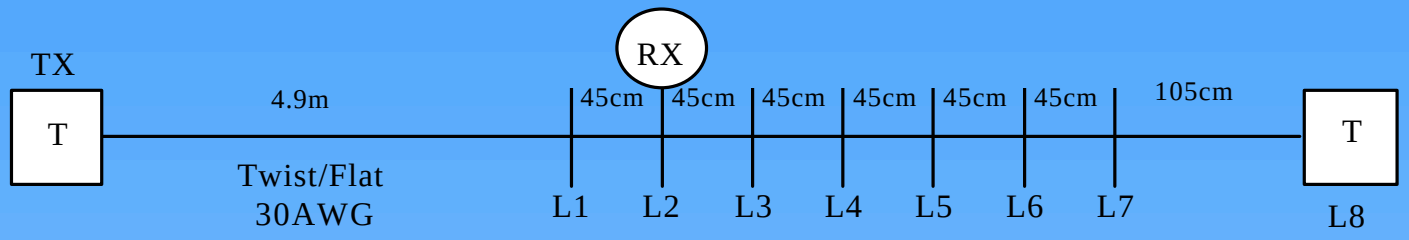

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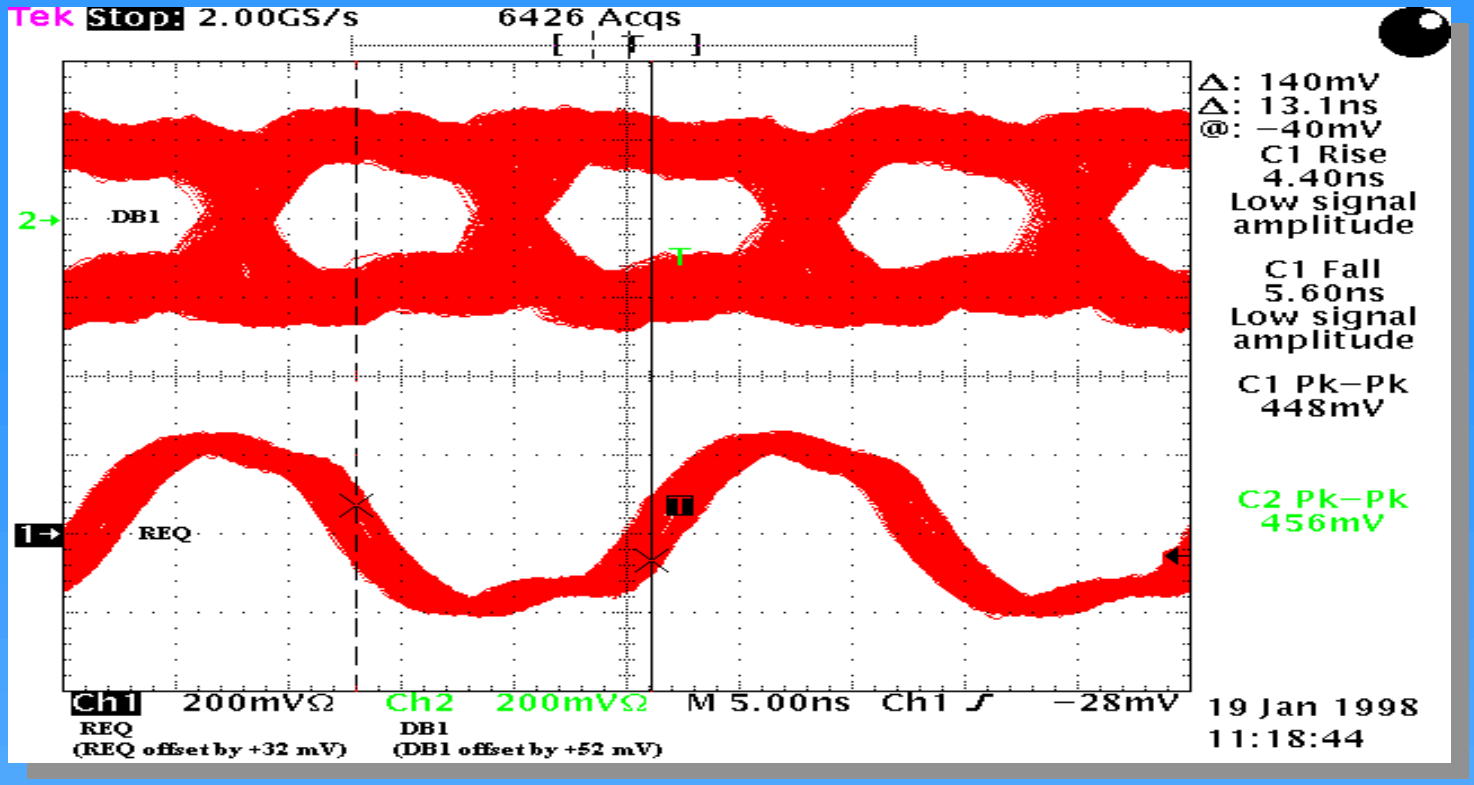

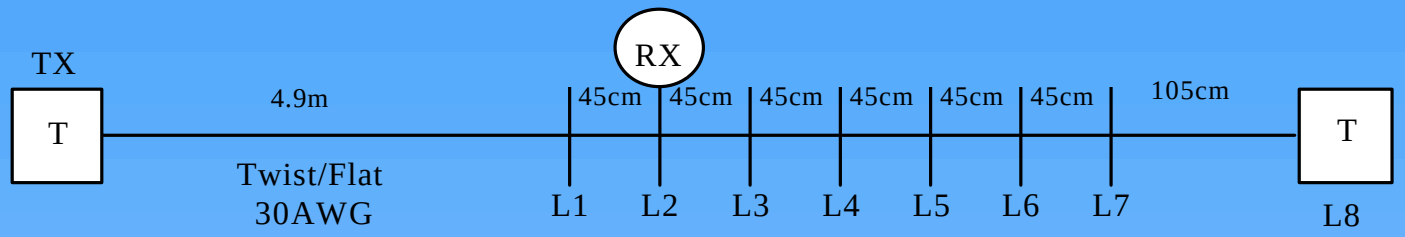

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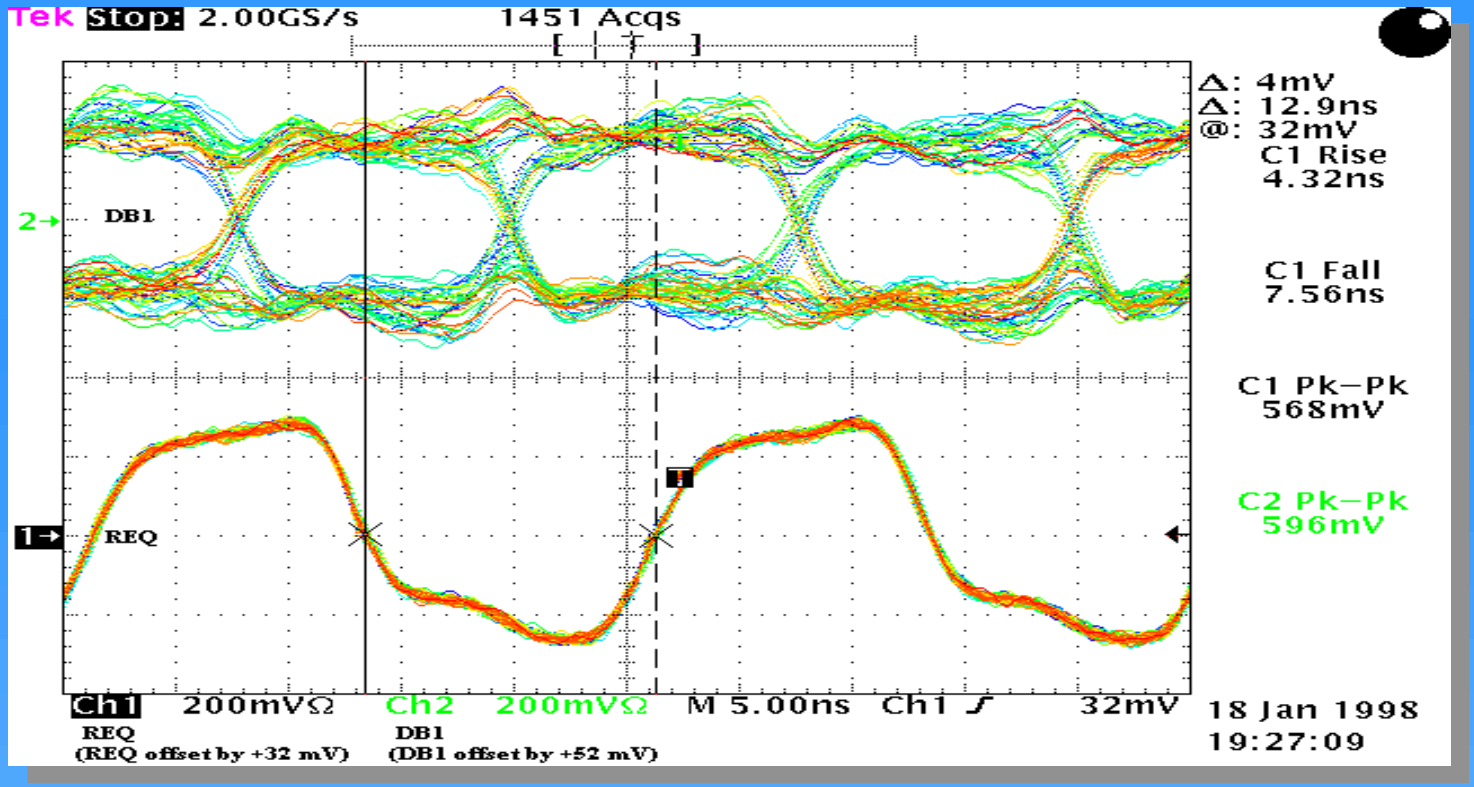

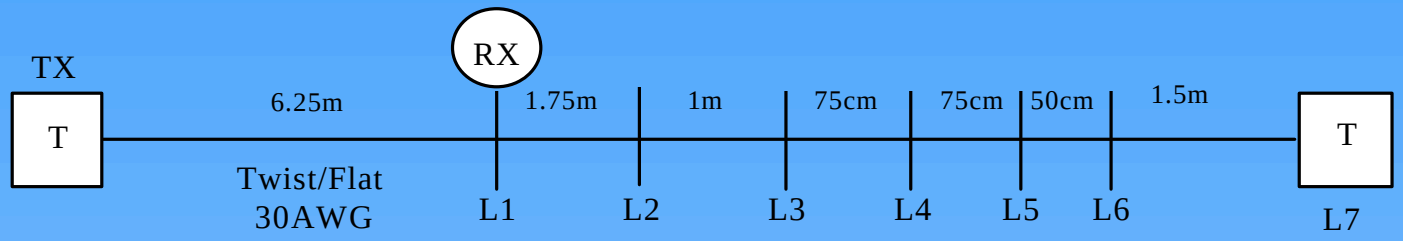

Note:
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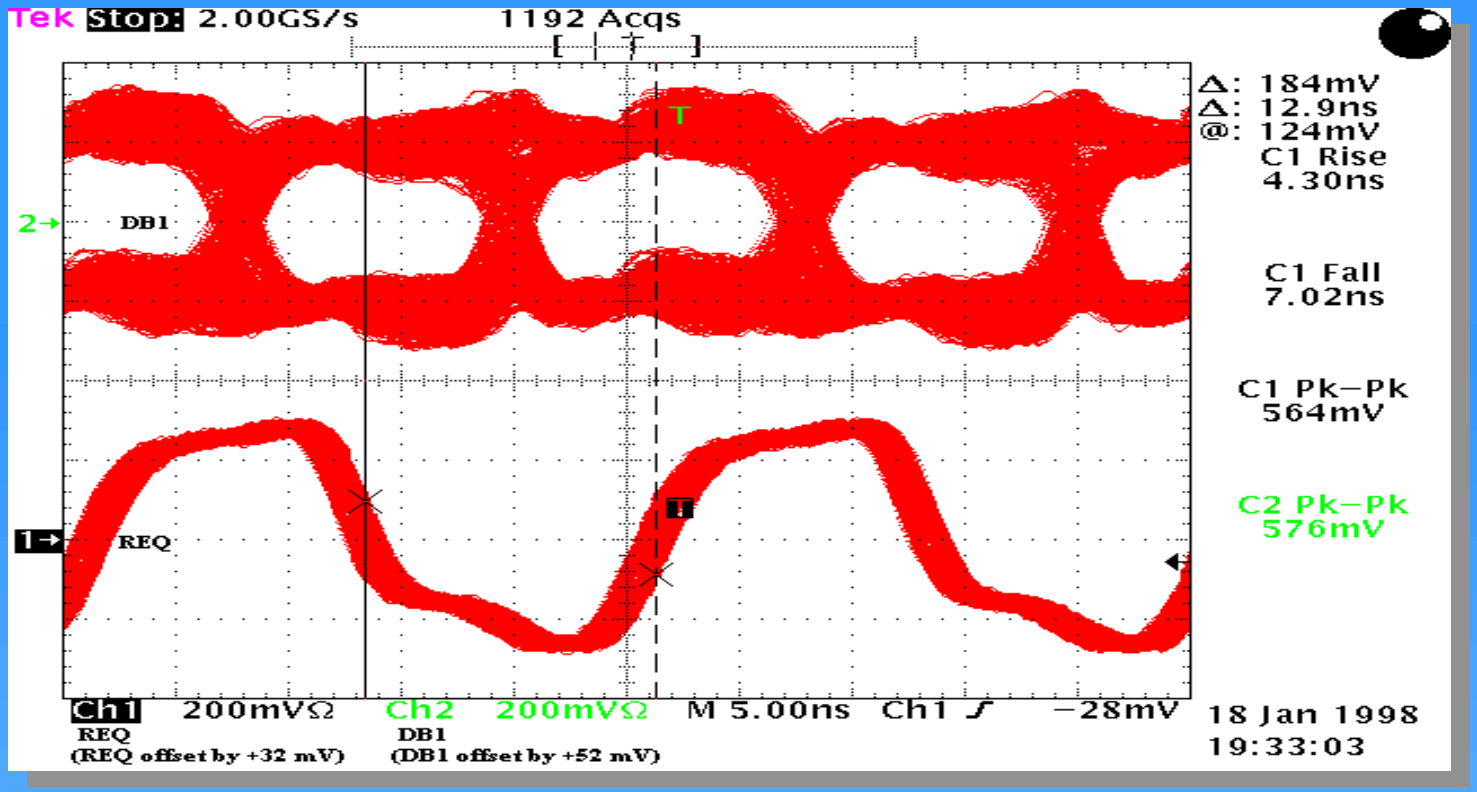
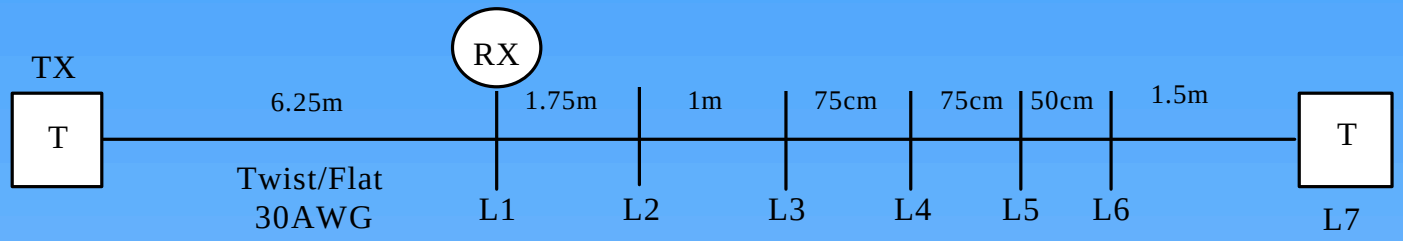
"Eye pattern for 12 m multi-drop configuration"
(trigger at center of REQ)





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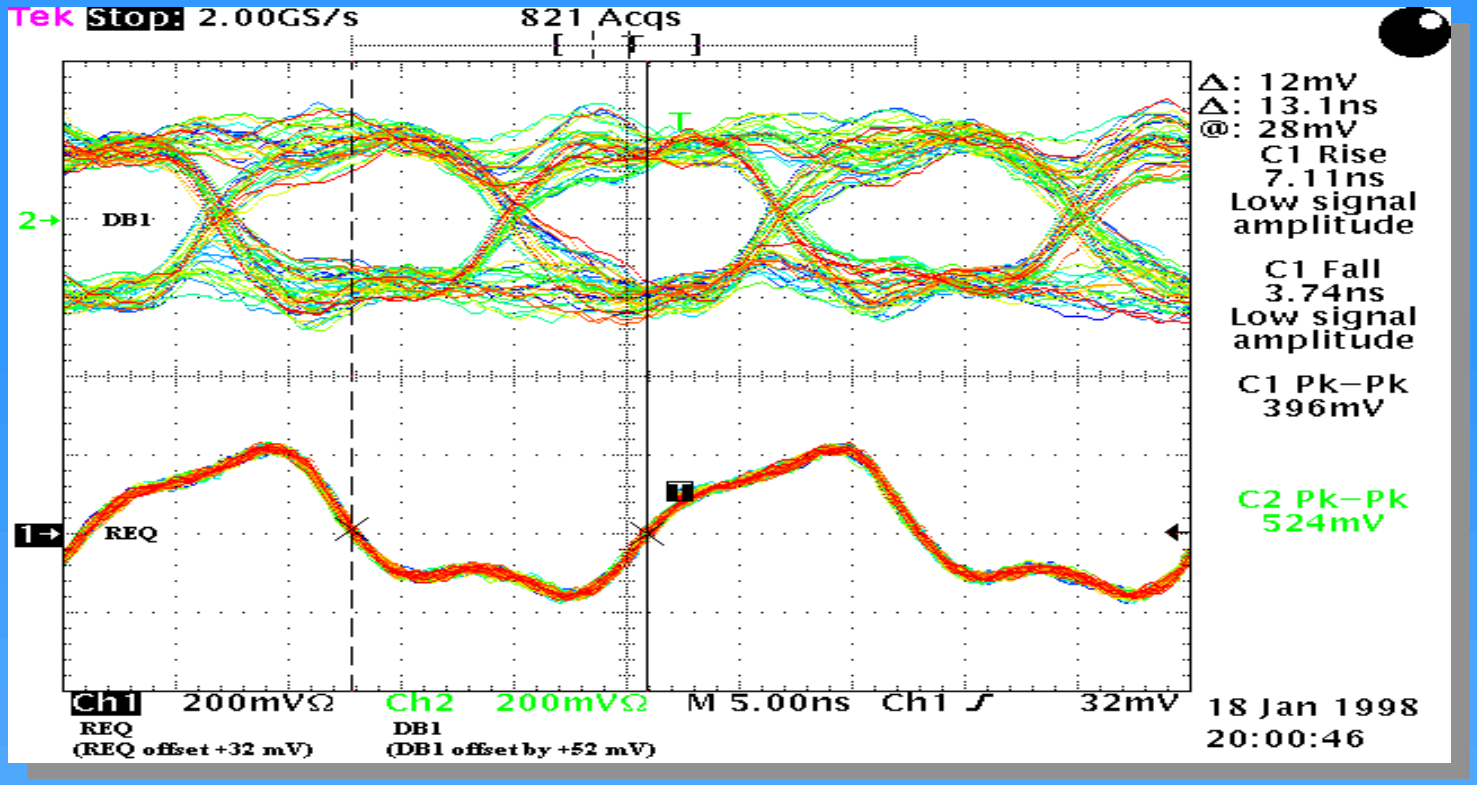

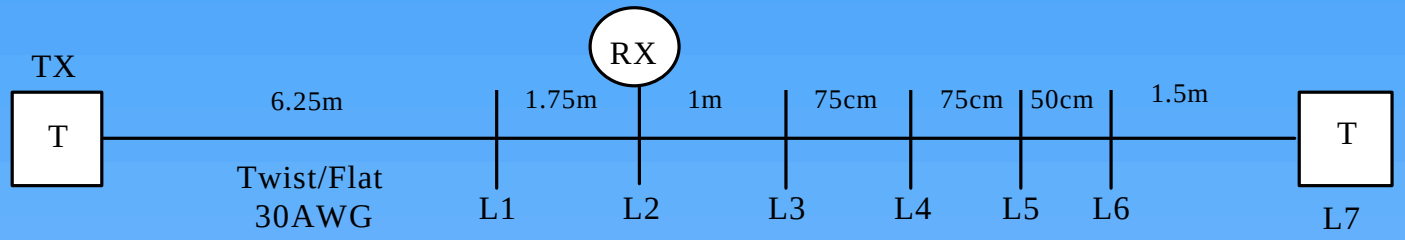

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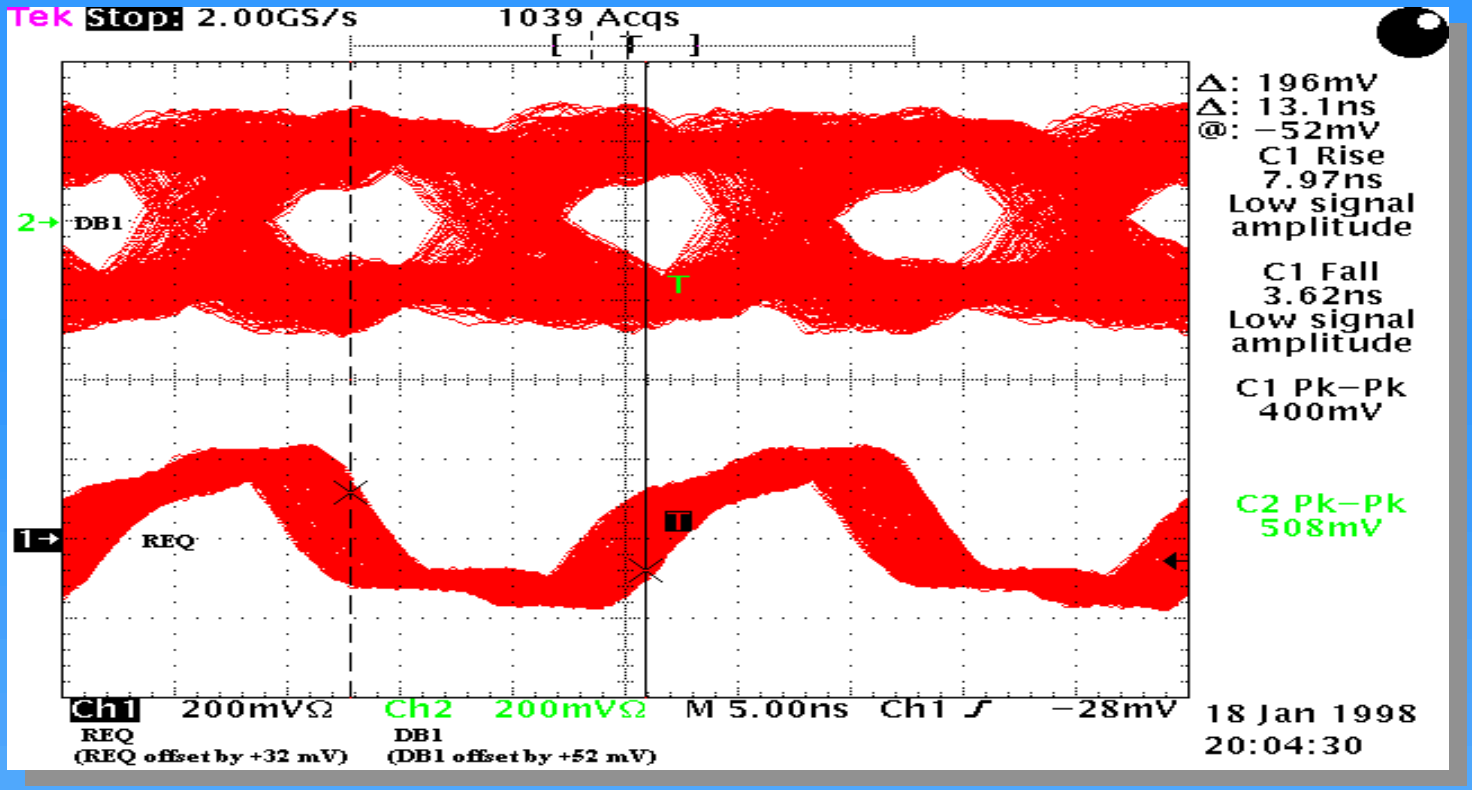

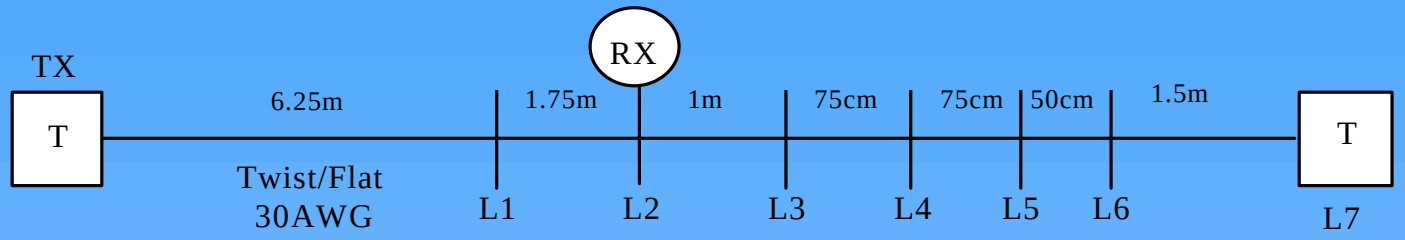

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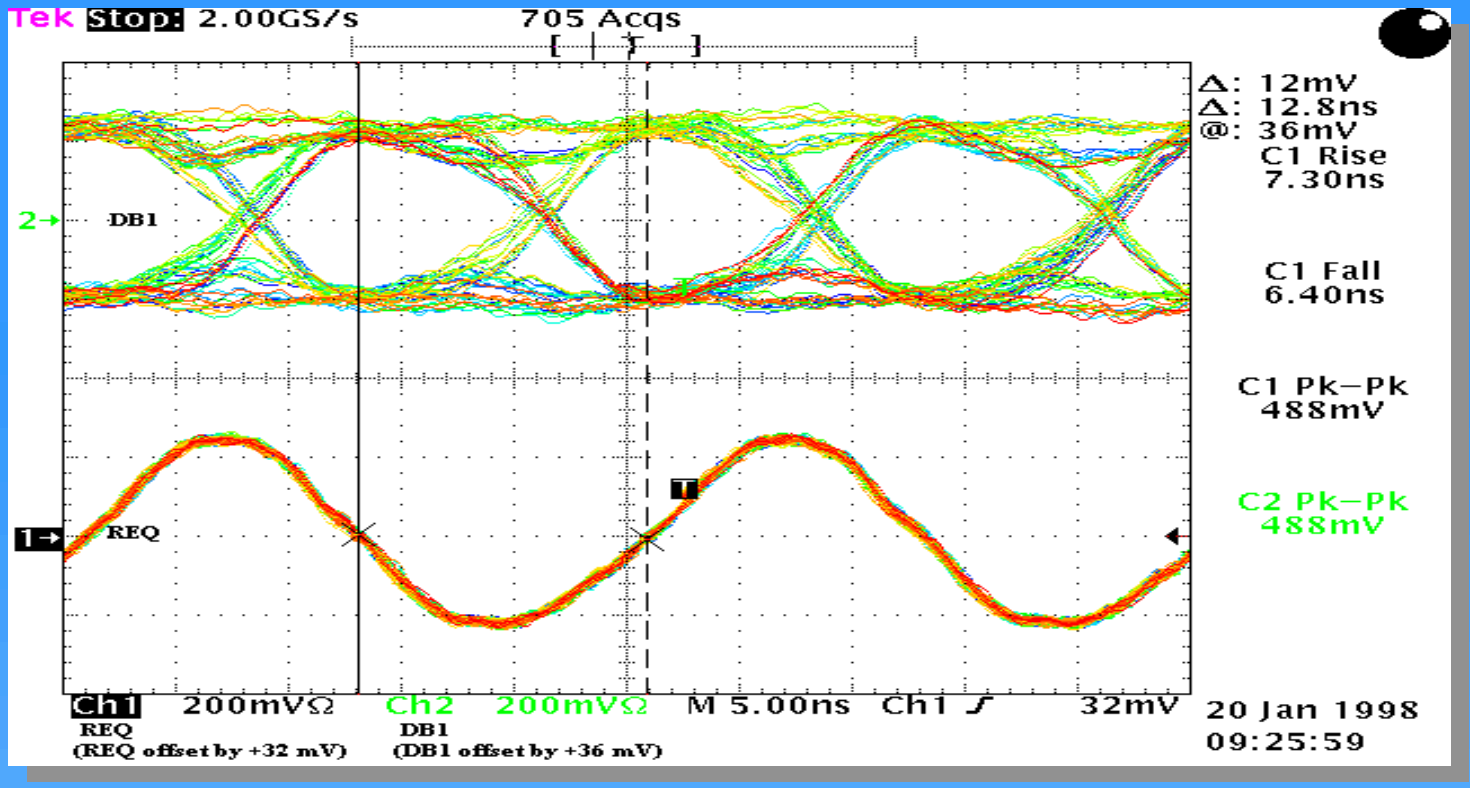

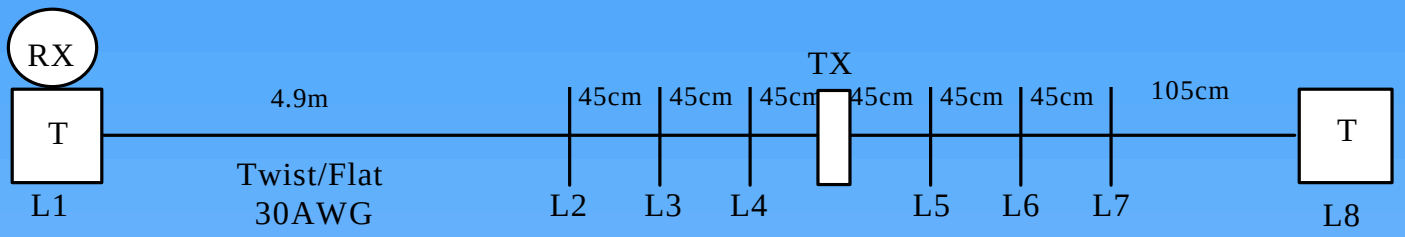

Note:
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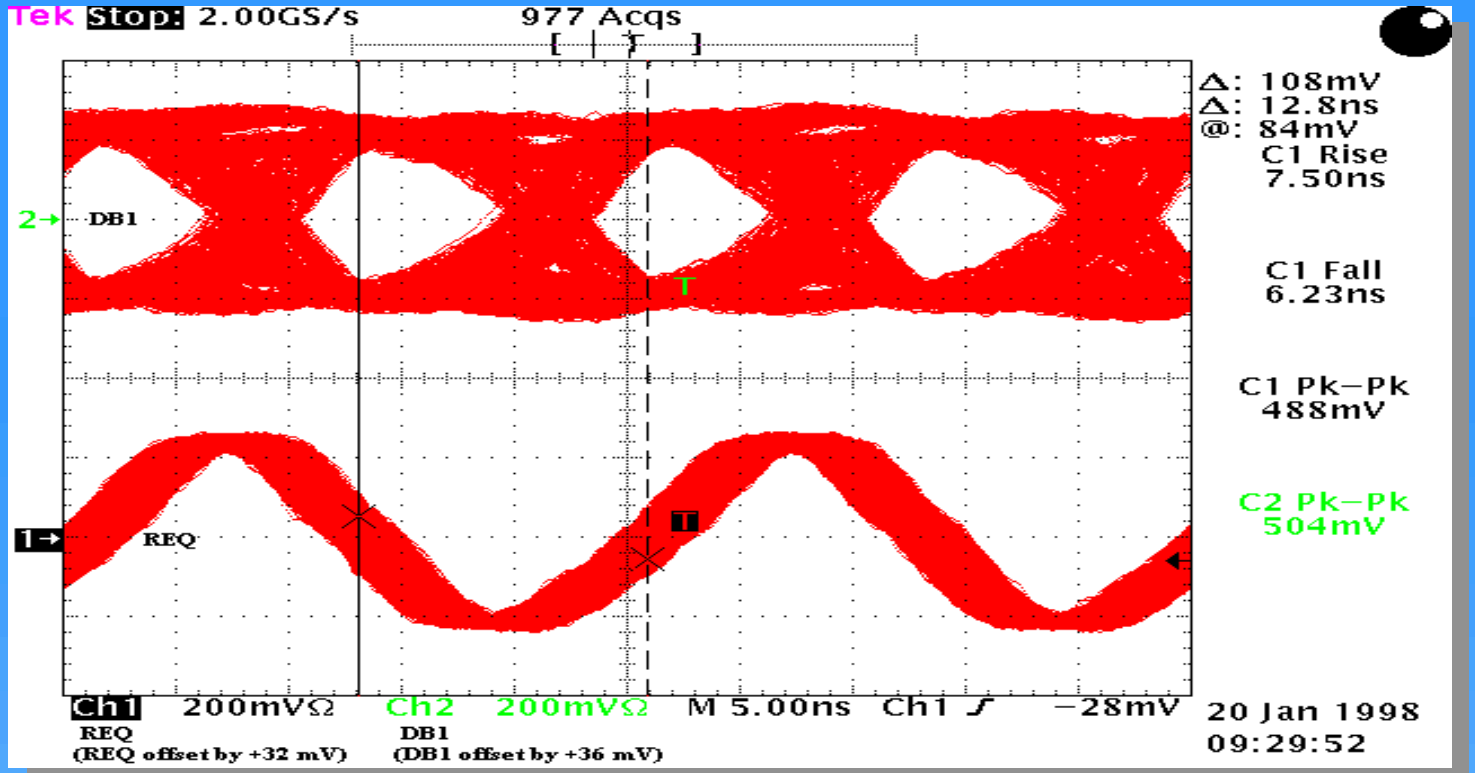
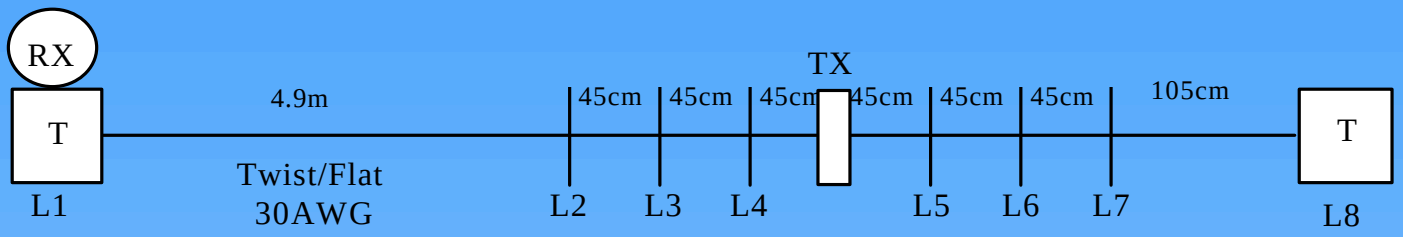
"Eye pattern for 8 m multi-drop configuration with driver in the middle" (trigger at center of REQ)





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(trigger +/- 60 mV from center of REQ)

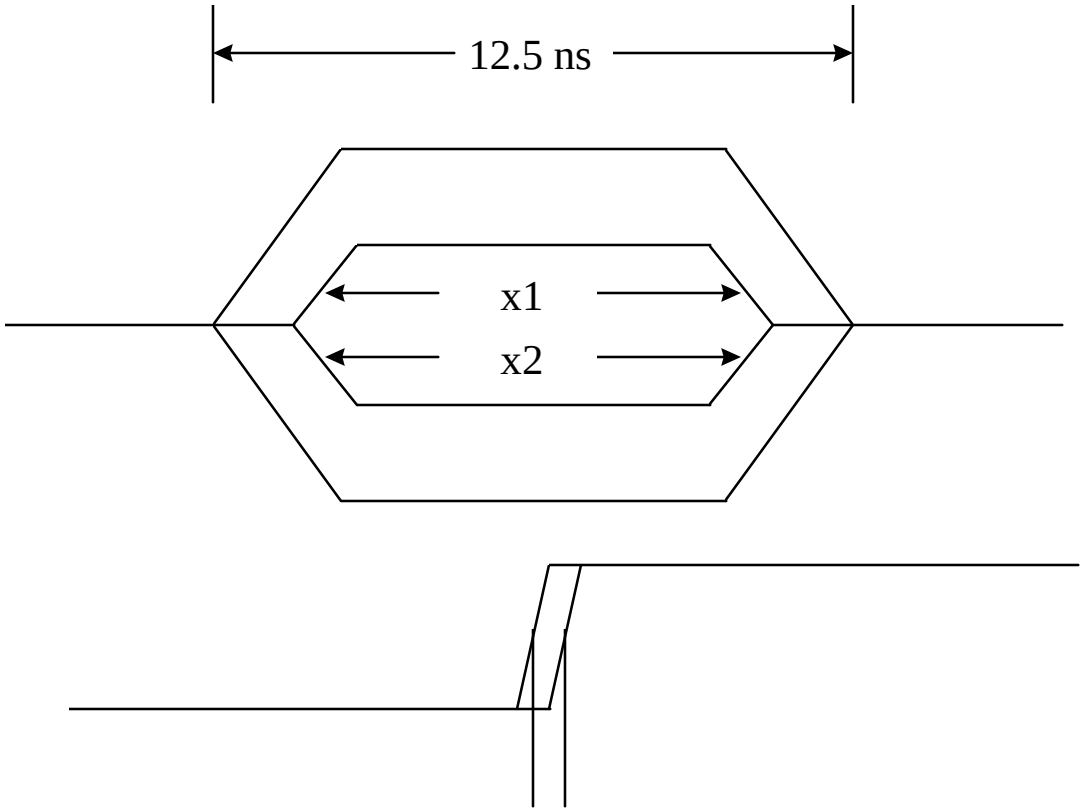
SUMMARY

- Worst case is tightly spaced loads
- Drive level is important when reflections are present
- More sensitive receiver would provide more margin
- Must add in worst case cable skew

SPECIFY MARGIN USING EYE PATTERNS

- Use eye pattern to evaluate driver and receiver compliance
- FC and 1394 specify this way but clock embedded in data
- In parallel system like SCSI need to account for cable skew

RECEIVER MARGIN (SETUP AND HOLD)



MARGIN = 1/2 X` - CABLE SKEW -1/2 CLOCK SKEW

X` IS SMALLER OF X1 OR X2
X1 AND X2 ARE MEASURED AT THRESHOLD OF RECEIVER