Date: Apr. 24, 1998
To: T10 Committee
From: Gerry Houlder, Seagate Technology
Subj: Add PLPB feature to Mode Page 19h

This proposal adds another feature to Mode Page 19h. This mode page is described in document 96-195r4, which was accepted for inclusion in FCP-2 at the March 1997 T10 meetings.

The Prevent Loop Port Bypass (PLPB) bit is being added at the request of a customer. We are not sure if any other customer is interested in this feature, but we would like to add it to this page. I think it is better to standardize this bit instead of defining a vendor unique field in a standard page.

One reason a vendor may want this feature is because “out of band” control of the port bypass circuits is desired. The Enclosure Services provides a method of controlling port bypass circuits or a proprietary method may be used. When such “out of band” control is desired, the primitive sequences intended to also control these circuits must be disabled to avoid conflict with the preferred mechanism.

Rev. 1: Adds text describing which bits cannot be set at the same time and describes error reporting for this case.

Addition to FCP-2:

The italicized text in the table and underlined words in the following text must be added.

Table xxx - Fibre channel control page

Bit Byte	7	6	5	4	3	2	1	0
0	PS	Resvd	Page code (19h)					
1	Page length (06h)							
2	Reserved							
3	Resvd	*PLPB*	DDIS	DLM	DSA	ALWLI	DTIPE	DTOLI
4	Reserved							
5	Reserved							
6	Reserved							
7	Reserved							

When Disable Target Originated Loop Initialization (DTOLI) bit is one, the target does not generate the initializing LIP following insertion into the loop. The target will respond to an initializing LIP when it is received. The target shall generate the Loop Failure LIP if it detects loop failure at its input and the Initializing LIP when the loop failure is corrected. When DTOLI bit is zero, the Target generates the Initializing LIP after it enables a port into a loop.

When Disable Target Initiated Port Enable (DTIPE) bit is one, the target waits for an initiator to send the Loop Port Enable primitive before inserting itself into the loop. The target uses the hard address available in the SCA connector or device address jumpers to determine if primitives are addressed to it. A Loop Port Enable primitive with the broadcast address shall also cause the target to insert itself into the loop. When DTIPE bit is zero, the target enables its port into the loop without waiting for a Loop Port Enable primitive.

When Allow Login Without Loop Initialization (ALWLI) bit is one, the target shall use the hard address available in the SCA connector or device address jumpers and accept logins without verifying the address with loop initialization. When ALWLI bit is zero, the target is required to verify its address through the loop initialization process before a login is accepted.

When Disable Soft Address (DSA) bit is one, the target does not select a soft address if there is a conflict for the hard address selection during loop initialization. In this case the target enters the non-participating state. If the target detects loop initialization while in the non-participating state, the target will again attempt to get its hard address. When DSA bit is zero, the target attempts to obtain a soft address during the loop initialization process.

When Disable Loop Master (DLM) bit is one, the target does not become loop master. The target only repeats LISM frames it receives. This allows the initiator to be loop master during loop initialization. When DLM bit is zero, the Target may become loop master during in the loop initialization process.

When Disable Discovery (DDIS) bit is one, the target does not require receipt of Address or Port Discovery following loop initialization. The target resumes processing of tasks on completion of loop initialization. When DDIS bit is zero, the target must wait to receive an Address or Port Discovery before it resumes processing tasks for that initiator.

When the Prevent Loop Port Bypass (PLPB) bit is one, the target shall ignore any Loop Port Bypass (LPB) and Loop Port Enable (LPE) primitive sequences. The loop port shall remain enabled. When the PLPB is zero, the target allows the Loop Port Bypass and Port Bypass Enable primitive sequences to control the port bypass circuit.

It shall be illegal to set DTIPE to one and PLPB to one.

When an illegal bit combination is sent by the application client the device server shall return CHECK CONDITION status and the sense key shall be set to ILLEGAL REQUEST with the additional sense code set to INVALID FIELD IN THE PARAMETER LIST.