Date: Jan. 1, 1998
To: T10 Committee
From: Gerry Houlder, Seagate Technology
Subj: Add PLPB feature to Mode Page 19h

This proposal adds another feature to Mode Page 19h. This mode page is described in document 96-195r4, which was accepted for inclusion in FCP-2 at the March 1997 T10 meetings.

The Prevent Loop Port Bypass (PLPB) bit is being added at the request of a customer. We are not sure if any other customer is interested in this feature, but we would like to add it to this page. I think it is better to standardize this bit instead of defining a vendor unique field in a standard page.

One reason a vendor may want this feature is because “out of band” control of the port bypass circuits is desired. The Enclosure Services provides a method of controlling port bypass circuits or a proprietary method may be used. When such “out of band” control is desired, the primitive sequences intended to also control these circuits must be disabled to avoid conflict with the preferred mechanism.

Addition to FCP-2:

The underlined text must be added. Unchanged text is not shown. The entire table describing mode page 19h is shown for reference.

Table xxx - Fibre channel control page

Bit Byte	7	6	5	4	3	2	1	0
0	PS	Resvd	Page code (19h)					
1	Page length (06h)							
2	Reserved							
3	Resvd	PLPB	DDIS	DLM	DSA	ALWLI	DTIPE	DTOLI
4	Reserved							
5	Reserved							
6	Reserved							
7	Reserved							

When the Prevent Loop Port Bypass (PLPB) bit is one, the target shall ignore any Loop Port Bypass (LPB) and Loop Port Enable (LPE) primitive sequences. The loop port shall remain enabled. When the PLPB is zero, the target allows the Loop Port Bypass and Port Bypass Enable primitive sequences to control the port bypass circuit.