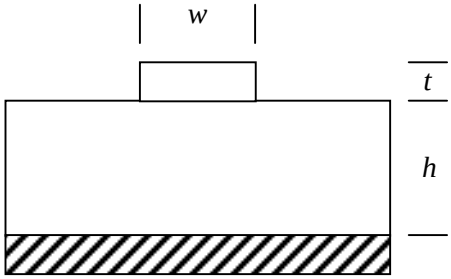
Universal Backplane Annex

By Dean Wallace
Linfinity Microelectronics Inc.

Printed circuit boards are constructed using either microstrip or stripline or a combination of both for routing signals. The important electrical characteristics can be determined from the geometries and the material properties of the microstrip or stripline.

Microstrip



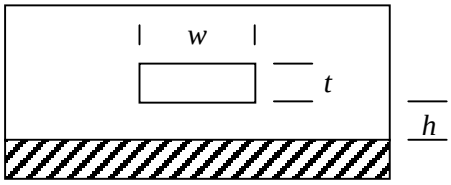
$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.83w + t}\right) ohms \quad \text{(characteristic impedance)}$$

$$T_{pd} = 33.36\left(0.475e_r + 0.67\right)^{1/2} \ ps/cm \quad \text{(propagation delay)}$$

Embedded Microstrip

$$Z_O = \frac{K}{\sqrt{0.805e_r + 2}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$T_{pd} = 33.36\left(0.475e_r + 0.67\right)^{1/2} \ ps/cm$$

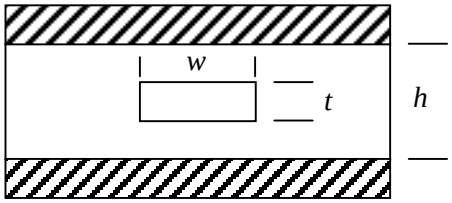


K is a constant, between 60 and 65, and varies with the thickness of the dielectric covering the conductor. If the thickness is below 15 mils K=65, at 20 mils K=60.

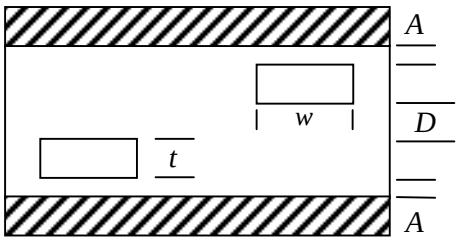
Stripline

$$Z_O = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{0.67\pi w\left(0.8 + t/w\right)}\right) ohms$$

$$T_{pd} = 33.36\left(e_r\right)^{1/2} \ ps/cm$$



Dual Stripline



$$Z_O = \frac{2F_1F_2}{F_1 + F_2}\ ohms$$

$$F_1 = \frac{60}{\sqrt{e_r}}\ ln\left(\frac{8A}{0.67\pi w\left(0.8 + {}^{t}/_{w}\right)}\right)$$

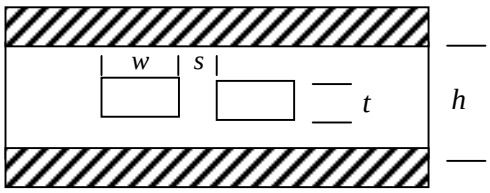
$$F_2 = \frac{60}{\sqrt{e_r}}\ ln\left(\frac{8(A+D)}{0.67\pi w(0.8 + {}^{t}/_{w})}\right)$$

$$T_{pd} = 33.36\left(e_r\right)^{1/2}\ {}^{ps}/_{cm}$$

e_r = is the relative dielectric constant

When the single-ended impedance has been determined, the differential impedance is found based on conductor spacing and dielectric thickness. Both traces of the differential pair should have the same physical cross section dimensions. If the spacing becomes too small the capacitive coupling and the *mutual* inductance will reduce the differential impedance.

Differential Impedance



Microstrip

$$Z_{diff} = 2Z_O\left(1 - 0.48e^{\left(-0.96\ {}^{s}/_{h}\right)}\right)\ ohms$$

Stripline

$$Z_{diff} = 2Z_O\left(1 - 0.374e^{-\left(2.9\ {}^{s}/_{h}\right)}\right)\ ohms$$

The practical range of Z_O and Z_{diff} are from 20 ohms to 150 ohms. A typical range is between 50 ohms and 110 ohms. This impedance depends on the trace width and distance to ground. If the trace is wide and closer to ground it is more capacitive and has a lower impedance. If the trace is narrow and the spacing from the ground plane is larger, the trace is more inductive and has a higher impedance. Controlled impedance boards in which all the impedances match within several ohms usually have a characteristic impedance in the 50 ohm to 80 ohm range. This is due to manufacturing constraints such as maximum dielectric thickness and minimum trace widths.
The trace capacitance and inductance are important parameters for calculating the transmission line parameters.

Microstrip

$$C_O = \frac{T_d}{Z_O} = \frac{33.36\sqrt{0.475e_r + 0.67}}{Z_O} \quad pF/cm$$

$$L_O = Z_O T_d = 33.36\ Z_O \sqrt{0.475e_r + 0.67} * 10^{-3}\ nH/cm$$

Stripline

$$C_O = \frac{T_d}{Z_O} = \frac{33.36\sqrt{e_r}}{Z_O} \quad pF/cm$$

$$L_O = Z_O T_d = 33.36\ Z_O \sqrt{e_r} * 10^{-3}\ nH/cm$$

From the above the characteristic impedance for the backplane is primarily determined by;

- Width and thickness of the conductors.
- Dielectric constant of the substrate material.
- The substrate material thickness between the conductor and reference planes.

The differential impedance is determined primarily by the conductor spacing and dielectric thickness.

Proper selection of the dielectric material is very important for high speed PCB's. Two key parameters are the dielectric constant of the material and the loss tangent. The dielectric constant relates to the materials' ability to hold charge and the loss tangent refers to how much of the energy is lost in the material due to dissipation. The ideal materials have small numbers. The table gives a sample of some materials.

Material	***Dielectric Constant***	***Loss Tangent***
Air	1.0	0
PTFE (teflon)	2.1 - 2.5	0.0002 - 0.002
BT resin	2.9 - 3.9	0.003- 0.12
Polyimide	2.8 - 3.5	0.004 - 0.02
Silica (quartz)	3.8 - 4.2	0.0006 - 0.005
Polyimide / Glass	3.8 - 4.5	0.003 - 0.01
Epoxy / Glass (FR-4)	4.1 - 5.3	0.002 - 0.02

The most frequently used dielectric are a glass-epoxy (G-10) and a derivative, FR-4. The FR-4 material has acceptable performance to about 100MHz.

For higher speeds, materials like teflon should be considered, although they are much more expensive. PCB manufacturers publish specifications with their boards, among them should be the dielectric constant and loss tangent and other electrical properties. The board tolerances should also be specified. For example in a FR-4 PCB the dielectric constant can change by as much as 10% on a single board. These changes affect the propagation velocity and lead to skew.

If the PCB trace impedance cannot be made to match the cable impedance then a decision has to be made if termination is needed. If the signal electrical length is greater than ½ of the rising edge, then the lines should be terminated (if the impedance can't be controlled). This length can be expressed as:

$$\text{Length} = \frac{T_r}{2\sqrt{LC}}$$

T_r is the rise time of the waveform

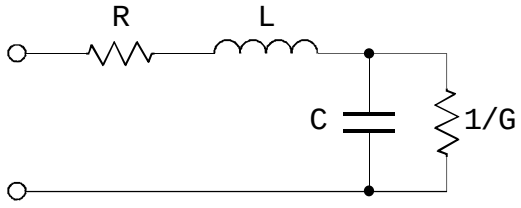
L is the inductance

C is the total capacitance

If the round trip time for the switching waveform is greater than the rise or fall time of the driving device, the settling of the transmission line effects are not hidden during the rise and fall time of the driving device.

In other words, in order to be a transmission line $2 \times T_{pd} > T_R$ or T_F (the minimum of the two), T_{pd} is the one way propagation delay.

A typical transmission line element is broken into four parts, a series resistance, series inductance, shunt conductance, and shunt capacitance.



When using this model the minimum wavelength must be much longer than the individual section to make it appear as a distributed model. The non-linearities are usually ignored. The general form for the impedance is:

$$Z_O = \frac{\lambda(R + j\omega L)}{2} \pm \frac{1}{2}\left(\lambda^2 (R + j\omega L)^2 + 4\left(\frac{R + j\omega L}{G + j\omega C}\right)\right)^{1/2}$$

If you make the section length (λ) of the segment small enough, the result is the distributed model.

$$Z_O = \left(\frac{R + j\omega L}{G + j\omega C}\right)^{1/2}$$

If the transmission rate is high i.e. $\omega/2\pi > 100kHz$ than ωL and ωC are much larger than R and G and the impedance becomes the more commonly used form of

$$Z = \left(L/C\right)^{1/2}$$

The other extreme is if $\omega/2\pi \leq 1kHz$ then

$$Z = \left(R/G\right)^{1/2}$$

Another important factor is the propagation velocity and propagation delay. The propagation delay per unit length is

$$T_{delay} = \frac{T_\lambda}{\lambda} = \left[\left(R + j\omega L\right) + \left(G + j\omega C\right)\right]^{1/2}$$

if the line is short then: $T_{delay} = j\omega\lambda\,(LC)^{1/2}$

The propagation velocity is $V = \lambda/(LC)^{1/2}$ for lossless lines.

The time delay is $T = 1/V = (LC)^{1/2}$ which give a total propagation delay of $T = \lambda\,(LC)^{1/2}$. The two equations most commonly used for hard calculations are:

$Z = (L/C)^{1/2}$ (characteristic impedance)

$T = \lambda\ (LC)^{1/2}$ (propagation delay)

If these values are not specified they can be calculated from the cross section geometries and dielectric material used for the PCB. The equation using the geometries and material are based on the above equation, but must also be treated as if they were operating in the transverse electromagnetic mode. When calculating the impedance and propagation delay, the capacitive loads also have to be accounted for. Capacitive loading decreases the impedance and increases the

$$T'_{pd} = T_{pd}\left(1+\left(C_D / C_O\right)\right)^{1/2}$$

$$Z'_O = \frac{Z_O}{\left(1+\left(C_D / C_O\right)\right)^{1/2}}$$

propagation delay.
Another form:

The intrinsic capacitance is C_O and the load cap is C_D. Besides reducing the impedance and increasing the propagation delay, a heavily loaded trace also slows the rise and fall times of the drivers and filters (RC filter) out some high frequency components. The loaded propagation delay must be used when deciding whether or not to treat the trace as a transmission line.

When adding the load capacitance, remember that sockets and vias add to the

$$T'_{pd} = \left(L\left(C_D + C_O\right)\right)^{1/2}$$

$$Z'_O = \left(\frac{L}{\left(C_D + C_O\right)}\right)^{1/2}$$

distributed capacitance, sockets add approximately 2pF and vias add from 0.3pF to 0.8pF. The impedance and length of the connector also must be considered.

Using traces with a higher intrinsic capacitance reduce the effects of the loading. For instance, microstrip is faster than stripline, but is affected more by loading since it has a lower characteristic capacitance.

The complete forms of loaded propagation delay and impedance are:

Microstrip

$$T'_{pd} = 5.776\left(15.85e_r + 22.35 + C_D Z_O\left(0.475e_r + 0.67\right)^{1/2}\right)^{1/2}\ ps/cm$$

$$Z'_O = \frac{Z_O}{\left(\frac{C_D Z_O}{33.36\left(0.475e_r + 0.67\right)^{1/2}} + 1\right)^{1/2}}\ ohms$$

Stripline

$$T'_{pd} = 5.776\left(33.36e_r + C_D Z_O\left(e_r\right)^{1/2}\right)^{1/2}\ ps/cm$$

$$Z'_O = \frac{Z_O}{\left(\frac{C_D Z_O}{33.36\left(e_r\right)^{1/2}} + 1\right)^{1/2}} \quad ohms$$

The impedance mismatches between loads, sources, connectors, cables, and traces can cause transmission line effects such as ringing, stair step effects, and long bus settle delays. These are caused by reflections at the impedance discontinuities, the reflection coefficients are:

$$P_L = \frac{Z_L - Z_O}{Z_L + Z_O} \quad \text{(at load)}$$

$$P_S = \frac{Z_S - Z_O}{Z_S + Z_O} \quad \text{(at source)}$$

These reflections, if large enough, can cause false transitions. They can also cause standing waves.

$$VSWR = \frac{1 + |P|}{1 - |P|}$$

The standing waves are the quarter wavelengths (2/4) when the wavelength is:

$$\lambda = \frac{1}{f\left(LC\right)^{1/2}}$$

To capture all the harmonic content of the square wave the frequency used should be $f = 0.5 / t_R$. The reflections can also cause long bus settle times. The signals magnitude at time t is $t = (P_S P_R)^{t/T}$ where T is the one way propagation delay. Remember the driver use and fall times are very important in the behavior of the transmission line.

If the round trip delay on the trace is longer than the rising or falling edge the line should probably be terminated or the characteristic impedance of the board should match the cable impedance.

The maximum non-terminated length for a trace is:

Microstrip

$$L_{max} = \frac{\left(\left(C + Z_O\right)^2 + 12.3 \times 10^6\right)^{1/2} - C_t Z_O}{66.7\left(0.475 e_r + 0.67\right)^{1/2}} \quad cm$$

Stripline

$$L_{max} = \frac{\left(\left(C_t Z_O\right)^2 + 12.3 \times 10^6\right)^{1/2} - C_t Z_O}{66.7\left(e_r\right)^{1/2}} \quad cm$$

Z_O is the unloaded impedance and C_t is the total load capacitance.

Some general guidelines for laying out PCB's are:

1. Evenly distribute loads along the trace, this give a distributed load and reduces reflection from discontinuities.
2. Avoid T's for critical signals.
3. Add sockets and vias into capacitance calculations.
4. Keep trace lengths as short as possible.
5. Use as low a dielectric constant material as possible.
6. If possible use a controlled impedance PCB, so that the behavior is predictable.
7. Balance path lengths to reduce skew.
8. Minimize length through the connector.

When deciding whether to use stripline or microstrip the number of layers and the complexity of the routing have to be taken into account. In many cases a combination of stripline and microstrip are used.

Differential pairs have the advantage that the two adjunct signals are the complement of each other. The current and voltage levels are the same, but 180 degrees out of phase, therefore concealing the magnetic fields. This provides immunity to EMI and crosstalk.

When routing differential traces the spacing between the pairs must be taken into account since this controls the differential impedance. The spacing should be as constant as possible. If possible the PCB impedance should match the cable impedance, if it is off substantially the trace dimensions should be adjusted to provide the match, therefore reducing reflections. The differential traces should run close to each other and as parallel as possible. The electrical lengths should be as close as possible to prevent skew. Mitering can be done on the traces to match electrical length. Orthogonal turns should be avoided because they change the impedance, also an arc can be used instead of rounding edge.

Crosstalk is always an issue and all TTL/CMOS signal paths should be isolated from LVD signal paths. Since crosstalk is proportional to d_v / d_t, crosstalk can easily occur if lines with large voltage swings are near LVD lines. To isolate the lines, either increase the separation, run ground traces between them, or isolate them by using different planes. Since crosstalk is caused by the capacitive coupling between signals and the mutual inductance some general observations are:

1. Crosstalk scales with signal amplitude.
2. Crosstalk is proportional to slew rate V/T_r. Slower rise/fall times yield less crosstalk.
3. For end crosstalk width is equivalent to the rise/fall time.