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Reply to: William C. Gintz

To: T10 Membership
From: William C. Gintz
Subject: Presentation to Fast-80 Study Group – 11/97

1 Overview

Fast-80 Amplitude and Jitter Budgets

Analytical Projections

Worst Case Margins 2.5 ns/6.25 ns

Multi-Drop Effect

Reflections and ISI

Hot Plug Simulation

Empirical Results

Reflections Dominate Jitter

Multi-Drop Dominates Amplitude

Skew and ISI Unwieldy

Hot Plug Is Problematical

2 Analysis

Table 1 shows the Fast-80 amplitude budget

Table 1 – Fast-80 Amplitude Budget

	Dual Edge at 40 MHz		
Signal Amplitudes	**Nominal**	**Weak**	**Proposed**
Driver Vop	445	270	270
Loaded Cable Attenuation	64% or –3.8 db	Cable –3.0 db	85%
Receiver (at SCSI pin)	278	162	230
First Pulse Vop	268	156	220
Noise & Offsets			
Fail Safe Bias	-112	-125	100
Receiver Offset	20	20	20
Cable Crosstalk	5	3	4
Reflections 10%	27	16	22
Totals	144	144	146
Margins			
Normal	114	2	74
Transient			70
Margin			-4

Figure 1 shows the relationship between amplitude and jitter.

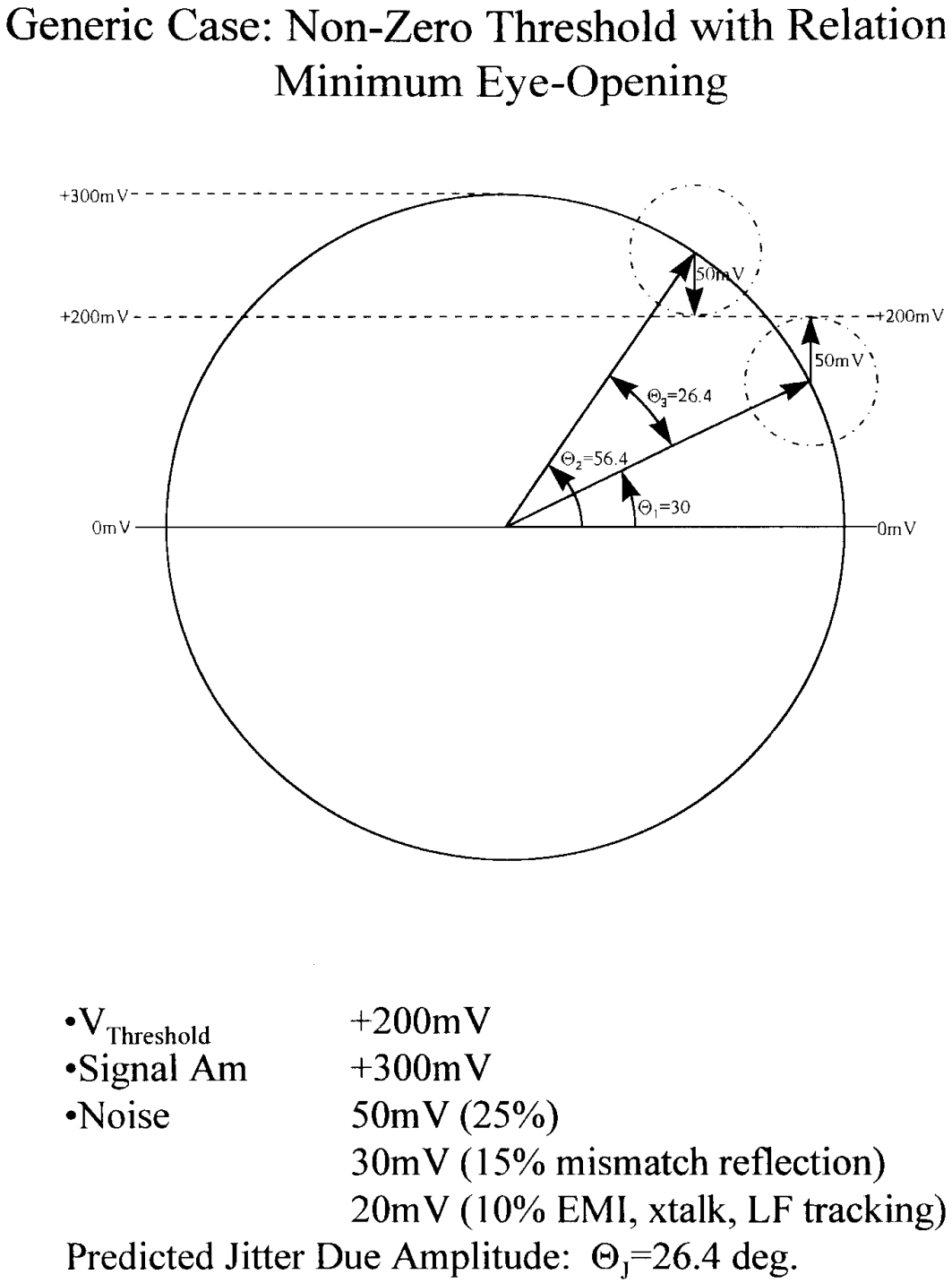

Figure 1- Relationship between Amplitude and Jitter

Table 2 shows the timing budget for duel edge clocking.

Table 2 – Timing Budget for Dual Edge Clocking

Generic Cause	Common name	abbreviation	Received signal levels		Remarks
			440mv	220 mv	
System band limit and cable loss	Data Dependent Jitter	DDJ	0.5	0.5 *	Hitachi data pending
Thermal noise in trigger levels	Gausian or random noise	RJ	0.1	0.2	
DC offset at detection point	Bi-modal jitter	BMJ	0.2	0. 4	
Reflections 10% of incident (mis-termination)	Deterministic Noise		0.5	0.6	
2% Local signal	Random System Noise	RXT	0.2	0.2	
Cable Skew unequal length	0.03ns/ft= 2.4 ns!		1.0	1.0	recommend cable be trimmed
Creq-Cdat = 2pf pcb layout	0.34ns/ft		(1.3)	(1.3)	applies only to multi-drop
HOT PLUG	a) 200mv; 4ns pulse		(2.0)-	(4.0)	prohibitive effect on REQ/ACK
	b) (Fast-80as connectors ~50mv 10ns pulse)		0.75	1.5	assumes staged R conector or
Totals /margin	25 meter point to point		3.25/3.0	4.4/1.85	
	12 meter multi-drop		4.55/1.7	5.7/0.5	

Notes: i) 25 meter 28-gauge cable point to point or;
ii) 12 meter 30-gauge cable multi-drop.

3 Empirical Data

Figure 2 is a block diagram of the hardware simulation. Figure 3 shows the instrumentation setup.

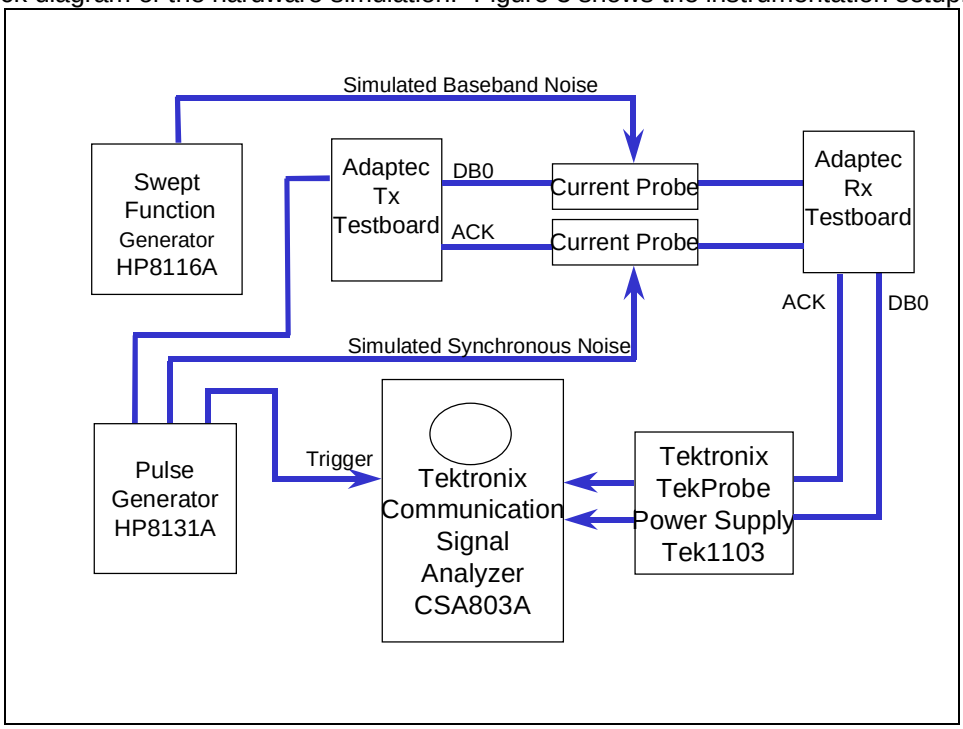

Figure 2 – Hardware Simulation of Fast-80

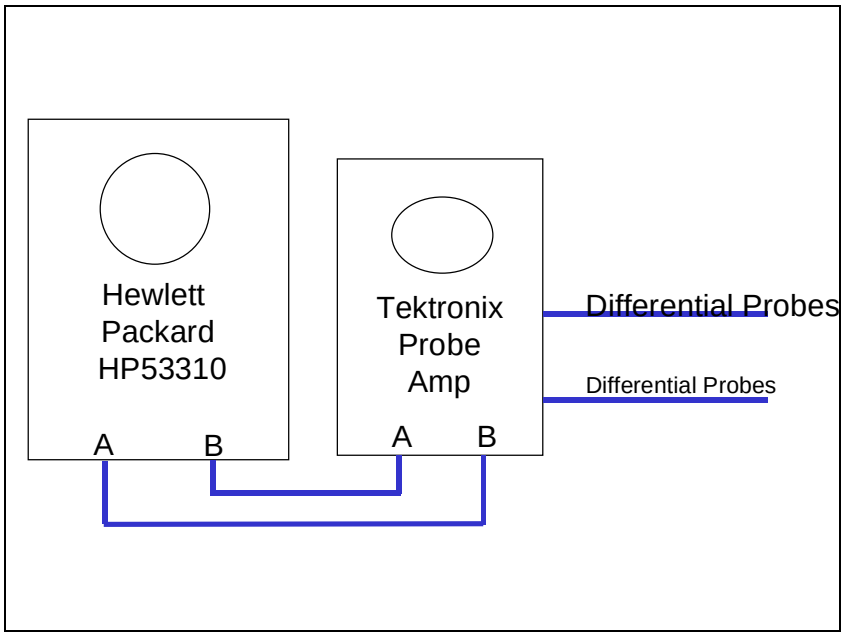

Figure 3 – Instrumentaion

Figure 4 shows a 25-meter 28-gauge point to point hardware simulation of timing margins. This is a 40-megatransfer single-edge simulating 80 megatransfers.

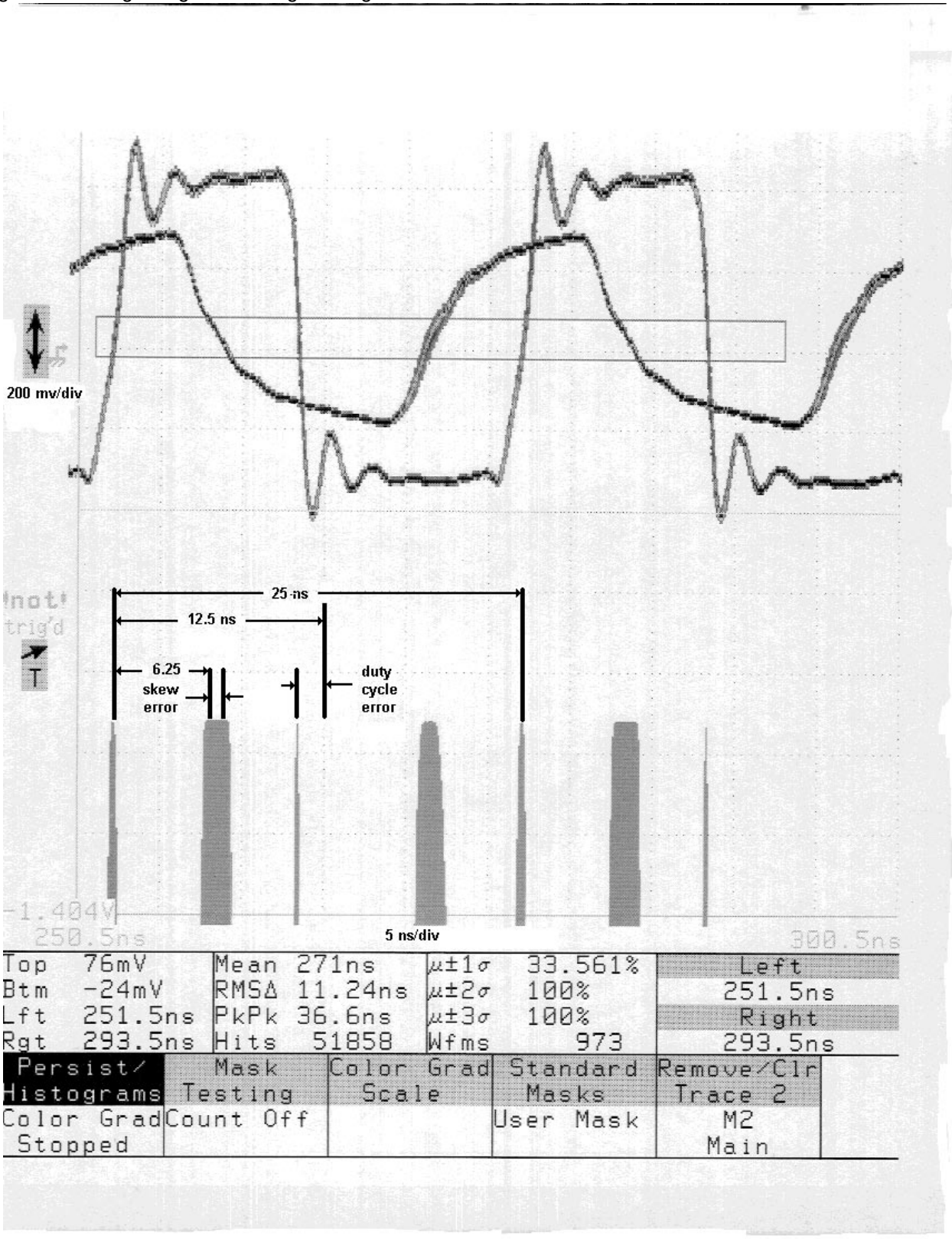

Figure 4 – 40 megatransfers Single Edge

Notes: i) duty cycle error 5%;
ii) skew error is 1 ns.

Figure 5 shows a 25-meter 28-gauge point to point hardware simulation of timing margins with inter-symbol interference (ISI). This shows a 40 MHz data edge with budget for ACK centering on errors

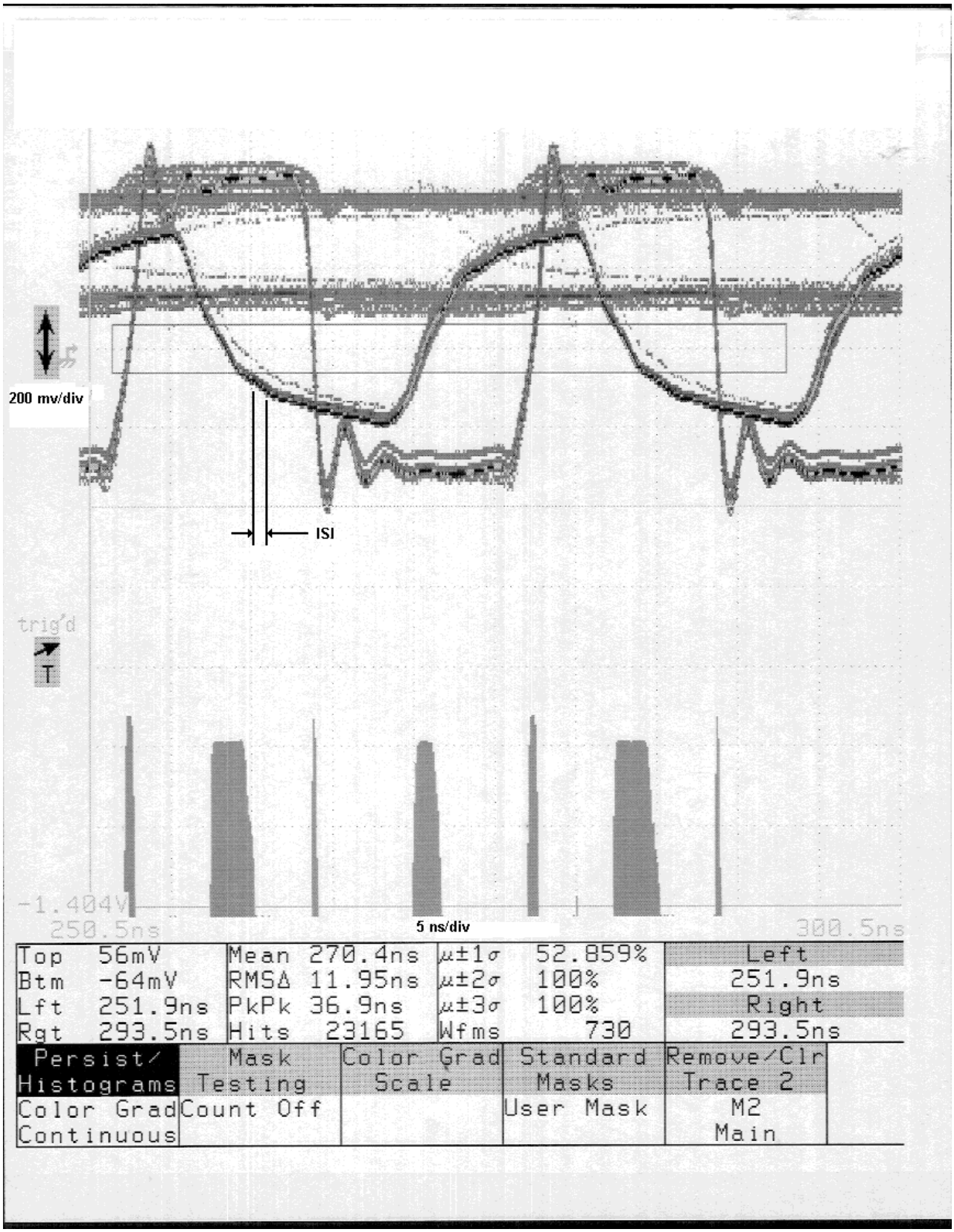

Figure 5 – 40 MHz Data Edges

Notes: i) “first pulse” adds 1.0 ns jitter to existing conditions of previous figure.

Figure 6 shows the normal signal.

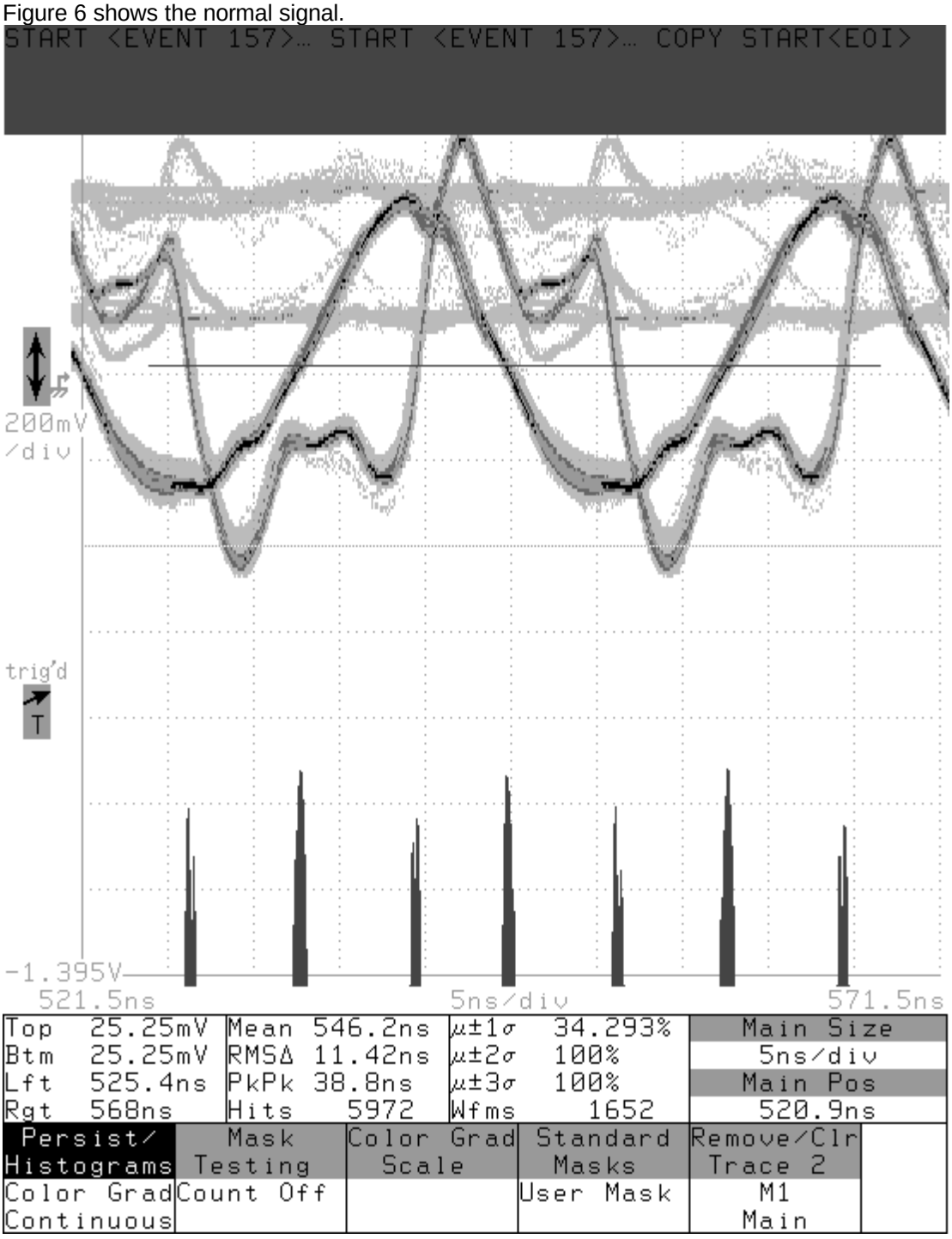

Figure 6 – Normal Signal

Notes:

Figure 7 shows the normal signal with 2 million cumulative hits.

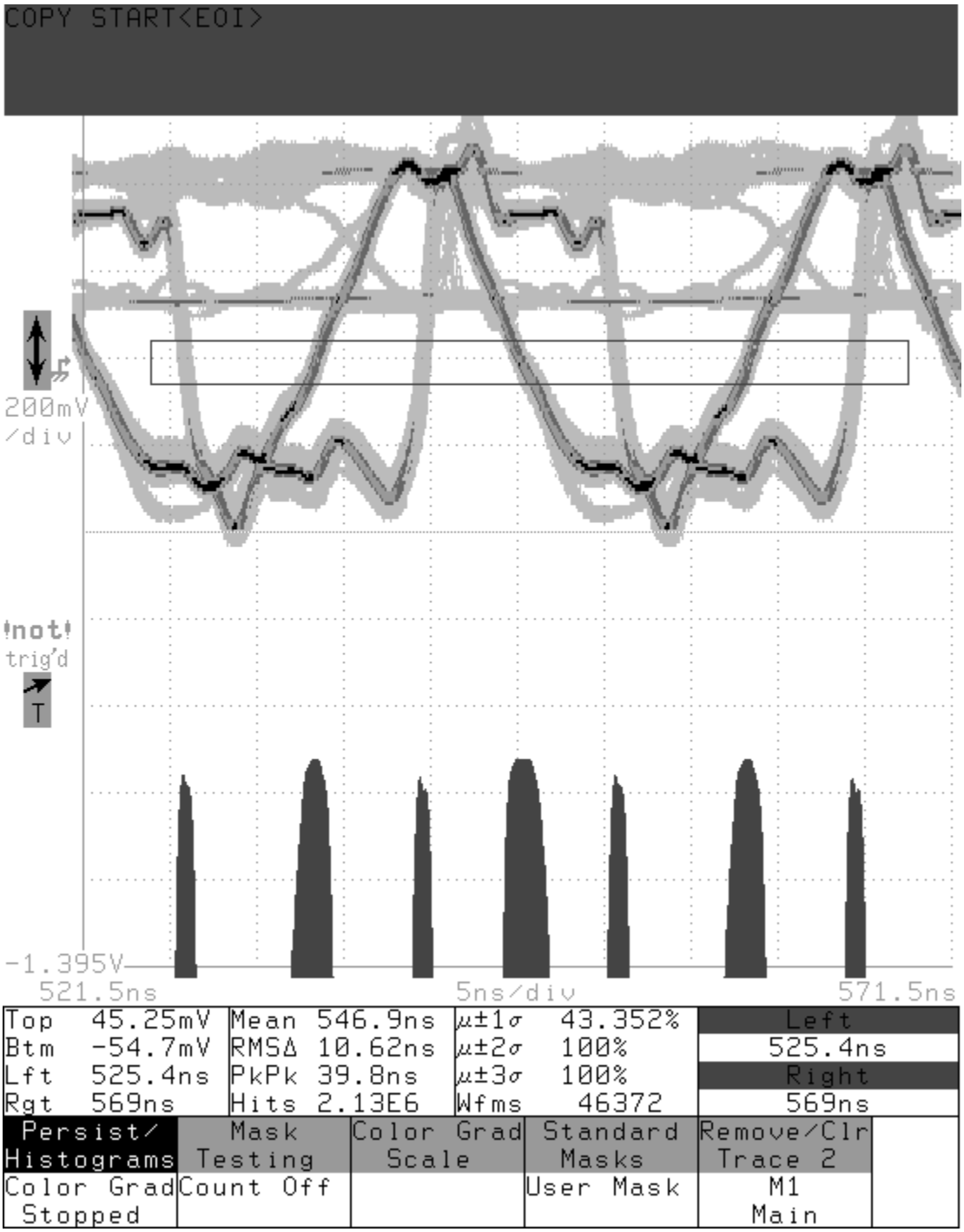

Figure 7 – Normal Signal with 2 million hits

Notes:

Figure 8 shows a simulated hot plugging with 2 million hits.

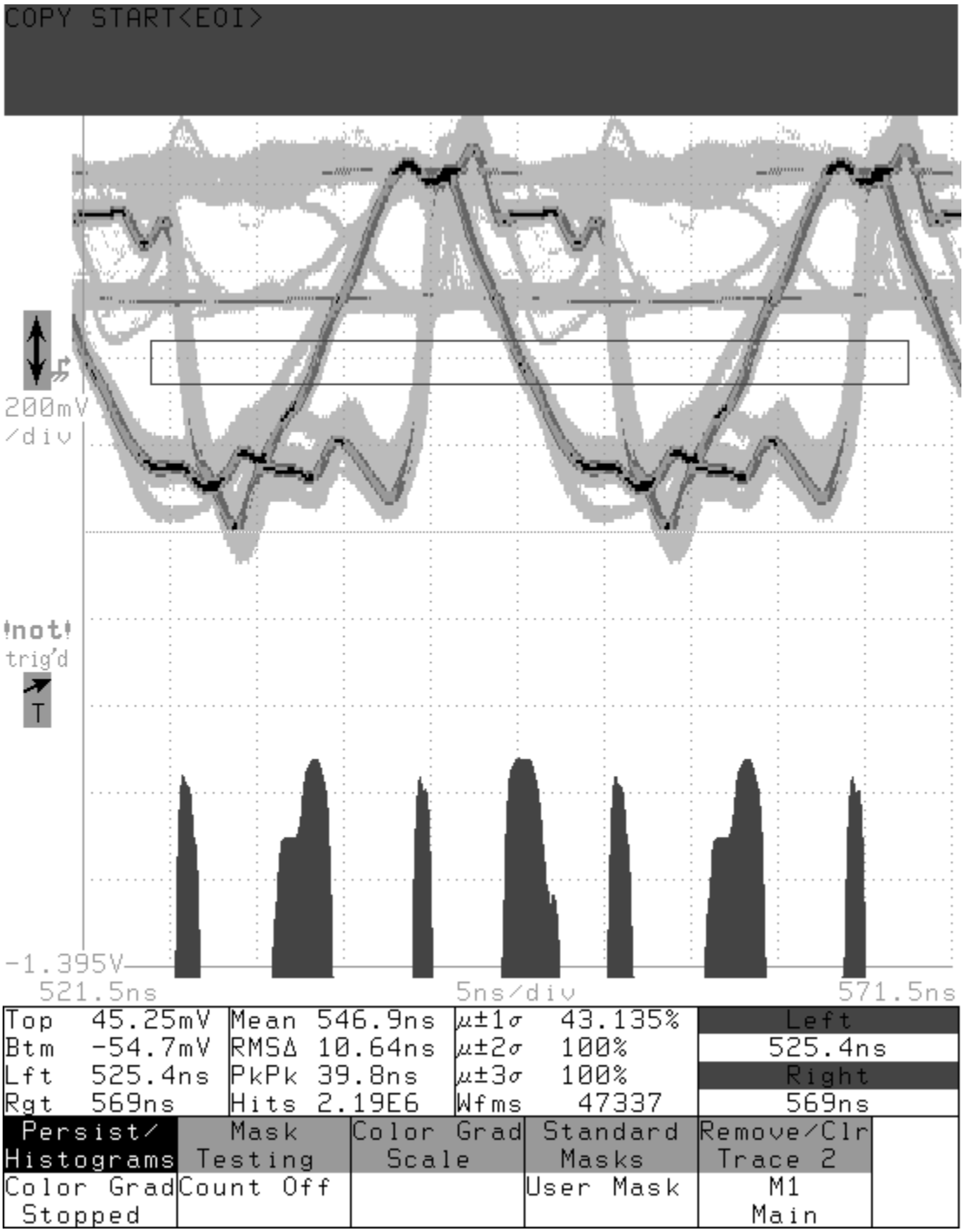

Figure 8 – Simulated hot-plugging with 2 million hits

Notes:

Figure 9 shows a hot-plugging induced failure.

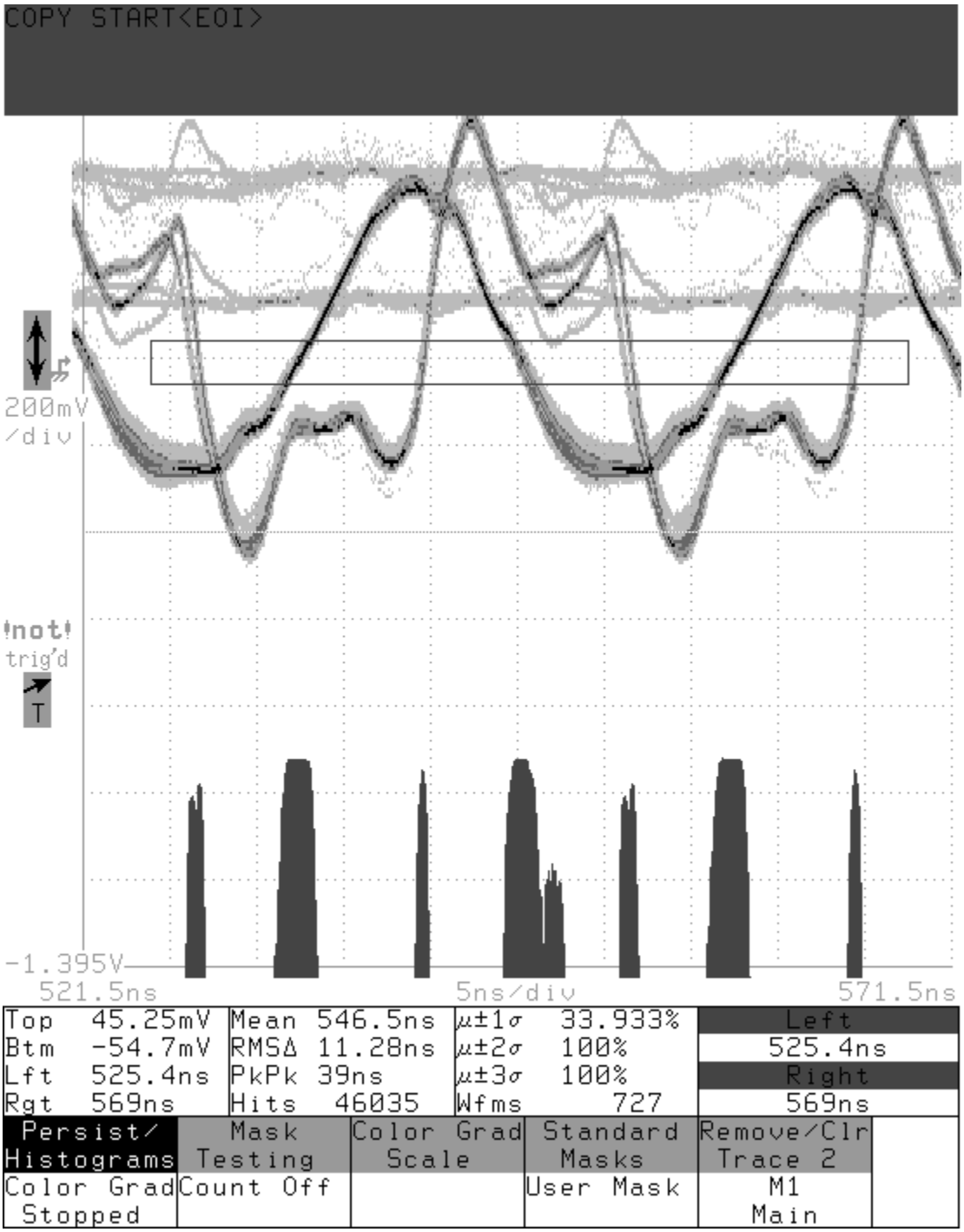

Figure 9 – Hot-plugging induced failure

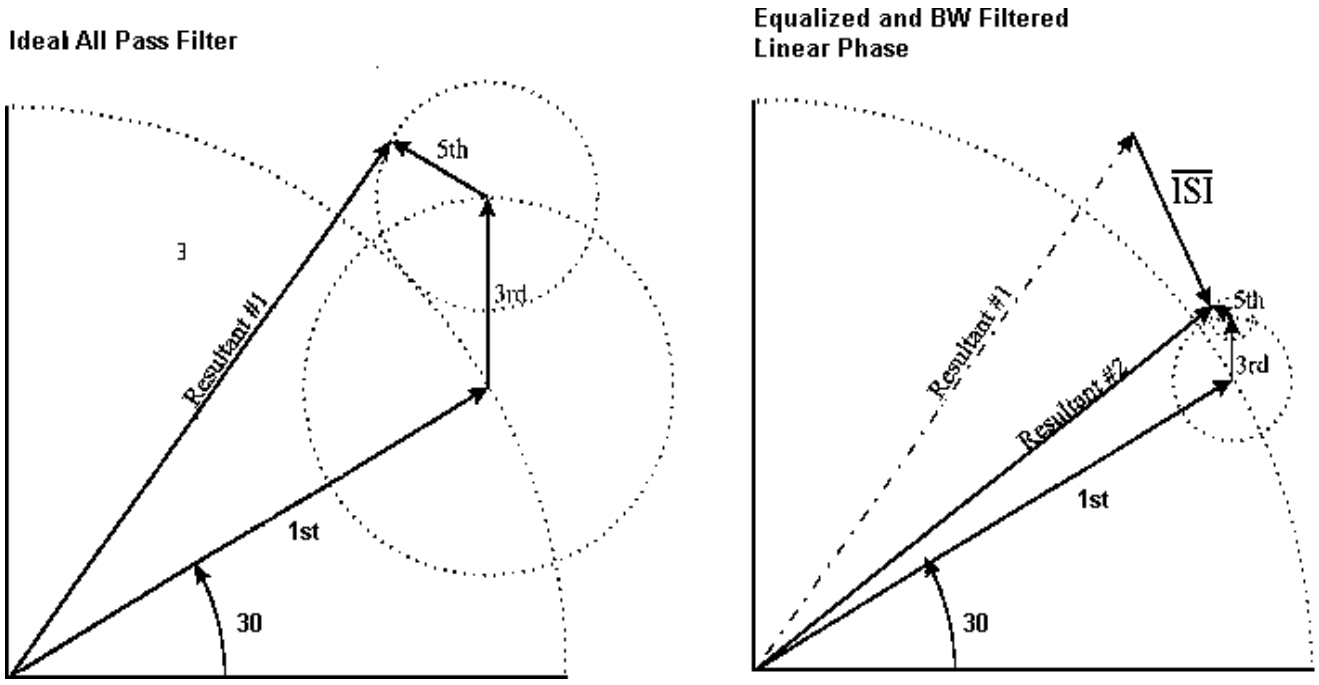

Figure 10 - Graphical Determination of Linear Phase ISI for Clock/Data Pattern

4 Summary and Recommendations

4.1 Summary

1. Dual-edge clock still seems to be the best solution
2. Cable skew and differential capacitance dominate offsets
3. Cable induced ISI still enigmatic – more data is being taken
4. The next step is ISI dual-edge test silicon to verify margin analysis
5. Jitter margin with nominal driver and skew control expected to be 2-6 ns
6. Hot-plugging is problematical – more test data is needed

4.2 Recommendations

1. Skew compensation or CRC for data signals
2. Staged resistance connector or ACK/REQ counters for hot-plugging