

Reduced Block Commands (RBC)

Draft Proposal (T10/97-260r0)

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Information technology — Reduced Block Commands

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American National Standard
for Information Systems –

Reduced Block Commands (RBC)

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Abstract

This standard specifies the functional requirements for the SCSI Reduced Block Commands (RBC). RBC provides a subset of SBC, yet permits SCSI block logical units such as flexible disks, rigid disks, optical disks, etc., to attach to computers and provides the definition for their use.

An annex is provided that contains information required to implement the Serial Bus Protocol - 2 (SBP-2) command and control protocol on block devices.

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Foreword (This foreword is not part of American National Standard NCITS.xxx -199x)

The Reduced Block Command set is designed to provide very efficient initiator-to-target operation of input/output logical units (disks, tapes, printers, etc.) by an operating system. RBC assumes that the underlying command-response protocol is SBP-2.

There are five annexes in this standard. Annexes and **Error! Reference source not found.** are normative and part of this standard. Annexes **Error! Reference source not found.**, **Error! Reference source not found.**, **Error! Reference source not found.** and **Error! Reference source not found.** are informative and are not considered part of this standard.

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Revision 0 (October 13, 1997)

First release of working draft. Created from prior work performed by the SBP-2 adhoc working group during 1996 and 1997.

American National Standard for Information Systems –

Reduced Block Commands (RBC)

1 Scope and purpose

1.1 Scope

This standard defines the reduced command set extensions to facilitate operation of RBC units. The clause(s) of this standard implemented in conjunction with the applicable clauses of SPC-2, fully specify the command set for RBC logical units.

The objectives of the Reduced Block Command set standard is to provide the following:

- a) Permit a host to communicate with a logical unit that declares itself to be an RBC logical unit in the Device Type field of the INQUIRY command response data.
- b) Define a limited set of commands and supported fields unique to this class of block logical units.
- c) Define a limited set of control commands and supported fields to manage the operation of RBC logical units.
- d) Application of RBC to devices supporting SBP-2.

1.2 Purpose

The purpose of this document is to provide a command set of reduced requirements and options from SBC for RBC logical units. The reduced command set is intended to more closely match the requirements and options necessary for simple block logical units. The command set is intended to place no restrictions on device performance. The initial focus of this command set is rigid disks and removable media devices attached to Serial Bus and utilizing SBP-2 for command and control.

2 Normative references

The standards named in this section contain provisions which, through reference in this text, constitute provisions of this American National Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision; parties to agreements based on this American National Standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

Copies of the following documents can be obtained from ANSI:

Approved ANSI standards;

Approved and draft regional and international standards (ISO, IEC, CEN/CENELEC and ITUT); and

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2.1 Approved references

The following approved ANSI, international and regional standards (ISO, IEC, CEN/CENELEC and ITUT) may be obtained from the international and regional organizations that control them.

IEEE Std 1394-1995, Standard for a High Performance Serial Bus

ISO/IEC 13213:1994, Control and Status Register (CSR) Architecture for Microcomputer Buses

2.2 References under development

At the time of publication, the following referenced standards were still under development.

IEEE P1394a, Draft Standard for a High Performance Serial Bus (Supplement)

T10 Project 1155D Serial Bus Protocol 2 (SBP-2)

T10 Project 1236D SCSI Primary Commands 2 (SPC-2)

3 Keywords and Notation

3.1 Keywords

Several keywords are used to differentiate levels of requirements and optionality, as follows:

3.1.1 expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.1.2 ignored: A keyword that describes bits, bytes, quadlets, octlets or fields whose values are not checked by the recipient.

3.1.3 mandatory: A keyword that indicates items required to be implemented as defined by this standard.

3.1.4 may: A keyword that indicates flexibility of choice with no implied preference.

3.1.5 non-volatile medium: A physical storage medium that retains data written to it for a subsequent read operation through power off/on cycles. An example of this is a disk within a device that stores data as magnetic field changes that do not require device power to exist.

3.1.6 optional: A keyword that describes features which are not required to be implemented by this standard. However, if any optional feature defined by the standard is implemented, it shall be implemented as defined by the standard.

3.1.7 shall: A keyword that indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this standard.

3.1.8 should: A keyword that denotes flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "is recommended."

3.2 Glossary

The following terms are used in this standard:

3.2.1 byte: Eight bits of data.

3.2.2 command block: Space reserved within an ORB to describe a command intended for a logical unit that controls device functions or the transfer of data to or from device medium. The format and meaning of command blocks are outside of the scope of SBP-2 and are command set- or device-dependent.

3.2.3 initial node space: The 256 terabytes of Serial Bus address space that is available to each node. Addresses within initial node space are 48 bits and are based at zero. The initial node space includes initial memory space, private space, initial register space and initial units space. See either ISO/IEC 13213:1994 or IEEE Std 1394-1995 for more information on address spaces.

3.2.4 initial register space: A two kilobyte portion of initial node space with a base address of FFFF F000 0000₁₆. Core registers defined by ISO/IEC 13213:1994 are located within initial register space as are Serial Bus-dependent registers defined by IEEE Std 1394-1995.

3.2.5 initial units space: A portion of initial node space with a base address of FFFF F000 0400₁₆. This places initial units space adjacent to and above initial register space. The CSR's and other facilities defined by unit architectures are expected to lie within this space.

3.2.6 kilobyte: A quantity of data equal to 2¹⁰ bytes.

3.2.7 logical unit: The part of the unit architecture that is an instance of a device model, e.g., mass storage, CD-ROM or printer. Targets implement one or more logical units; the device type of the logical units may differ.

3.2.8 login: The process by which an initiator obtains access to a set of target fetch agents. The target fetch agents and their control and status registers provide a mechanism for an initiator to signal ORB's to the target.

3.2.9 octlet: Eight bytes, or 64 bits, of data.

3.2.10 operation request block: A data structure fetched from system memory by a target in order to execute the command encapsulated within it.

3.2.11 quadlet: Four bytes, or 32 bits, of data.

3.2.12 receive: When any form of this verb is used in the context of Serial Bus primary packets, it indicates that the packet is made available to the transaction or application layers, *i.e.*, layers above the link layer. Neither a packet repeated by the PHY nor a packet examined by the link is "received" by the node unless the preceding is also true.

3.2.13 register: A term used to describe quadlet aligned addresses that may be read or written by Serial Bus transactions. In the context of this standard, the use of the term register does not imply a specific hardware implementation. For example, the behavior of registers may be emulated by a processor.

3.2.14 status block: A data structure written to system memory by a target when an operation request block has been completed.

3.2.15 system memory: The portions of any node's memory that are directly addressable by a Serial Bus address and which accepts, at a minimum, quadlet read and write access. Computers are the most common example of nodes that make system memory addressable from Serial Bus, but any node, including those usually thought of as peripheral devices, may have system memory.

3.2.16 transaction: An exchange between a requester and a responder that consists of a request and a response subaction. The request subaction transmits a Serial Bus transaction such as quadlet read, block write or lock, from the requesting node to the node intended to respond. Some Serial Bus commands include data as well as transaction codes. The response subaction returns completion status and sometimes data from the responding node to the requesting node.

3.2.17 unit: A component of a Serial Bus node that provides processing, memory, I/O or some other functionality. Once the node is initialized, the unit provides a CSR interface that is typically accessed by device driver software at an initiator. A node may have multiple units, which normally operate independently of each other. Within this standard, a unit is equivalent to a target.

3.2.18 unit architecture: The specification of the interface to and the services provided by a unit implemented within a Serial Bus node. This standard is a unit architecture for SBP-2 targets.

3.2.19 unit attention: A state that a logical unit maintains while it has unsolicited status information to report to one or more logged-in initiators. A unit attention condition shall be created as described elsewhere in this standard or in the applicable command set- and device-dependent documents. A unit

attention condition shall persist for a logged-in initiator until a) unsolicited status that reports the unit attention condition is successfully stored at the initiator or b) the initiator's login becomes invalid or is released. Logical units may queue unit attention conditions; after the first unit attention condition is cleared, another unit attention condition may exist.

3.3 Abbreviations

The following are abbreviations that are used in this standard:

CDB	Command descriptor block
CSR	Control and status register
EUI-64	Extended Unique Identifier, 64-bits
ORB	Operation request block
SBP-2	Serial Bus Protocol 2 (this standard itself)

3.4 Conventions

The following conventions should be understood by the reader in order to comprehend this standard.

3.4.1 Non-numeric values

- a) The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE).
- b) Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field.
- c) If a field is specified as not meaningful or it is to be ignored, the entity that receives the field shall not check that field.

3.4.2 Numeric values

Decimal, hexadecimal and, occasionally, binary numbers are used within this standard. By editorial convention, decimal numbers are most frequently used to represent quantities or counts. Addresses are uniformly represented by hexadecimal numbers. Hexadecimal numbers are also used when the value represented has an underlying structure that is more apparent in a hexadecimal format than in a decimal format. Binary numbers are used infrequently and generally limited to the representation of bit patterns within a field.

- a) Decimal numbers are represented by Arabic numerals without subscripts or by their English names.
- b) Hexadecimal numbers are represented by digits from the character set 0 – 9 and A – F followed by the subscript 16.
- c) Binary numbers are represented by digits from the character set 0 and 1 followed by the subscript 2.

For the sake of legibility, binary and hexadecimal numbers are separated into groups of four digits separated by spaces.

As an example, 42, 2A₁₆ and 0010 1010₂ all represent the same numeric value.

4 Reduced Block Commands

The Reduced Block Command set (RBC) for SCSI block device logical units is shown in Table 1. Each command is mandatory.

Table 1 - Reduce Block Command Set

Command Name	Opcode	Reference
INQUIRY	12 ₁₆	SPC-2
MODE SELECT	55 ₁₆	SPC-2
MODE SENSE	5A ₁₆	SPC-2
READ (10)	28 ₁₆	RBC
START/STOP UNIT	1B ₁₆	RBC
SYNCHRONIZE CACHE	35 ₁₆	RBC
TEST UNIT READY	00 ₁₆	SPC-2
WRITE (10)	2A ₁₆	RBC
WRITE AND VERIFY (10)	2E ₁₆	RBC
WRITE BUFFER	3B ₁₆	SPC-2

The Control byte (the last byte of the Command Descriptor Bytes) is described in SBP-2, Annex Q. In addition, the supported field and bit values are defined.

4.1 READ(10) Command

The READ(10) command (see Table 2) requests that the device transfer data to the initiator. The most recent data value written in the addressed logical block shall be returned.

Table 2 - READ(10) command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (28 ₁₆)							
1	Reserved			DPO = 0	FUA = 0	Reserved		RelAdr=0
2	(MSB)							
3	Logical Block Address							
4								
5								
6	Reserved							
7	(MSB)							
8	Transfer Length							
9	(LSB)							
9	Control							

The disable page out (DPO) bit shall be set to zero indicating that retention priority shall be determined by the device.

The Force Unit Access (FUA) bit shall be set to zero indicating that the device may satisfy the command by accessing the cache memory. For read operations, any logical blocks that are contained in the cache memory may be transferred to the initiator directly from the cache memory.

The Relative Address (RelAdr) bit is NOT supported.

The Logical Block Address field specifies the starting logical block address on the device for the read data to be accessed.

The Transfer Length field specifies the number of contiguous logical blocks of data that shall be transferred. A transfer length of zero indicates that no logical blocks shall be transferred. This condition shall not be considered an error. Any other value indicates the number of logical blocks that shall be transferred.

4.2 START STOP UNIT Command

The START STOP UNIT command (see Table 3) requests that the device enable or disable the logical unit for media access operations and controls certain power conditions.

Table 3 - START STOP UNIT command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (1B ₁₆)							
1	Reserved							Immed
2	Reserved							
3	Reserved							
4	Power Conditions				Reserved		LoEj	Start
5	Control							

An *Immediate* (Immed) bit of one indicates that status shall be returned as soon as the command descriptor block has been validated. An *Immed* bit of zero indicates that status shall be returned after the operation is completed.

The power conditions field requests the logical unit to be placed into the power condition defined in Table 4. If this field contains any value other than 0₁₆ then the Start and the LoEj bits shall be ignored.

The logical unit may notify the initiator of the change of power state via unsolicited status, depending on the value of the `unsolicited_status_enable` variable.

Table 4 - Power Condition Descriptions

Code	Description
0 ₁₆	No change in power conditions.
1 ₁₆	Place device in Active state
2 ₁₆	Place device in Idle state
3 ₁₆	Place device in Standby state
4 ₁₆	Reserved
5 ₁₆	Place device in Sleep state
6 ₁₆ - F ₁₆	Reserved

If the START STOP UNIT command is issued with the Power Conditions field set to 1₁₆, 2₁₆, or 3₁₆ the device shall terminate any command received that requires more power than allowed by the START

STOP UNIT command's most recent power condition setting with a CHECK CONDITION status, sense key of ILLEGAL REQUEST and sense code of POWER CONDITION ACTIVE.

If the START STOP UNIT command is issued with the Power Conditions field set to 5_{16} , the device shall ignore the Immediate bit.

Prior to entering the Sleep state or executing the STOP UNIT command, a SYNCHRONIZE CACHE operation shall be performed.

It is not an error to request a device be placed into the same power state that it currently occupies.

The *LOAD/EJECT* (LoEj) bit shall NOT be supported by simple hard disk drives.

A *Start* bit of zero requests that the device be stopped (media shall not be accessed by the initiator). A *Start* bit of one request the device be made ready for use.

4.3 SYNCHRONIZE CACHE Command

The SYNCHRONIZE CACHE command (see Table 5) ensures that logical blocks in cache have their most recent data value recorded on the physical medium. If a more recent data value for a logical block exists in the cache memory than on the physical medium, then the logical block from the cache memory shall be written to the physical medium. Logical blocks are not necessarily removed from the cache memory as a result of the synchronize cache operation. The SYNCHRONIZE CACHE function is also required implicitly by other functions as defined in other clauses of this standard.

Table 5 - SYNCHRONIZE CACHE command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (35_{16})							
1	Reserved					WCD	Immed=0	RelAdr=0
2	(MSB)							
3	Logical Block Address = 0000 0000							
4								
5	(LSB)							
6	Reserved							
7	(MSB)							
8	Number of Blocks = 0000							
9	(LSB)							
9	Control							

A *Write Cache Disable* (WCD) bit of zero specifies that the device server may return GOOD status for a WRITE command after successfully receiving the data and prior to having successfully written it to the

medium. A WCD bit of one specifies that the device shall return GOOD status for a WRITE command after successfully writing all of the data to the medium.

The Immediate (Immed) bit is NOT supported.

The Relative Address (RelAdr) bit is NOT supported.

The Logical Block Address field is NOT supported.

The Number Of Blocks field is NOT supported.

4.4 WRITE(10) Command

The WRITE(10) command (see Table 6) requests that the device write data transferred from the initiator to the medium.

Table 6 - WRITE(10) command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code ($2A_{16}$)							
1	Reserved			DPO = 0	FUA	Reserved		RelAdr=0
2	(MSB)							
3	Logical Block Address							
4								
5								
6								
7	(MSB)							
8	Transfer Length							
9	(LSB)							
9	Control							

The disable page out (DPO) bit shall be set to zero indicating that retention priority shall be determined by the device.

A Force Unit Access (FUA) bit of zero indicates that the device may satisfy the command by accessing the cache memory. For write operations, logical blocks may be transferred directly to the cache memory. GOOD status may be returned to the initiator prior to writing the logical blocks to the medium. Any error that occurs after the GOOD status is returned is a deferred error, and information regarding the error is not reported until a subsequent command.

An FUA bit of one indicates that the device shall access the media in performing the command prior to returning GOOD status. Write commands shall not return GOOD status until the logical blocks have actually been written on the media (i.e. the data is not write cached).

The Relative Address (RelAdr) bit is NOT supported.

The Logical Block Address field specifies the starting logical block address on the device for the read data to be accessed.

The Transfer Length field specifies the number of contiguous logical blocks of data that shall be transferred. A transfer length of zero indicates that no logical blocks shall be transferred. This condition shall not be considered an error. Any other value indicates the number of logical blocks that shall be transferred.

4.5 WRITE AND VERIFY Command

The WRITE AND VERIFY command (see Table 7) requests that the device write the data transferred from the initiator to the medium and then verify that the data is correctly written. The data is only transferred once from the application client to the device server.

Table 7 - WRITE AND VERIFY command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code ($2E_{16}$)							
1	Reserved			DPO = 0	Reserved		BytChk=0	RelAdr=0
2	(MSB)							
3	Logical Block Address							
4								
5								
6								
7	(MSB)							
8	Transfer Length							
9	Transfer Length							
9	(LSB)							
9	Control							

The disable page out (DPO) bit shall be set to zero indicating that retention priority shall be determined by the device.

The byte check (BytChk) bit shall be set to zero requesting a medium verification to be performed with no data comparison

The Relative Address (RelAdr) bit is NOT supported.

The Logical Block Address field specifies the starting logical block address on the device for the read data to be accessed.

The Transfer Length field specifies the number of contiguous logical blocks of data that shall be transferred. A transfer length of zero indicates that no logical blocks shall be transferred. This condition

shall not be considered an error. Any other value indicates the number of logical blocks that shall be transferred.

4.6 MODE SELECT/SENSE page parameters

The RBC Device Parameters page is intended to provide general configuration information and to modify that configuration where necessary.

Table 8 -RBC Device Parameters Page Format (3E₁₆)

Bit Byte	7	6	5	4	3	2	1	0
0	PS = 1	Rsvd	Page Code (3E ₁₆)					
1	Page Length (8 ₁₆)							
2	Reserved							WCD
3	(MSB)	Logical Block Size						
4	Logical Block Size						(LSB)	
5	(MSB)	Number of Logical Blocks						
6								
7								
8								
9	Number of Logical Blocks						(LSB)	

Write Cache Enable (WCD) reflects the setting of the WCD bit in the SYNCHRONIZE CACHE command.

(This bit is NOT changeable)

The *Logical Block Size* field indicates the number of use data bytes contained in a logical block.

(This field is NOT changeable)

The *Number of Logical Blocks* field indicates the number of logical blocks contained in the user data area. **(This field is changeable)**

NOTE – The default Number of Logical Blocks value may be obtained by requesting the Default Mode Sense data for this page. The current Number of Logical Blocks value may be obtained by requesting the Saved Mode Sense data for this page.

Annex A

SPC-2 Compliance for Simple SBP-2 Disk Drives

(Normative)

Table 9 - SPC-2 commands for simple SBP-2 Disk Drives

Command Name	Opcode	Reference
INQUIRY	12 ₁₆	SPC-2
MODE SELECT	55 ₁₆	SPC-2
MODE SENSE	5A ₁₆	SPC-2
TEST UNIT READY	00 ₁₆	SPC-2
WRITE BUFFER	3B ₁₆	SPC-2

A.1 MODE SELECT(10) Command

The MODE SELECT(10) command provides a means for the initiator to specify device parameters to the mass storage device. Devices shall also implement the MODE SENSE(10) command.

Table 10 - MODE SELECT(10) command format

Bit Byte	7	6	5	4	3	2	1	0	
0	Operation Code (55 ₁₆)								
1				PF = 1				SP = 1	
2	Reserved								
3	Reserved								
4	Reserved								
5	Reserved								
6	Reserved								
7	(MSB)	Parameter list length							
8	Parameter list length						(LSB)		
9	Control								

The Page Format (PF) bit shall be set to one, indicating that all parameters following the header are structured as pages of related parameters and are specified in this standard.

The Save Pages (SP) bit shall be set to one, indicating that the device shall perform the specified MODE SELECT operation and shall save, to a non-volatile vendor-specific location, all the *changeable* pages, including any sent with the command.

The Parameter List Length field specifies the length, in bytes, of the mode parameter list that shall be transferred in the MODE SELECT parameter read data request from the device. A Parameter List Length of zero shall not be considered an error.

If the Parameter List Length results in the truncation of any mode parameter header or mode page, the device shall terminate the command with CHECK CONDITION status, set the sense key to ILLEGAL REQUEST, and the sense code to PARAMETER LIST LENGTH ERROR.

The device shall terminate the MODE SELECT command with CHECK CONDITION status, set the sense key to ILLEGAL REQUEST, set the sense code to INVALID FIELDS IN PARAMETER LIST, and refrain from changing any mode parameters for the following conditions:

- a) If the initiator sets any field in the mode parameter header to an unsupported value.
- b) If an initiator sends a mode page with a page length not equal to the page length returned by the MODE SENSE command for that page;
- c) If the initiator sends an unsupported value for a mode parameter and rounding is not implemented for that parameter.

A device may alter any mode parameter in any mode page as a result of changes to other mode parameters.

The device shall NOT validate the non-changeable parameters against the current values that existed for those mode parameters prior to executing the MODE SELECT command.

A.2 MODE SENSE(10) Command

Table 11 - MODE SENSE(10) command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (5A ₁₆)							
1					DBD = 1			
2	PC		Page Code					
3	Reserved							
4	Reserved							
5	Reserved							
6	Reserved							
7	(MSB)		Allocation length					
8					Allocation length		(LSB)	
9	Control							

The Disable Block Descriptors (DBD) bit shall be set to one, indicating that the device shall not return any block descriptors in the returned MODE SENSE data.

The Page Control (PC) field defines the type of mode parameter values to be returned in the mode pages. The Page Control field is defined in Table 12.

Table 12 - Simple Hard Disk Page Control Values

Code	Type of parameter	Support
00 _b	Current	Optional
01 _b	Changeable	Not supported
10 _b	Default	Mandatory
11 _b	Saved	Mandatory

NOTE – RBC devices only support Saved and Default parameter values. Since the SP bit is required to be one for the MODE SELECT command, Current and Saved values are the same.

An initiator may request any one or all of the supported mode pages from the device. If an initiator issues a MODE SENSE command with a Page Code value not implemented by the device, the device shall return CHECK CONDITION status, set the sense key to ILLEGAL REQUEST and set the sense code to INVALID FIELD IN CDB.

A Page Code of $3F_{16}$ indicates that all mode pages implemented by the device shall be returned to the initiator. If the mode parameter list exceeds 65 536 bytes, the device shall return CHECK CONDITION status, set the sense key to ILLEGAL REQUEST and set the sense code to INVALID FIELD IN CDB.

Mode pages should be returned in ascending Page Code order.

A.2.1 Current Values (00_b)

If an RBC logical unit returns values when current values are requested, those values shall be the same as saved values.

A.2.2 Changeable Values (01_b)

Changeable values shall not be supported by RBC logical units.

A.2.3 Default Values (10_b)

Unsupported parameters shall be set to zero. Default values should be accessible even if the device is not ready.

A.2.4 Saved Values (11_b)

Unsupported parameters shall be set to zero.

NOTE – The method of saving parameters is vendor-specific. The parameters shall be preserved in such a manner that they are retained when the device is powered down.

A.2.5 Initial Response

After a power-up condition or hard reset condition, the device shall respond in the following manner:

- a) If default values are requested, report the default values;
- b) If saved values are requested, report valid restored mode parameters, or restore the mode parameters and report them. If the saved values of the mode parameters are not able to be accessed from the non-volatile vendor-specific location, terminate the command with CHECK CONDITION status and set the sense key to NOT READY.
- c) If current values are requested, report saved values as described in b).

A.3 TEST UNIT READY Command

The TEST UNIT READY command (see Table 13) provides a means to check if the device is ready. This is not a request for a self-test. If the device is able to accept an appropriate medium-access command without returning CHECK CONDITION status, this command shall return GOOD status. If the device cannot become operational or is in a state such that an application client action (e.g., START UNIT command) is required to make the unit ready, the device shall return CHECK CONDITION status with a sense key of NOT READY.

Table 13 - TEST UNIT READY command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (00 ₁₆)							
1	Reserved							
2	Reserved							
3	Reserved							
4	Reserved							
5	Control							

Table 14 defines the suggested GOOD and CHECK CONDITION status responses to the TEST UNIT READY command. Other conditions, including deferred errors, may result in other responses (e.g., BUSY status).

RBC devices shall report SMART status via the TEST UNIT READY status response. The required Key, Code and ASCQ values are described in Table 14 and Table 15.

Table 14 - Preferred TEST UNIT READY sense values

Status	Sense Key	ASC, ASCQ
00 ₁₆ - Good	00 ₁₆ - No Sense	00 ₁₆ , 00 ₁₆ - No additional sense information
02 ₁₆ - Check Condition	05 ₁₆ - Illegal Request	25 ₁₆ , 00 ₁₆ - Logical Unit not supported
02 ₁₆ - Check Condition	02 ₁₆ - Not Ready	04 ₁₆ , 00 ₁₆ - Logical Unit not ready cause not reportable
02 ₁₆ - Check Condition	02 ₁₆ - Not Ready	04 ₁₆ , 01 ₁₆ - Logical Unit becoming ready
02 ₁₆ - Check Condition	01 ₁₆ - Recovered Error	5D ₁₆ , ¹ - SMART threshold exceeded,

NOTE 1 - See Table 15 for SMART ASCQ responses.

Table 15 - SMART ASCQ values

Value	Definition
X0 ₁₆	General hard drive failure
X1 ₁₆	Drive Error threshold exceeding limits.
X2 ₁₆	Data Error Rate exceeding limits.
X3 ₁₆	Seek Error Rate exceeding limits.
X4 ₁₆	LBA reassignment exceeding limits.
X5 ₁₆	Access Times exceeding limits.
X6 ₁₆	Start Unit Times exceeding limits.
X7 ₁₆	Channel parametrics indicate impending failure
X8 ₁₆	Controller detected impending failure.
X9 ₁₆	Throughput performance
XA ₁₆	Seek time performance
XB ₁₆	Spin-up retry count
XC ₁₆	Drive calibration retry count
0D ₁₆ - 0F ₁₆	Reserved
1X ₁₆	Hardware impending failure
2X ₁₆	Controller impending failure
3X ₁₆	Data Channel impending failure
4X ₁₆	Servo impending failure
5X ₁₆	Spindle impending failure
6X ₁₆	Firmware impending failure
7X ₁₆ - FX ₁₆	Reserved

A.4 WRITE BUFFER Command

The WRITE BUFFER command (see Table 16) is used to download and save microcode.

Table 16 - WRITE BUFFER command format

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (3B ₁₆)							
1	Reserved					Mode		
2	Buffer ID							
3	(MSB)							
4	Buffer Offset							
5								
	(MSB)							
7	Parameter List Length							
8								
9	Control							

The function of this command and the meaning of the fields within the command descriptor block depend on the contents of the Mode field. The Mode field is defined in Table 17.

Table 17 - WRITE BUFFER Mode field

Mode	Description	Implementation Requirements
000 _b	Write combined header and data	Not Supported
001 _b	Vendor specific	Vendor specific
010 _b	Write data	Not Supported
011 _b	Reserved	Reserved
100 _b	Download microcode	Not Supported
101 _b	Download microcode and save	Mandatory
110 _b	Download microcode with offset	Not Supported
111 _b	Download microcode with offset and save	Not Supported

A.4.1 Download Microcode and Save Mode (101_b)

If the logical unit cannot accept this command because of some device condition, the device shall terminate each WRITE BUFFER command with this mode (101_b) with a CHECK CONDITION status, a sense key of ILLEGAL REQUEST, and an additional sense code of COMMAND SEQUENCE ERROR.

In this mode, vendor-specific microcode or control information shall be transferred to the device and, if the WRITE BUFFER command is completed successfully, also shall be saved in a non-volatile memory space (semiconductor, disk, or other). The downloaded code shall then be effective after each power-cycle and reset until it is supplanted in another download microcode and save operation. The meaning of the Buffer ID, Buffer Offset, and Parameter List Length fields are not specified by this standard and are not required to be zero filled. When the download microcode and save command has completed successfully the device server shall generate a Unit Attention status block and send it, via unsolicited status, to all initiators except the one that issued the WRITE BUFFER command. When reporting the Unit Attention condition, the device shall set the additional sense code to MICROCODE HAS BEEN CHANGED.

A.5 Event Status Notification

Previous mass storage device interfaces have been unable to consistently and reliably support asynchronous event notification. As a substitute, initiators have used the GET EVENT STATUS NOTIFICATION command to acquire asynchronous event status from devices. The GESN command was used to either poll the device's event status or, if the device supported queued commands, the GESN command did not complete until an event occurred. The polling method requires the initiator to provide a timer in order to repetitively acquire device status. The queued command method requires a device to process the GESN command in a different manner from all other queued commands. To solve this problem asynchronous event notification has been made a fundamental part of SBP-2 and RBC devices.

Through the use of Unsolicited Status, mass storage devices may report asynchronous events the moment that they occur. The initiator need only process the status block to determine the cause of the event. The device is no longer required to support the GESN command in the polled or queued mode. It simply builds and transmits a status block whenever an event occurs.

A.5.1 Unsolicited Status Sense Definitions

The following table describes unsolicited status sense key and sense code values that may be written to an initiator's Status_FIFO if the initiator has previously written to the device's `unsolicited_status_enable` register.

Table 18 - Unsolicited Status Sense Key/Code Values

Sense Key	Sense Code	Description
02 ₁₆	04 ₁₆	Device Not Ready (reported only on transition or at power on.)
06 ₁₆	28 ₁₆	Not Ready to Ready transition. Medium may have changed
06 ₁₆	29 ₁₆	Power on reset, bus reset, etc.

Deferred errors may also be reported as unsolicited status.

A.5.1.1 Event Status Sense Information

In order to support traditional Event Status Notification through the use of Unsolicited Status, specific Status, Sense Key, and Sense Code values must be combined.

Status = 02₁₆, Check Condition, indicates that the condition of the device has changed.

Sense Key = 06₁₆, Unit Attention, indicates that an event has occurred that the device must communicate to the initiator.

Sense Code = 7F₁₆, Event Status Notification, indicates that an asynchronous event has occurred.

Sense Qualifier values are:

- 02₁₆, Power Management Class Event, indicates that a Power Management event has occurred.
- 04₁₆, Media Class Event, indicates that a Media Class event has occurred.
- 06₁₆, Device Busy Class Event, indicates that a Device Busy Class event has occurred.

The contents of the Information field further define the event status. Interpretation of the values are dependent upon the Sense Key, Code, and Qualifier values. The following tables provide the Event Status Information values for each Sense Qualifier type described above.

information			
byte 0	byte 1	byte 2	byte 3
event	status	event specific	event specific

Figure 1 - Event Status Information Format

A.5.1.2 Power Management Information Values

information			
byte 0	byte 1	byte 2	byte 3
event	status	reserved	reserved

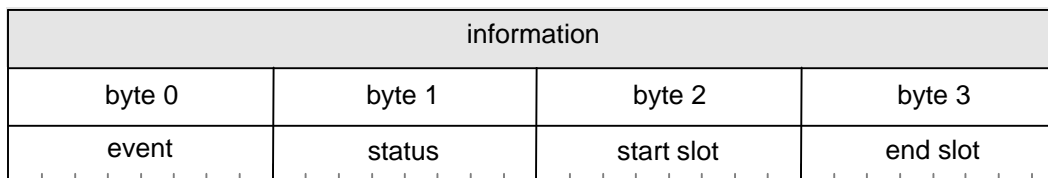
Figure 2 - Power Management Information Format

Table 19 - Power Management Information Values - Event Field

Event Field	Description
00 ₁₆	No power state change
01 ₁₆	The device successfully changed to the specified power state.
02 ₁₆	The device failed to enter the last requested power state and is still operating at the state specified in the Power Status field.
03 ₁₆ - FF ₁₆	Reserved

Table 20 - Power Management Information Values - Status Field

Status Field	Description
00 ₁₆	Reserved
01 ₁₆	The device is in the Active state
02 ₁₆	The device is in the Idle state
03 ₁₆	The device is in the Standby state
04 ₁₆ - FF ₁₆	Reserved

A.5.1.3 Media Event Information Values**Figure 3 - Media Event Information Format****Table 21 - Media Event Information Value - Event Field**

Event Field	Description
00 ₁₆	Media status is unchanged
01 ₁₆	Eject request. The user has issued a request to eject the slot or media
02 ₁₆	The specified slot has received new media and the media is ready to be accessed.
03 ₁₆	Media Removal. The media has been removed from the specified slot and the target is unable to access the media without user intervention.
04 ₁₆ - FF ₁₆	Reserved

Table 22 - Media Event Information Value - Status Field

Bit Byte	7	6	5	4	3	2	1	0
1	Reserved						Media Present	Door or Tray Open

The **Door or Tray Open bit** indicates the mechanical position of the device's door or tray. A **Door or Tray Open** value of 1 indicates that the door or tray is open. A value of 0 indicates that the door or tray is closed.

The **Media Present** bit indicates whether media is installed in the device. A value of 1 indicates that media is present in the device. A value of 0 indicates that no media is present. The **Media Present** bit is reported independently from the Door or Tray Open bit. If the device cannot report the media state while the door or tray is open, this bit shall be set to 0 when the Door or Tray Open bit is 0.

The **Start Slot** field defines the first slot of a multiple slot device that the media status notification applies to. For devices that do not support multiple slots, this field shall be reserved.

The **End Slot** field defines the last slot of a multiple slot device that the media status notification applies to. For devices that do not support multiple slots, this field shall be reserved.

A.5.1.4 Device Busy Event Information Values

information			
byte 0	byte 1	byte 2	byte 3
event	status	Time (MSB)	Time (LSB)

Figure 4 - Device Busy Information Format**Table 23 - Device Busy Event Information Values - Event Field**

Event Field	Description
00 ₁₆	No event is available
01 ₁₆	A time-out has occurred
02 ₁₆ - FF ₁₆	Reserved

Table 24 - Device Busy Event Information Values - Status Field

Status Field	Description
00 ₁₆	No event. The device is ready to accept commands
01 ₁₆	The device is in the process of waking up from a lower power state
02 ₁₆	The device is in the process of completing an earlier command
03 ₁₆	The device is in the process of completing a deferred operation, such as a write.
04 ₁₆ - FF ₁₆	Reserved

The **Time** field is the predicted amount of time remaining for the device to become not busy, in unit of 100ms.

Annex B

RBC Logical Unit Configuration ROM Requirements

(normative)

Although most Configuration ROM entries are generic, several contain information that is specific to each device type. Hard disk drive specific Configuration ROM information is defined in this section.

B.1 Unit Directory - Command_Set

The *Command_Set* entry (key - $3A_{16}$) is an immediate entry that, in combination with the *Command_Set_Spec_ID* entry specifies the command set supported by the unit.



Figure 5 - Command_Set entry

B.2 Unit Directory - Command_Set_Revision

The *Command_Set_Revision* entry (key - $3B_{16}$) is an immediate entry that specifies the current revision level of the command set implemented by the unit.

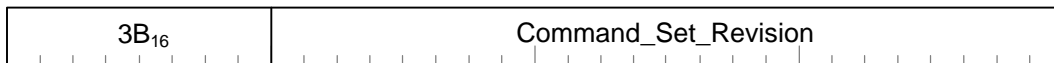


Figure 6 - Command_Set_Revision entry

B.3 Unit Directory - Logical_Unit_Number

The *Logical_Unit_Number* entry (key - 14_{16}) is an immediate entry that specifies the device type and the logical unit number of a logical unit supported by the drive. The format of this entry is defined in SBP-2 and duplicated here with additional field information for hard disk drives.

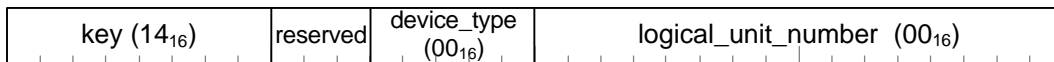


Figure 7 - Logical_Unit_Number entry

The *device_type* field indicates the peripheral device type implemented by the logical unit. The value defined by the command set for hard disk drives is 00_{16} .

The *logical_unit_number* field indicates the value of a logical unit supported by the drive. For hard disk drives that support one logical unit, the value is 0000_{16} .

B.4 Node Power Directory

Note - The power management entries described below are preliminary. Use their definitions at your own risk.

The Node Power Directory describes the power characteristics of the node and the offset of the Node Power Management CSRs in the node's address space.

Block	Description						
Node Power Directory	Node Power Directory Length				Directory CRC (calculated)		
	Node_Power_Level key 30 ₁₆	v	w	lv	voltage	reserved	power_requirements
	Cable_Power_Source_Level key 30 ₁₆	v	r	lv	voltage	reserved	power_requirements
	Node_Power_Mgmt key 70 ₁₆	Node_Power_Management_CSR offset					

Figure 8 - Node Power Directory Sample

B.4.1 Node_Power_Level

The *Node Power Directory* shall contain a *Node_Power_Level* entry for each different voltage and power level required by the node .

The *valid* bit (*v*) shall be one if the information contained in the *voltage* and *power_requirements* fields is valid.

The *wakeup* bit (*w*) shall NOT be supported by Mass Storage Devices and shall be set to zero.

The *power level* field (*lv*) shall specify the power level, 0-3, for each *Node_Power_Level* entry.

The *voltage* field shall specify the voltage at which the power value specified in the *power_requirements* field shall be supplied to the node, as defined in the following table:

Table 25 - Voltage Field Definition

Value	Description
0	Power shall be supplied within the tolerances for cable power specified by IEEE std 1394-1995
1	Power shall be supplied at +3.3V DC
2	Power shall be supplied at +5.0V DC
3	Power shall be supplied at +12.0V DC
4-F ₁₆	Reserved for future specification

The *power_requirements* field shall specify, in deciwatts, the amount of power that the node consumes when operating at the power level, specified by *lvl*, and the voltage level, specified by *voltage*.

NOTE – A device may be required to support a matrix of *lvl*, *voltage* and *power_requirements*. In the worst case, a device may be requested to deliver *power_requirements* for 2^6 combinations of *lvl* and *voltage* values.

B.4.2 Cable_Power_Source_Level entry

The *Cable_Power_Source_Level* entry is an immediate entry in the node power directory that describes the Serial Bus cable power sourcing characteristics of the node at a specified cable power source level. There shall be one *Cable_Power_Source_Level* entry for each cable power source level implemented by the node.

The *valid* bit (*v*) shall be one if the information contained in the *voltage* and *power_requirements* fields is valid.

The *power_level* field (*lvl*) shall specify the cable power source level, 0-3, for each *Cable_Power_Source_Level* entry.

The *voltage* field shall specify the voltage at which the power value specified in the *power_requirements* field shall be supplied to the Serial Bus cable, as defined in the following table:

Table 26 - Voltage Field Definition

Value	Description
0	Power is supplied within the tolerances for cable power specified by IEEE std 1394-1995
1	Power is supplied at +12.0V DC
2-F ₁₆	Reserved for future specification

The *power_requirements* field shall specify, in deciwatts, the amount of power that the node sources to the Serial Bus while operating at the cable power source level, specified by *lvl*, and the voltage level, specified by *voltage*.

NOTE – A device may be required to support a matrix of *lvl*, *voltage* and *power_requirements*. In the worst case, a device may be requested to deliver *power_requirements* for 2^6 combinations of *lvl* and *voltage* values.

B.4.3 Node_Power_Management_CSR offset

The *Node_Power_Management_CSR_offset* entry is an immediate entry that specifies the offset, from the base address, of the node's power management registers.

B.5 Unit Power Directory

The Unit Power Directory specifies the power characteristics of the unit and the offset of the Unit Power Management CSRs in the node's address space.

Block	Offset	Description	
Unit Power Directory	49C ₁₆	Unit Power Directory Length	Directory CRC (calculated)
	4A0 ₁₆	Unit_Power_Level_Key 30 ₁₆	v w lV voltage reserved power_requirements
	4A4 ₁₆	Unit_Power_Mgmt_key 70 ₁₆	Unit_Power_Management_CSR_offset

Figure 9 - Unit Power Directory Sample

B.5.1 Unit_Power_Level

The *Unit Power Directory* shall contain a *Unit_Power_Level* entry for each different voltage and power level required by the unit .

The *valid* bit (*v*) shall be one if the information contained in the *voltage* and *power_requirements* fields is valid.

The *wakeup* bit (*w*) shall NOT be supported by Mass Storage Devices.

The *power level* field (*lV*) shall specify the power level for each *Unit_Power_Level* entry..

The *voltage* field shall specify the voltage associated with the power value specified in the *power_requirements* field.

Table 27 - Voltage Field Definition

Value	Description
0	Power shall be supplied within the tolerances for cable power specified by IEEE std 1394-1995
1	Power shall be supplied at +3.3V DC
2	Power shall be supplied at +5.0V DC
3	Power shall be supplied at +12.0V DC
4-F ₁₆	Reserved

The *power_requirements* field shall specify, in deciwatts, the amount of power that the unit consumes when operating at the power level, specified by *lV*, and the voltage level, specified by *voltage*.

NOTE – A device may be required to support a matrix of *lV*, *voltage* and *power_requirements*. In the worst case, a device may be requested to deliver *power_requirements* for 2⁵ combinations of *lV* and *voltage* values.

B.5.2 Unit_Power_Management_CSR_offset

The *Unit_Power_Management_CSR_offset* entry is an immediate entry that specifies the offset, from the base address, of the unit's power management registers.

Annex C

RBC Logical Unit Serial Bus CSR Requirements

(normative)

Control and Status Registers are used to determine the state of a device or control its operation. CSRs required to implement a mass storage device, that are not described in SBP-2, or that require additional information than that contained in SBP-2 are described in the following section.

C.1 Node Power Management Registers

Note - The power management CSRs described below are preliminary. Use their definitions at your own risk.

The 1394 Trade Association Specification for Power Management defines a set of CSRs required to allow initiators to control device power usage. These registers shall lie within initial units space and shall be located at or above address FFF F001 0000₁₆ within the node's 48-bit address range. The relative relationship of these registers is fixed within a contiguous block of four quadlets, as defined by the table below.

The base address of the set of power management registers is obtained from the Node_Power_Management entry in the node's Configuration ROM, Node_Power_Directory.

Although the Power Management specification defines registers that permit device power modes to be modified, mass storage devices are not required to support this feature. Mass storage devices shall, at a minimum, provide node power state status.

Table 28 - Node Power Management registers

Offset	Register name	Implementation Requirement	Description
00 ₁₆	Node_Power_State	Mandatory	Reports the node's current power state
04 ₁₆	Node_Power_Control	Not Supported	Permits the node's power state to be managed
08 ₁₆	Notification_Address	Not Supported	The 64-bit destination address for a power status change notification or request.
0C ₁₆	Cable_Power_Source	Optional	Reports the node's present cable power sourcing capabilities
10 ₁₆	Cable_Power_Source Control	Not Supported	Permits the node's cable power sourcing capabilities to be managed

D.1.1 Node_Power_State register

The *Node_Power_State* register is a read-only register that provides information about the node's current power status. The definition of the register is shown in the figure below.



Figure 10 - Node_Power_State register format

The *lvl* field shall specify the unit's power level, D0 - D3.

The *valid* bit (*v*) shall be one if the information contained in the *src*, *voltage*, and *power* fields is valid. If this bit is zero, the contents of none of these fields may be considered valid.

If the *valid* bit is one, the *src* field shall specify the node's power source, according to the values encoded in the table below.

Table 29 - SRC field values

Value	Function
0	The node is powered from the Serial Bus cable
1	The node is powered from its own battery
2	The node is powered from electric mains
3	Reserved for future specification

The *wake_source* bit (*k*) shall NOT be supported by Mass Storage Devices and shall be set to zero.

If the *valid* bit is one, and the *src* field contains a value of zero, the *voltage* field shall be valid. If the *src* field contains a value of zero, the *voltage* field shall specify the minimum, voltage level required by the node, in decivolts.

If the *valid* bit is one, the *power* field shall specify, in deciwatts, the amount of power the node is utilizing.

C.1.2 Cable_Power_Source_State register

The Cable_Power_Source_State register is a read-only register that provides information about the node's current cable power sourcing status. The definition of this register is given by the figure below.



Figure 11 - Node_Power_State register format

The *lvl* field shall specify the node's cable power sourcing level, 0-3.

The *valid* bit (*v*) shall be one if the information contained in the *voltage*, and *power* fields is valid. If this bit is zero, the contents of none of these fields may be considered valid.

If the *valid* bit is one, the *voltage* field shall specify the minimum voltage level provided by the node, in decivolts.

If the *valid* bit is one, the *power* field shall specify, in deciwatts, the amount of power the node is providing.

C.2 Unit Power Management Registers

The 1394 Trade Association Specification for Power Management defines a set of CSRs required to allow initiators to control device power usage. These register shall lie within initial units space and shall be located at or above address FFFF F001 0000₁₆ within the node's 48-bit address range. The relative relationship of these registers is fixed within a contiguous block of four quadlets, as defined by the table below.

Although the Power Management specification defines registers that permit device power modes to be modified, mass storage devices are not required to support this feature. Mass storage devices shall, at a minimum, provide unit power state status.

Table 30 - Unit Power Management registers

Offset	Register name	Implementation Requirement	Description
00 ₁₆	Unit_Power_State	Mandatory	Reports the unit's current power state
04 ₁₆	Unit_Power_Control	Not Supported	Permits the unit's power state to be managed
08 ₁₆			Reserved for future specification
0C ₁₆			Reserved for future specification
10 ₁₆			Reserved for future specification
18 ₁₆	Notification_Address	Not Supported	The 64-bit destination address for a power status change notification or request.

C.2.1 Unit_Power_State Register

The *Unit_Power_State* register is a read-only register that provides information about the unit's current power status. The definition of the register is shown in the figure below.

The base address of the set of power management registers is obtained from the *Unit_Power_Management* entry in the unit's Configuration ROM, *Unit_Power_Directory*.



Figure 12 - Unit_Power_State register format

The *lvl* field shall specify the unit's power level, 0-3.

The *valid* bit (*v*) shall be one if the information contained in the *src*, *voltage* and *power* fields is valid. If this bit is zero, the contents of none of these fields may be considered valid.

If the *valid* bit is one, the *src* field shall specify the unit's power source, according to the values encoded in the table below.

Table 31 - SRC field values

Value	Function
0	The unit is powered from the Node's power source
1	The unit is powered from its own battery
2	The unit is powered from electric mains
3	The unit is the power source for the node. Disabling this unit may result in loss of this power to both the node and Serial Bus.

The *wake_source* bit (k) shall NOT be supported by Mass Storage Devices and shall be set to zero.

If the *valid* bit is one, and the *src* field contains a value of zero or three, the *voltage* field shall be valid. If the *src* field contains a value of zero, the *voltage* field shall specify the minimum, voltage level required by the node, in volts. If the *src* field contains a value of three, the voltage field shall specify the voltage level provided by the unit. In both cases the voltage indicated is that used in determining the number of deciwatts indicated.

If the *valid* bit is one, the *power* field shall specify, in deciwatts, the amount of power the unit is utilizing or providing.

Annex D

RBC Logical Unit Security Requirements

(normative)

RBC Logical Units shall implement security against unauthorized media access as defined in the security annex of SBP-2.

The master password, referenced in SBP-2, is contained in INQUIRY command, Vital Product Data page 80₁₆. Following a successful Login operation, the host must request that the device perform the INQUIRY command, in order to obtain the device's serial number.

Annex E

SBP-2 Storage Model

(informative)

E.1 Model Configuration

This configuration is used only as an example of a common implementation. The following assumptions are made for this model configuration.

- * The device supports a single logical unit.
- * The device does not support multiple initiators.
- * The device does not support isochronous data transfers.

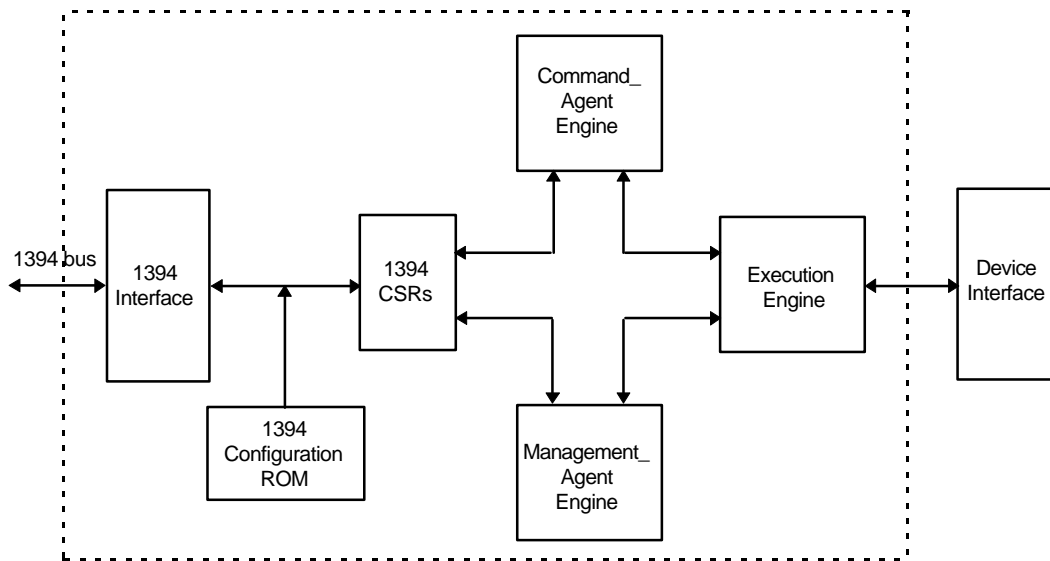


Figure 13 - Mass Storage Interface Block Diagram

E.2 Model Operation

The block diagram in Figure 13 indicates the functional blocks contained in a mass storage device that supports SBP-2. This section describes the function of those blocks when processing a list of ORBs. The ORBs contain READ commands in this example.

After power-on or bus reset, the Command_Agent and Management_Agent engines are in the Reset state.

The initiator reads the device's Configuration ROM data in order to determine its 1394 capabilities, SBP-2 capabilities, EUI-64 value, command set identifiers, software versions, and Management_Agent CSR address.

The initiator performs a Login operation prior to any request to the device. To perform a Login, the initiator writes its Login ORB address to the Management_Agent register. This specification requires that the Login ORB contain either the current or master password for the Login to be successful. The device returns the Login response to the bus address specified in the Login ORB. One field of the Login response contains the Command_Agent's CSR base address.

Prior to initiating command transfers, the initiator builds a list of Command_Block ORBs in system memory. The list may be as short as one ORB, but this example assumes a list length of more than one. The last ORB in the list contains a NULL Next_ORB pointer which indicates the end of the list to the device's Command_Agent fetch engine.

To transition the Command_Agent state from Reset to Active the initiator writes the offset of the first ORB in the ORB list to the device's ORB_Pointer CSR address. This allows the Command_Agent fetch engine to begin fetching ORBs from initiator memory. If the initiator writes to the Doorbell CSR, the device will ignore the Doorbell at this time.

The device fetches ORBs until its ORB space is full or until an ORB containing a NULL Next_ORB pointer is fetched. Fetched ORBs are routed to the Execution engine. The Execution engine may reorder the commands contained in the ORBs for best performance.

As each READ command is executed the device transfers READ data to the initiator's memory space via block write requests.

Following the data transfer portion of each command the device writes a Status Block to the initiator's Status_FIFO address. The Status_FIFO address for Command Block ORBs is contained in the Login ORB. The status block contains SBP-2 specific command information as well as general sense information.

If an ORB containing a Null Next_ORB pointer is fetched the Execution engine completes all fetched commands, including the one in the just fetched ORB, before the Command_Agent transitions to the Suspended state.

If additional commands are to be executed, the initiator creates a new list of Command_Block ORBs; changes the Next_ORB pointer in the last ORB of the old list from NULL to the offset of the first ORB in the new list; then writes to the device's Doorbell CSR address. This transitions the Command_Agent to the Active state.

The device fetches the new Next_ORB pointer value from the last ORB of the old list and begins fetching ORBS from the new list at that offset.

If the Command_Agent fetch engine has not reached the ORB containing a Null Next_ORB pointer, (and is still in the Active state) the device ignores any writes to the Doorbell CSR address.

This sequence may continue until the device is reset, power is removed, or an error occurs.