To: T10 Membership
From: Lawrence J. Lamers (ljlamers@corp.adaptec.com)
Subject: SPI-3 Protocol INQUIRY data
Date: Thursday, May 07, 1998

1. SPI-3 Protocol INQUIRY data

Table 19 Standard INQUIRY data format

Byte	Bit 7	6	5	4	3	2	1	Bit 0
0	Peripheral qualifier			Peripheral device type				
1	RMB	Reserved	Reserved	Reserved	Reserved			
2	ISO/IEC version		ECMA version			ANSI version		
3	AERC	TrmTsk	NormACA	Reserved	Response data format			
4	Additional length (n-4)							
5	Reserved	Reserved	Reserved	Reserved	Reserved	DEC	QAS	PP
6	Reserved	EncServ	VS	MultiP	MChngr	ACKREQQ	Addr32	Addr16
7	RelAdr	WBus32	WBus16	Sync	Linked	TranDis	CmdQue	VS
8	Vendor identification							
15								
16	Product identification							
31								
32	Product revision level							
35								
36	Vendor-specific							
55								
56	Reserved							
95								
96	Vendor-specific parameters							
n								

A double-edge clocking (DEC) bit of one indicates that the device server supports double-edge clocking. A value of zero indicates that the device server does not support double-edge clocking.

A packet protocol (PP) bit of one indicates that the device server supports the packet protocol. A value of zero indicates that the device server does not support the packet protocol.

A quick arbitrate select (QAS) bit of one indicates that the device server supports the quick arbitrate select feature. A value of zero indicates that the device server does not support the quick arbitrate select feature.

2. MODE SENSE Data

Table 98 Control mode page

Byte	Bit 7	6	5	4	3	2	1	Bit 0
0	PS	Reserved	Page Code (0Ah)					
1	Page Length (0Ah)							
2	Reserved	Reserved	Reserved	ECRC	EQAS	DFA	GLTSD	RLEC
3	Queue algorithm modifier				Reserved	Reserved	QERR	DQUE
4	Reserved	RAC	Reserved	Reserved	SWP	RAERP	UAAERP	EAERP
5	Reserved							
6	Ready AER holdoff period							
7								
8	Busy timeout period							
9								
10	Reserved							
11	Reserved							

A disable fairness algorithm (DFA) if set disables the fairness algorithm during arbitration; if cleared enables the fairness algorithm during arbitration.

An enable QAS (EQAS) if set enables QAS; if cleared disables QAS.

An enable CRC (ECRC) if set enables CRC; if cleared disables CRC.