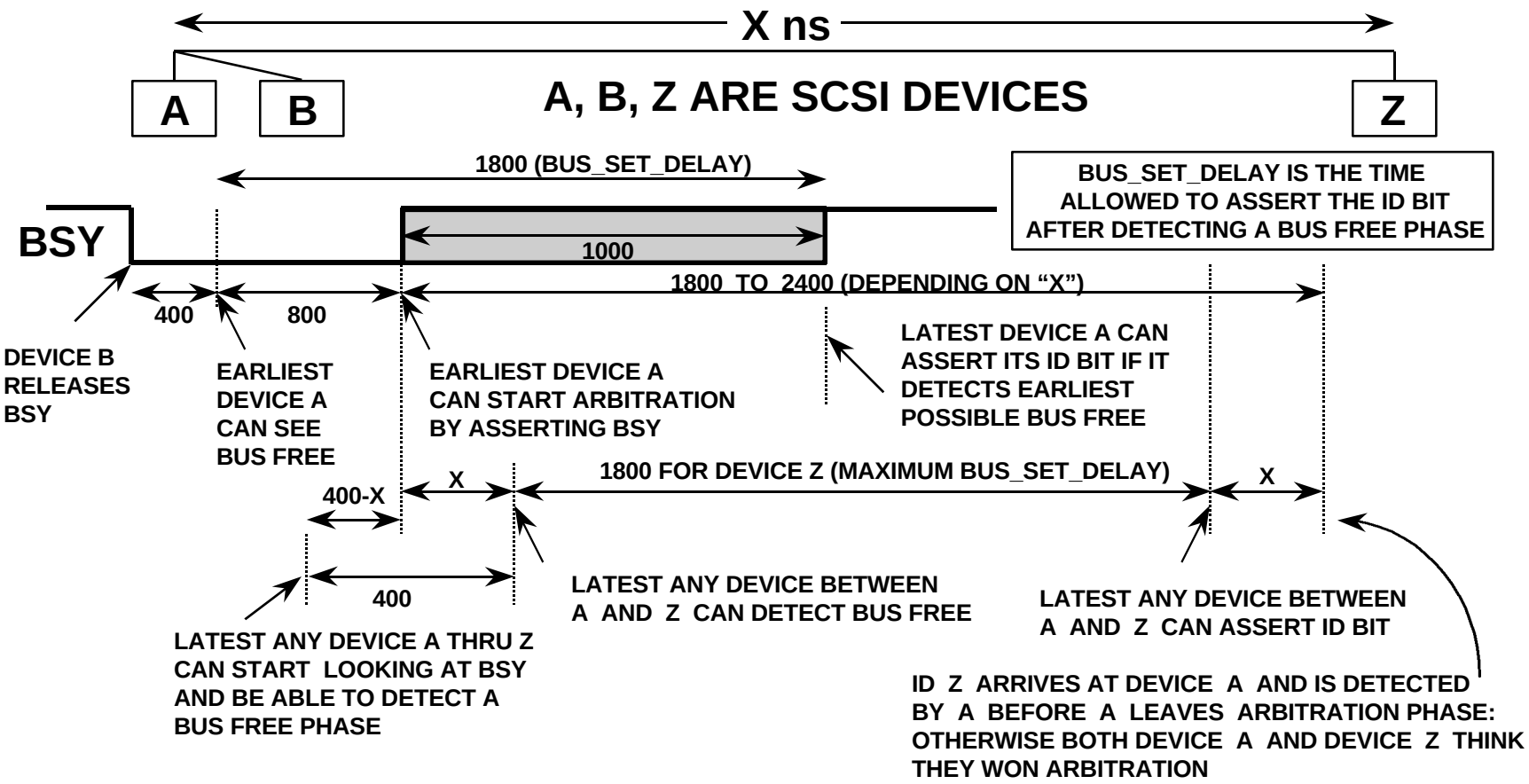
EFFECT OF BUS_SET_DELAY ON MAXIMUM DOMAIN DELAY

T10/97-223r0



WORST CASE UNDER ABOVE ASSUMPTIONS: 2X + 1800 = 2400 => X = 300 ns

NEED TO REDUCE MAXIMUM BUS_SET_DELAY TO 1600 ns OR LESS
IN ORDER TO RECOVER THE FULL 400 ns PROPAGATION TIME ALLOWED
BY THE BUS SETTLE DELAY

THIS SHOULD NOT BE A PROBLEM FOR ANY MODERN DEVICES THAT USE
KNOWN CLOCK RATES AS THEIR RESPONSE TO BUS FREE
AND DESIRE TO ARBITRATE WILL BE VERY FAST

Motion to change bus_set_delay in SPI-2

- **Motion: that SPI-2 require 1600ns maximum for bus_set_delay**
- **Note: this is a 200 ns reduction from the present 1800ns that does not affect any recently designed devices (per working group discussions) [these devices actually do not need anywhere near the full 1800ns but only the 200ns reduction needed is requested to minimize impact on much older devices in large domains]**
- **Note: this change allows the maximum worst case domain delay to be the bus_settle_delay limit of 400 ns -- with the present 1800ns for bus_set_delay (and devices that use the entire 1800ns) the domain delay is reduced to 300ns**