To: T10 T10/97-215r0
From: Bill Ham, Digital Equipment
Subject: SCSI receiver glitch filter requirements for SPI-2
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The following requirements are proposed for SPI-2 SCSI receiver glitch filters. The term “filters” is used in this document to provide continuity to the discussions in the working group. The wording in the standard should not use these terms but rather be a description of the performance requirements.

The performance requirements proposed are:

During the synchronous data phase the receiver shall not respond to detected changes in input logic state during a blank-out period after the initial logic state change is detected. The initial state change is any detected logic state change during the synchronous data phase not occurring during a blank-out period. The blank-out period duration is indicated in Table 1.

Table 1 - Blank-out times for receivers operating in synchronous data phase

Data phase speed	Minimum blank-out time (ns) after initial detection of the input logic state change indicated	
	Assertion to negation	Negation to assertion
Fast (10)	10 **	10
Fast 20	7	7
Fast 40	4	4
** already a requirement in SPI		

Note: during the SCSI working group meeting on July 14, 1997 there was much discussion on the best way to specify this performance requirement for “glitch filters”. Among the points raised were different numbers (IBM proposed 7,5,3 instead of 10,7,4), the concept of describing the characteristics of the optimum “filter” based on the available pulses widths at different speeds, extending the speed range to slow and acync, and making this whole issue a recommendation - not a requirement. There was nearly unanimous agreement that there should be a significant discussion of making receivers more robust somewhere in the SPI-2 document.

Tak Asami proposed the following wording as an alternate:

It is strongly suggested that all SCSI devices incorporate the glitch filter function on REQ and ACK receiver inputs such that:

Reduce or eliminate the effect of glitch pulses after detection of either assertion or negation transistion edges

Since the width of the glitch pulse does not scale with DATA phase speed the detected glitch may occur at different relative positions within the pulse - for this reason the greater fraction of the pulse period that is protected by the filter the greater the protection

The filter period should never be so long as to mask out the subsequent transition edges of the incoming REQ/ACK signals