Basic Idea Is To Use Dual Edge Clocking

- Keeps frequency same as 40
 - -- Frequency related loss issues highest concern



- Changes:
 - 28 gauge mandatory
 - Reduce bias voltage
 - -- Was based on assumptions no longer valid
 - Decide on way to solve ISI problem which is also problem with NRZ data string
 - Use expanders for backplane impedance control

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- Reduce Distance
 - Verify loss in MP and PP configurations
 - Keep loss to less than 6 db over all MP and PP configurations
 - Require 28 gauge as minimum
 - Suggest 6 m MP since this is original SCSI distance

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- Reduced Bias Voltage
 - Bias voltage based on 20 microamps leakage of 16 devices
 - More realistic number 10 microamps
 - Could reduce to 30 mv (extreme lower limit)
 - Provides 70 mv more margin

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- Inter-Symbol Interference Problem
 - Shown before that is issue with clock line
 - Using dual edge clock may be issue with data lines
 - Long 1 or 0 string may cause data to have first pulse problem
 - Propose variable strength driver to resolve this on clock
 - To be determined if needed on data lines

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Use Expanders For Backplane Impedance Matching

- Due to impedance discontinuity expander is solution at these frequencies (with retiming)
- Cost usually not an issue with backplanes and complex sysmtems

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Concerns:

- DC bias due to NRZ code
 - -- NRZ code with long 1 or 0 string may not be detected on first transition
- Possible solutions
 - -- Try to eliminate with multi-strength drivers on each data line
 - -- Could be eliminated with encoding, but would reduce transfer rate and increase gate count

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- Concerns:
 - Setup and hold timing
 - -- Reduced by half, since data frequency 2X
 - Possible solutions
 - -- Reason to reduce distance is to cut data line to clock line skew
 - -- High quality cables
 - Or could consider compensation scheme as done in HIPPI but would require changes to way data phase done

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SKEW



