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TO: T10 SBP-2 ad hoc Working Group

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RE: Configuration ROM, power reset and security

The text below reflects agreements reached by the SBP-2 *ad hoc* working group. These changes affect stabilized portions of the SBP-2 draft; consequently they are being held until the July T10 plenary in Colorado Springs, CO, for final approval and inclusion in the subsequent revision of SBP-2.

The following two clauses are to be added just before existing 7.1, "Bus information block".

# 7.1 Power reset initialization

During the initialization process that follows a power reset a target may not be able to respond to Serial Bus request subactions addressed to all of configuration ROM. When the target has insufficient information to make general format configuration ROM accessible, it shall return a response value of zero for any quadlet read addressed to FFFF F000 0400<sub>16</sub> (the first quadlet of configuration ROM).

NOTE – An alternative to the return of zeros for the first quadlet of configuration ROM is to acknowledge request subactions with *ack\_tardy*, as specified by draft standard P1394a.

Targets shall complete initialization within five seconds of a power reset. Once power reset initialization completes, the target shall make all mandatory configuration ROM available in the general format described in the clauses that follow. The target should not initiate a Serial Bus reset solely as a consequence of the completion of power on reset initialization.

Additional, optional configuration ROM information, such as textual descriptor leaves that identify the target vendor and model, may not be available when power reset initialization completes. In such cases the target may add this information to configuration ROM as it becomes available and may initiate a Serial Bus reset to alert the initiator to the changed configuration ROM. The target should initiate a Serial Bus reset if there is no reasonable expectation that the initiator would otherwise become aware of changed configuration ROM.

# 7.2 ROM CRC coverage

The ROM CRC in the first quadlet of general format configuration ROM shall be calculated over the entire length of entries present within the range FFFF F000 0400<sub>16</sub> through FFFF F000 07FC<sub>16</sub>, inclusive.

The following clause is to be added to the description of entries in the unit directory.

#### 7.3.6 Firmware\_Revision entry

The Firmware Revision entry is an immediate entry that, when present in the unit directory, specifies the firmware revision level implemented by the target. Figure 50 shows the format of this entry.

most significant	least significant
<u>3C<sub>16</sub></u>	firmware_revision

# Figure 50 – Firmware Revision entry format

<u>3B<sub>16</sub> is the concatenation of key type and key value for the Firmware Revision entry.</u>

The meaning of *firmware\_revision* shall be specified by the manufacturer of the target.

The following clauses are to be deleted. These changes anticipate redefinition of configuration ROM required entries to be addressed by IEEE P1212, the five-year revision of the existing CSR architecture.

#### 7.2.3 Node\_Unique\_ID entry

The Node\_Unique\_ID entry is a leaf entry in the root directory that describes the location of the node unique ID leaf within configuration ROM. Figure 43 shows the format of this entry.

most significant	least significan
8D <sub>16</sub>	indirect_offset

# Figure 43 – Node\_Unique\_ID entry format

8D<sub>16</sub> is the concatenation of *key\_type* and *key\_value* for the Node\_Unique\_ID entry.

The *indirect\_offset* field specifies the number of quadlets from the address of the Node\_Unique\_ID entry to the address of the node unique ID leaf within configuration ROM.

#### 7.5 Node unique ID leaf

As specified by ISO/IEC 13213:1994, the node unique ID is a 64-bit number appended to a company ID value to create a globally unique 88-bit number. While conforming to this definition, Serial Bus additionally constrains the 64-bit node unique ID values so that they are unique within the global context of all Serial Bus nodes. Figure 56 shows the format of the node unique ID leaf.



least significant

#### Figure 56 – Node unique ID leaf format

The first quadlet of the node unique leaf shall contain the number of following quadlets in the leaf and a CRC calculated for those quadlets, as specified by ISO/IEC 13213:1994.

The node\_vendor\_ID value shall be the same as the module\_vendor\_ID value from the root directory.

The *chip\_ID\_hi* field is concatenated with the *chip\_ID\_lo* field to create a 40-bit chip ID value. The vendor specified by the *node\_vendor\_ID* value shall administer the chip ID values. When appended to the

node\_vendor\_ID value, these shall form a unique 64-bit value called EUI-64 (Extended Unique Identifier, 64-bits). These EUI-64 values are, by definition, unique from other EUI-64 identifiers derived from the IEEE/RAC-provided company ID value.

The sample configuration ROM in informative Annex B is to be changed to reflect the above additions and deletions.

The following text is to be added to Annex A, Minimum Serial Bus node capabilities.

Once a target completes its power reset initialization sequence, it shall acknowledge, and subsequently respond to, Serial Bus transaction request subactions within the time limits specified by IEEE Std 1394-1995 and draft standard P1394a. A Serial Bus reset, by itself, shall not alter a target's responsiveness to request subactions.

NOTE – While initializing after a power reset, a target should respond to quadlet read requests addressed to FFFF F000 0400<sub>16</sub> with a response data value of zero. This indicates that the remainder of configuration ROM, as well as other target CSR's, are not accessible.

As mandated by draft standard P1394a, a target shall abide by the following restrictions:

- <u>The value returned for a target's unique ID, EUI-64, if read from the configuration ROM bus</u> information block by quadlet read requests, shall be that assigned at the time of manufacture;
- The target shall not originate any asynchronous request or response packets with a source\_ID field that is not equal to either a) the most significant 16 bits of the target's NODE\_IDS register or b) the concatenation of 3FF<sub>16</sub> (the local bus ID) and the physical ID assigned to the target's PHY during the self-identify process; and
- The target shall not receive any asynchronous request or response packet unless the destination\_ID field is equal to either a) the concatenation of the most significant 10 bits of the target's NODE\_IDS register and either the physical ID assigned to the target's PHY during the self-identify process or 3F<sub>16</sub> (the broadcast physical ID), or b) the concatenation of 3FE<sub>16</sub> (the local *bus ID*) and either the physical ID assigned to the target's PHY during the self-identify process or 3F<sub>16</sub> (the broadcast physical ID).