To: T10 Membership T10/97-181r0

Subject: Presentation on LVD results

Date: 5/2/97

Talk about the wedgy effect, show measured data (used data in 97-178)

Go over list of 10 differences between A & S

Explain why the dual receiver approach adds so little capacitence

Answer back from last months minutes about “what is a prefect symmetrical driver”

Ten Problems that Asymmetrical Drivers with Bias Voltage Termination Have, that are not there for Symmetrical Drivers with No Bias Voltage Termination

1.0 ΔI problems (designed into the driver):

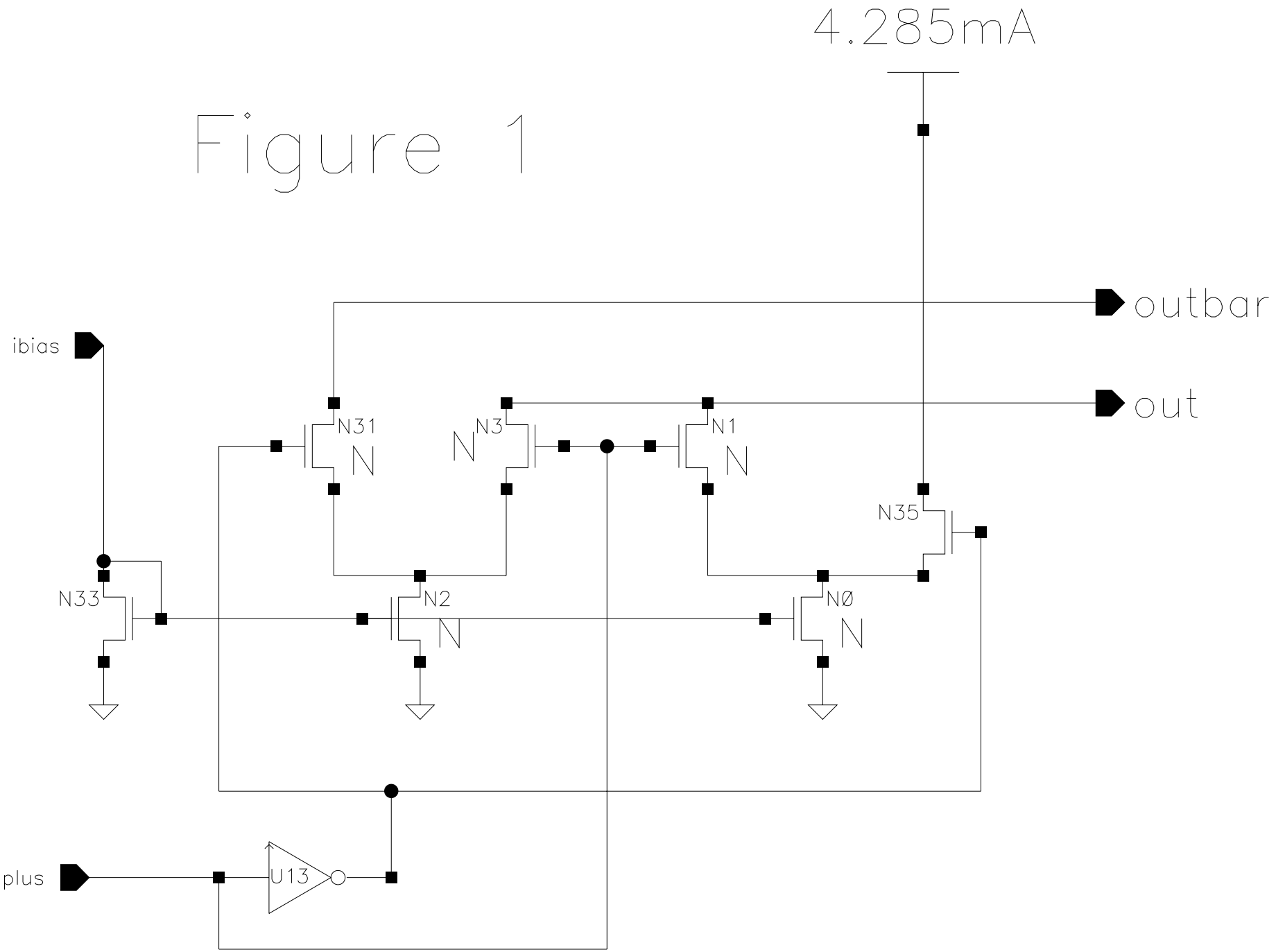
1.1 $\Delta I * Z_0 = \Delta V$, ΔV varies as a function of cable Z_0, but ΔI varies independently as a function of circuit design and process tolerance for the LVD driver.

1.2 ΔI causes modulation in the common mode bias point of the termination. The size of this effect is a function of the driver output resistance. The higher the output resistance the less the modulation effect.

1.3 Unequal output currents creates greater RFI or EMI (radio frequency interference, electromagnetic interference). This has not been measured.

1.4 For a good current mode design (this doesn't apply to voltage mode drivers), extra current or power is needed to create lower impedance reference voltages to bias the current source transistors. Or, you need extra power to have a separate bias distribution system for the offset current. The charge coupling from gate to source/drain overlap capacitance is unequal as the outputs switch back and forth from high current to low current, and the unequal charges, create a short term accuracy problem (unless you have a low impedance bias voltage driving all your current sources). Also, for the offset current

Figure 1



mirror transistors, they turn on & off, and that couples into the bias voltage with a greater effect than the overlap capacitances do. See figure 1. This applies only if you try to do a really good current mode output design.

1.4.1 By comparison, the low speed offset receiver needs to use only about 250uA max.

2.0 ∆V problems, 0 reference shift, "wedgy effect" (designed into the terminator):

2.1 Cause a 0 shift (with respect to the reference) when the cable has any loss, (and maybe even we there is no loss).

2.1.1 At higher frequencies

2.1.2 At long cable lengths

2.1.3 Because of reflections

2.1.4 Because of cable Z_0 changes due to loading variations, going in & out of boxes or backplanes.

2.1.5 Trying to do a case 4 hot plug.

3.0 ∆R problems (designed into the terminator, part 3.1, & was called the "thought experiment" previously, part 3.2):

3.1 When data signals start and stop, the system goes from AC to DC and back and forth. Since AC cable Z_0 are different from DC resistive termination, fluctuations on the signal levels will happen. Part of this will be the

same whether or not you have asymmetrical or symmetrical drivers. But, their will be an additional component of noise for the asymmetrical drivers, that the symmetrical drivers don't have. This component of extra noise for the asymmetrical driver is because of item 1.1 above, $\Delta I * Z_0 = \Delta V$ for the cable, and $\Delta I * \Delta R = \Delta V$ for the terminator.

3.2 Early SCSI had no active negation, and it was found to be better to have active negation. If you can drive the cable evenly in both directions, that is best. With the bias termination/asymmetrical drive setup now, the resistor is doing ~40% of the driving for negation. How much impact this has, if any has not been determined yet. But it is something where asymmetrical is different than symmetrical and it is noted here for that reason.

This could also be the reason that explains why we have the wedgy effect.

4.0 Mis-match tolerances between 1.0, 2.0 & 3.0 above:

4.1 Because scsi devices and terminators from many different companies must work all together on the same SCSI bus, large tolerance must be designed into the specification (SPI-2). When devices end up at the limits of the specifications because the tolerances can and will, go to the limits. All the inherit problems above are made even worse by this.

5.0 Excessive power dissipation:

5.1 Also, due to all of the above, the lowest operating output voltage swing must be increased, causing more power dissipation. Note that maximum voltage swing for 1394 is less than our minimum voltage swing.

6.0 Nobody else is doing this:

6.1 Show me just 1 public, high-speed interface standard that does this! I can't find any, 1394, fiber channel (I'm not French), ATM, & 10,100, & gigabit ethernet are all symmetrical. (I basically hate this kind of argument, but I think it is valid in this case, because there are no positive reason why we are doing asymmetrical.)

7.0 Doesn't work at 80mhz:

7.1 The asymmetrical approach has no future unless we push the power even higher, probably doubling it. Or, we will need to tighten the current spec to the point where you need a 1% tolerance off chip current bias.

adaptec, Bill Ham from DEC and Dave Steele from Symbios all agreed that everything asymmetrical that was shown in the April, '97 working group meeting didn't work. And it was agreed that you can't use the 40mhz specification to do testing at 80mhz because it won't work and your data isn't valid. No one has shown for cases other than lumped loads that symmetrical doesn't work at 80mhz. I don't have any problem with

For this table mid-point values are used,
bias=0.1125 volts & Rterminatio = 105 ohms

vswing,	Inegate ma,	Iassert ma,	diff ma,	ratio	
.27	3	7.285	4.285	2.4285	
.273	3.057	7.342	4.285	2.4018	
.275	3.095	7.38	4.285	2.3846	
.3	3.571	7.857	4.285	2.1999	
.313	3.819	8.104	4.285	2.1221	
.318	3.914	8.199	4.285	2.0948	
.325	4.047	8.333	4.285	2.0588	
.3415	4.361	8.647	4.285	1.9825	
.35	4.523	8.809	4.285	1.9473	
.3694	4.893	9.179	4.285	1.8758	
.375	5	9.285	4.285	1.8571	
.3865	5.219	9.504	4.285	1.8211	
.4	5.476	9.761	4.285	1.7826	
.425	5.952	10.238	4.285	1.72	
.45	6.428	10.714	4.285	1.6666	
.455	6.523	10.809	4.285	1.6569	+/- 40%
.475	6.904	11.19	4.285	1.6206	
.5	7.38	11.666	4.285	1.5806	
.525	7.857	12.142	4.285	1.5454	
.55	8.333	12.619	4.285	1.5142	
.575	8.809	13.095	4.285	1.4864	
.592	9.133	13.419	4.285	1.4692	
.6	9.285	13.571	4.285	1.4615	
.625	9.761	14.047	4.285	1.439	
.637	9.99	14.276	4.285	1.42891	
.64	10.047	14.333	4.285	1.4265	
.273	3.057	7.342	4.285	2.4018	
.455	6.523	10.809	4.285	1.6569	.455 +/- 40%
.637	9.99	14.276	4.285	1.42891	
.318	3.914	8.199	4.285	2.0948	
.455	6.523	10.809	4.285	1.6569	6.523 +/- 40%
.592	9.133	13.419	4.285	1.4692	

example of a worst case design point

vswing,	Inegate ma,	Iassert ma,	diff ma,	ratio	
.3865	5.219	9.504	4.285	1.8211	
.3865	5.219	8.6464	4.285	1.6569	
.3415	4.361	8.647	4.285	1.9825	
.455	6.523	10.809	4.285	1.6569	6.523 +/- 20%

For this point with vbias = 125mV,
Va=(.3415-0.0125=0.329 volts)
Vn=(.3865+0.0125=0.399 volts)

Example Worst Case Design Point

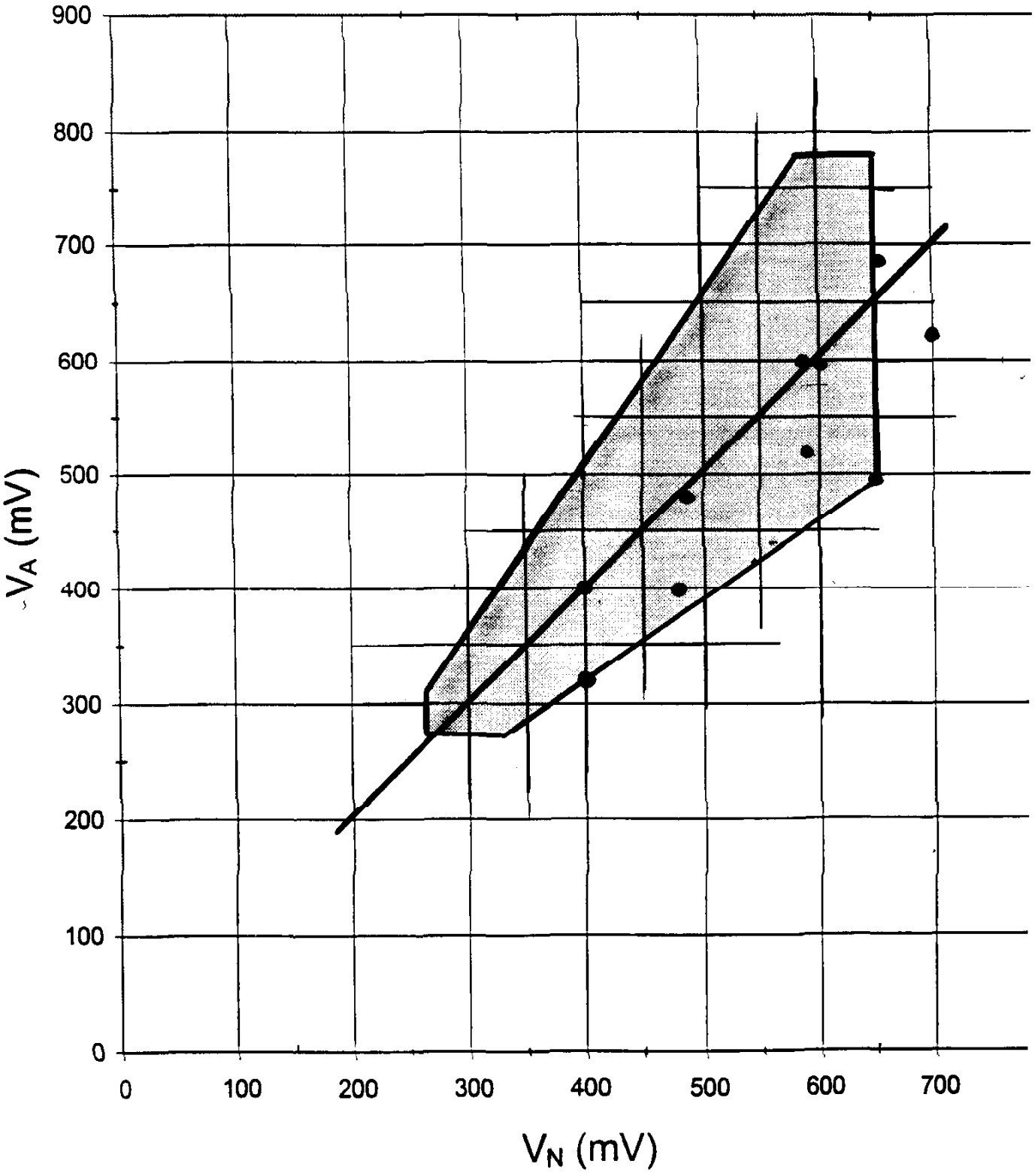
Table 1:

vswing	Inegate ma	I assert ma	diff ma	ratio	tolerance / notes
.3865	5.219	9.504	4.285	1.8211	target design point
.3865	5.219	8.6464	4.285	1.6569	ratio correct
.3415	4.361	8.647	4.285	1.9825	Va vswing
.455	6.523	10.809	4.285	1.6569	+/- 20%

For the above point with vbias = 125mV

Va = .3415 - 0.0125 = 0.329 volts

Vn = .3865 + 0.0125 = 0.399 volts



Domain for Driver Assertion and Negation Levels

having to require expanders for lumped loads, symmetrical or asymmetrical

If it is insisted that lumped load cases must work at 80mhz to prove that symmetrical works, then those same lumped load cases must work at 40mhz at all corners of the driver's specification, just like symmetrical should.

8.0 Doesn't work at 40mhz on paper.

9.0 "Enhancements" to improve asymmetrical, improve symmetrical more.

9.1 If things like stretching the 1st pulse's clock cycle, or an adjustable strength output drive are done to improve 1st pulse response for asymmetrical, more margin is gained by doing the same things to a symmetrical driver. From the best estimates, changing to symmetrical drive with no bias, will get you more margin improvement than both pulse stretching & adjustable strength drive combined.

9.2 It should be easier to make a symmetrical driver strength adjustable. You can modify the transistors you have now to make it the asymmetrical driver into an adjustable one.

10.0 It is very difficult to write a correct asymmetrical specification:

10.1 Example 1, page 47 section A.2.2, Offset (common-mode output) V_{cm}. This test has a built in bias against asymmetrical output unless the output resistance is very high. See attached proof.

10.2 Example 2, later date.

Problem with common mode offset test. This test has a built-in
bias against asymetical drivers.

Following is the proof:

Spice netlist of circuit for resistor connections.

```
  Rtop  Vmax  top   rtop   $ pull up resistance
  R27t   top  Vcm   r27t   $ test circuit 27 ohm resistor
  R27b   Vcm  bot   r27b
  Rbot   bot  gnd   rbot   $ pull down resistance
  R75    Vcm  Vb    r75    $ voltage bias 75 ohm reisistor
```

Math stuff

r27t = r27b = r27 =27 ohmhs
Vmax = 2.5 volts, for this proof
rtop = rbot, this means there should not be any offset possible, since the
pull up & down resistances are exactly the same.
Vb = 0.7 volts, this is the applied bias voltage, it ranges from 0.7 to 1.8
the current equation is good for Vb < 1.25 volts (above 1.25
is just a mirror of what is below).
Vmin = gnd = 0 volts
rt = rtop + r27
rb = rbot + r27
rt = rb

Outline of proof:

For 0.7 <= Vb < 1.25 volts you can write a current equation for the
resistor network and 3 current equations based on V & R, this gives
you an equation you can solve for Vcm.

After you have an equation for Vcm, you can substitute different values
of output resistances to model NEGATION & ASSERTION, for asymetrical
drivers.
Then you calculate the difference's in Vcm's. Since there is a difference,
this means that the test circuit is also testing a balance between
NEGATION & ASSERTION currents. This is the problem.

The proof:

From Kirkoff's laws, we can write,

Itop = Ibot + I75 for 0.7 <= Vb < 1.25

(For 1.25 > Vb >= 1.8, Ibot = Itop + I75 & Vb=1.25 Itop=Ibot)

From Ohm's law,

I75 = (Vcm - Vb) / r75

Itop = (Vmax - Vcm) / (rtop + r27)

Ibot = (Vcm - Vmin) / (rbot + r27)

Back substituting you get,

(Vmax - Vcm) / (rtop + r27) = ((Vcm - Vmin) / (rbot + r27)) + ((Vcm - Vb) / r75))

Since rt = rb & rt = rtop + r27, rb = rbot + r27

(Vmax - Vcm) / rb = ((Vcm - Vmin) / rb) + ((Vcm - Vb) / r75))

((Vmax - Vcm) / rb) - ((Vcm - Vmin) / rb) = (Vcm - Vb) / r75

((Vmax - Vcm) - (Vcm - Vmin)) / rb = (Vcm - Vb) / r75

(Vmax + Vmin - 2Vcm) / rb = (Vcm - Vb) / r75

r75 * (Vmax + Vmin - 2Vcm) = rb * (Vcm - Vb)

(r75 * Vmax) + (r75 * Vmin) + (r75 * -2Vcm) = (rb * Vcm) - (rb * Vb)

(r75 * Vmax) + (r75 * Vmin) + (rb * Vb) = (rb * Vcm) - (r75 * -2Vcm)

(r75 * Vmax) + (r75 * Vmin) + (rb * Vb) = Vcm * (rb + 2 * r75)

Vcm = ((r75 * Vmax) + (r75 * Vmin) + (rb * Vb)) / (rb + 2 * r75)

Since Vmin = 0 volts

Vcm = ((r75 * Vmax) + (rb * Vb)) / (rb + 2 * r75)

Since r75 = 75, Vmax = 2.5, & Vb = 0.7

Vcm = 187.5 + 0.7rb / (rb + 150)

Since rb = rtop + r27, rb = rtop + 27

Vcm = 206.4 + 0.7rtop / (rtop + 177)

Two values for rtop, 94 ohms for Ascertion & 156 ohms for Negation, these will have a 56.7 millivolt common mode offset from this equation.

But, since rtop & rbot are exactly equal, there should not be any offset if this is a good way to measure it.

Therefore, some how the measurement technique needs to be fix so that an ideal case doesn't have any "built-in offset"

Wally Bridgewater

To Increase Slew Rate:

Make the ratio Ibias / gm as large as possible

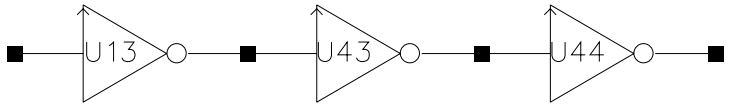
$$\frac{Ibias}{gm} \leq \infty$$

Where Ibias is the current flowing through your differential pair. gm is the transconductance of your differential pair.

If you want to minimize power, make Ibias as small as possible. Then you need to make your input transistors (differential pair) as small as possible, down to minimum size. It also helps your common mode range to have as little drain-to-source voltage drop across your current source transistor.

References you can look at:
“Bipolar & Mos Analog IC Design”, by Alan B. Grebene, pg 338
“Analog Design?”, by Paul Gray & Meyer
There are some tutorial classes that James McCreary used to teach, they were much more detailed.

Figure 4



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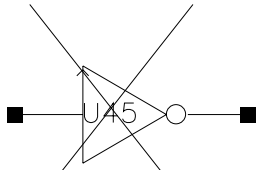

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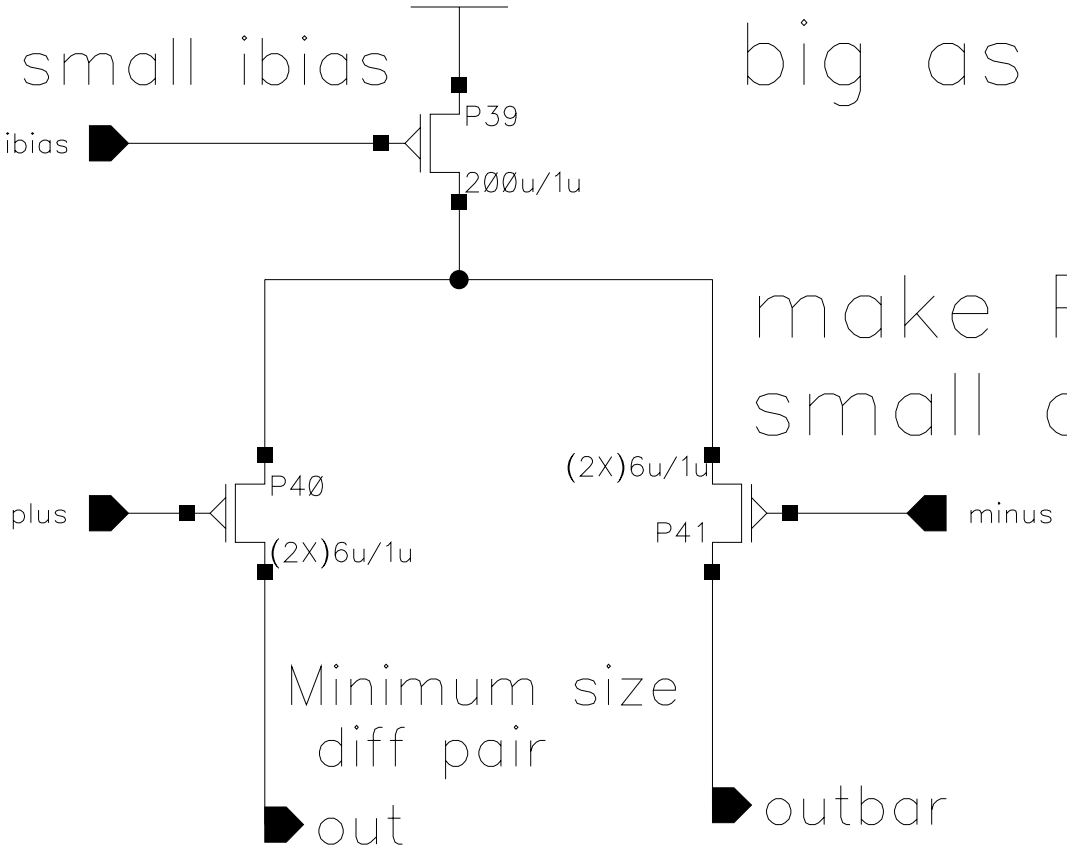
to make I/gm as big as possible



$Z \leq 15\ \Omega$ from 2 MHz to 500 MHz.

4.2.2 Media signal interface

The cable media signal interface is called a port. It consists of two twisted pair interfaces (TPA/TPA* and TPB/TPB*) and a power distribution pair (VP/VG). A node may have several such ports. Each port has associated circuitry that provides separate signals for packet data reception/transmission and for arbitration as shown in figure 4-12.

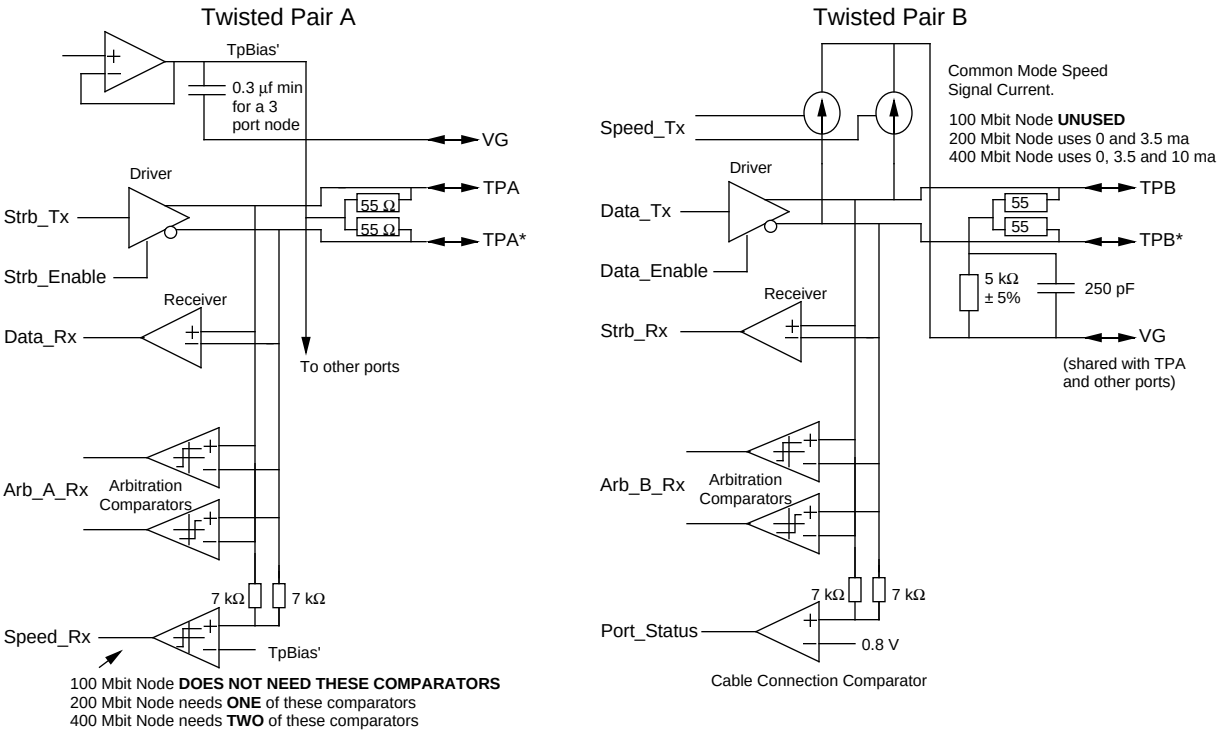


Figure 4-12 — Cable media signal interface configuration

The TPA/TPA* pair transmit the Strb_Tx signal and receive the Data_Rx, Arb_A_Rx and Speed_Rx signals, while the TPB/TPB* pair transmits the Data_Tx and Speed_Tx signals and receives the Strb_Rx, Arb_B_Rx and Port_Status signals. The Strb_Tx, Data_Tx, Strb_Enable and Data_Enable signals are used together to generate the arbitration signals. The Arb_A_Rx and Arb_B_Rx signals are each generated by two comparators since they are have three states: 1, 0, and Z.

In addition, the TPA/TPA* transmit TpBias while TPB/TPB* receive the TpBias signal which is used by the Port_Status comparator to determine that a cable connection exists.

4.2.2.1 Signal amplitude

For the test loads shown in figure 4-13, the drivers for TPA and TPB shall provide the following differential output signal amplitude (an additional 10% is allowed for signal overshoot):

Table 4-12 — Differential output signal amplitude

Max	Min	Units
265	172	mV

Capacitance calculations

$$141A^{\circ} = 2.45fF \times 12u = 0.05676pF$$
$$73A^{\circ} = 4.73fF \times 7u = 0.03311pF$$

If for some reason, you have to run an additional 500u of metal 1 to connect to the inputs, then add ~0.050pF more capacitance to account for metal 1 line length, this is way over kill, but it not much capacitance either.

Total worst case estimated capacitance = ~0.1pf, as compared to 5pf or about 2%

But remember

ACK & REQ (also parity) don't need dual receivers since release glitches changes take care of them. Data lines are the only signal that really need dual receivers. So the most critical lines aren't affected anyway. But, you might want to think about the effect of having less capacitance on ACK & REQ might have on system skew verses the affect of 0.5% to 2% more capacitance.

4.2.2.6 Noise

The maximum output common mode noise, V_{cmout}, shall be 200 mV p-p during arbitration and 30 mV during data transmission, as measured in a 400 MHz bandwidth using the following test loads:

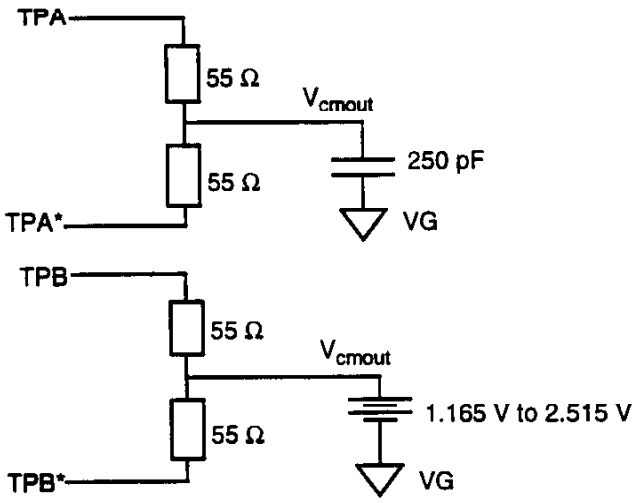


Figure 4-15 — Common mode output noise test loads

The maximum input common mode noise shall be 225 mV p-p during arbitration and 55 mV p-p during packet reception. This shall be measured in a bandwidth of 20 MHz to 400 MHz.

The maximum input differential noise shall be 8mV p-p.