

To: T10 Membership

Subject: 1st Pulse Measurements

Date: 4/17/97

Board #5, Asymmetrical Va & Vn, 431mV & 540mV (Fig. 27 edge point)

Board #6, Asymmetrical Va & Vn, 630mV & 700mV (Not in shaded area)

Board #5, Symmetrical Va & Vn, 413mV & 406mV

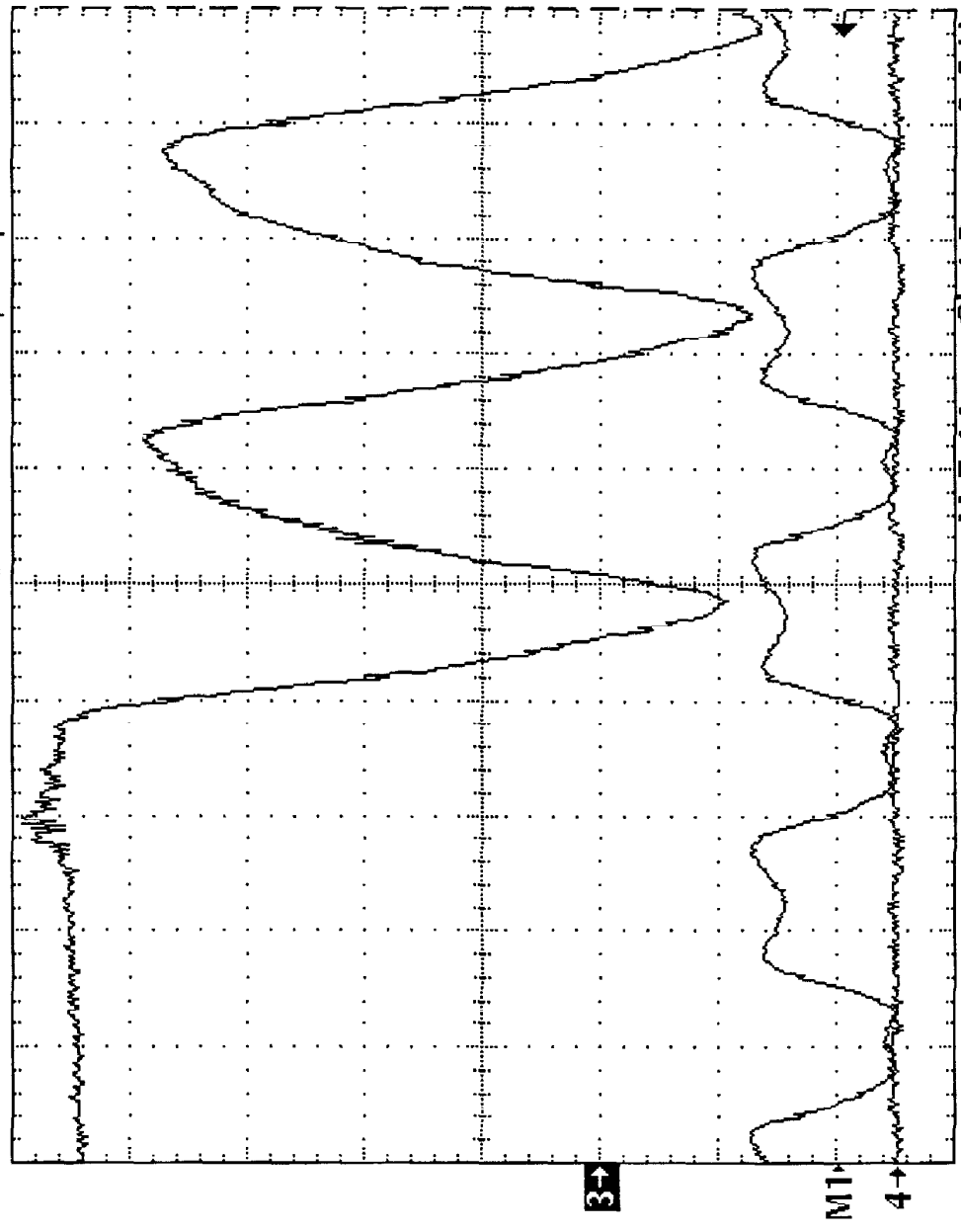
Board #6, Symmetrical Va & Vn, 602mV & 579mV

Table 1

Board # & Type	Amplitude	Over/Under Drive Ratio
Board 5 Asym	100mV	~1:4
Board 5 Sym	160mV	~1:1.5 (160/260)
Board 6 Asym	130mV	~1:4 (130/500)
Board 6 Sym	180mV	~1:2

1st pulse As you Bic #5,  
80 mhz 35 meter cable

Tek Run: 10.0GS/s ET Hi Res



Δ: 209.2ns  
@: 810.5ns

M1 Freq  
79.53583MHz  
low signal  
amplitude

M1 +Duty  
57.227 %  
low signal  
amplitude

C3 +Duty  
59.073 %

C4 +Duty  
92.687 %  
low signal  
amplitude

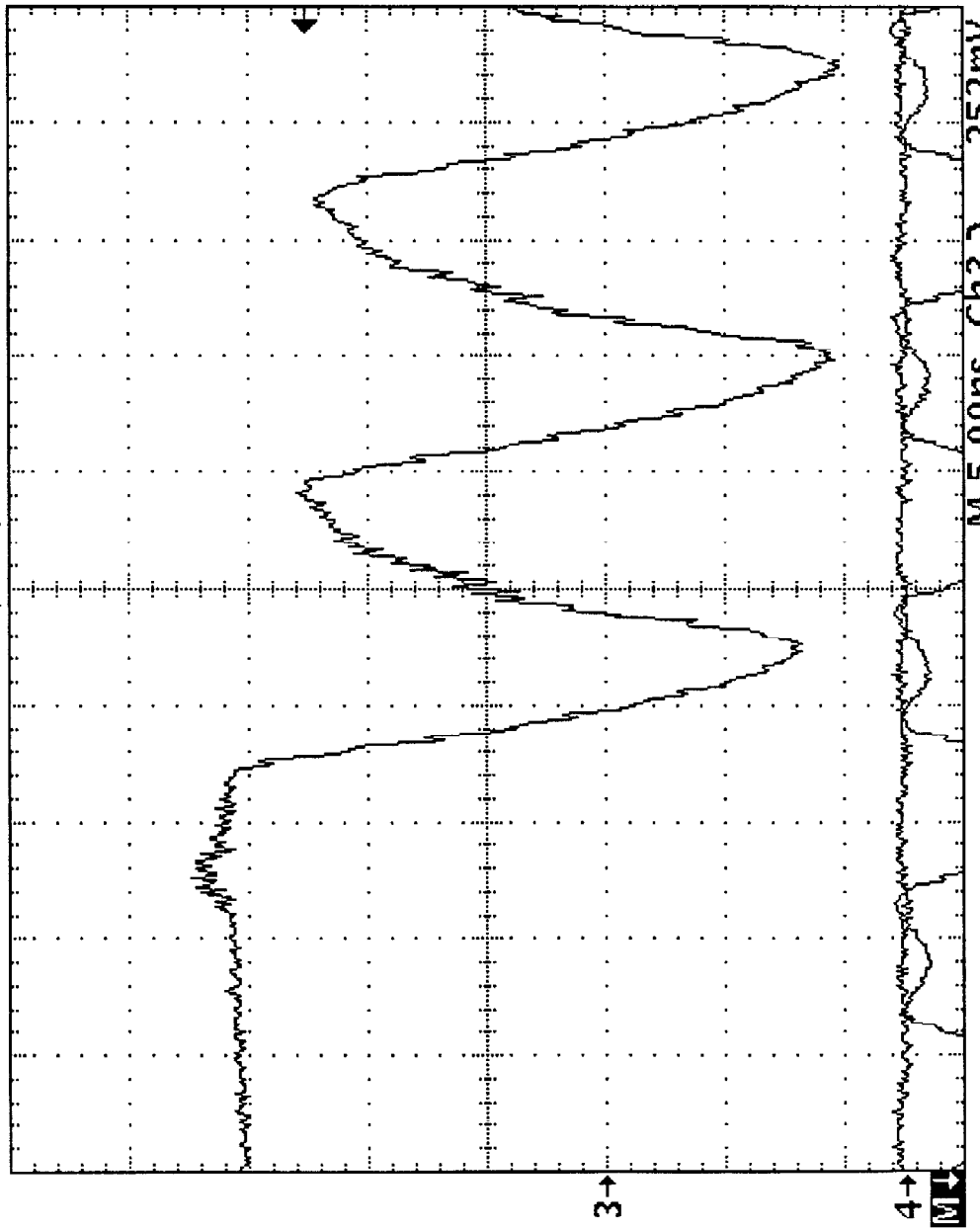
17 Apr 1997  
17:50:07

Ch3 100mVΩ Ch4 5.00 V  
Math1 1.00 V 5.00ns

M 5.00ns Ch4 2.2V

157 Pulse Sym No Bias Board #5  
80 MHz 75 ohm Cable

Tek Run: 10.0GS/s ET Hi Res



$\Delta$ : 209.2ns  
@: 810.5ns

M1 Freq  
79.69368MHz  
Low signal  
amplitude

M1 +Duty  
55.313 %  
Low signal  
amplitude

C3 +Duty  
56.333 %

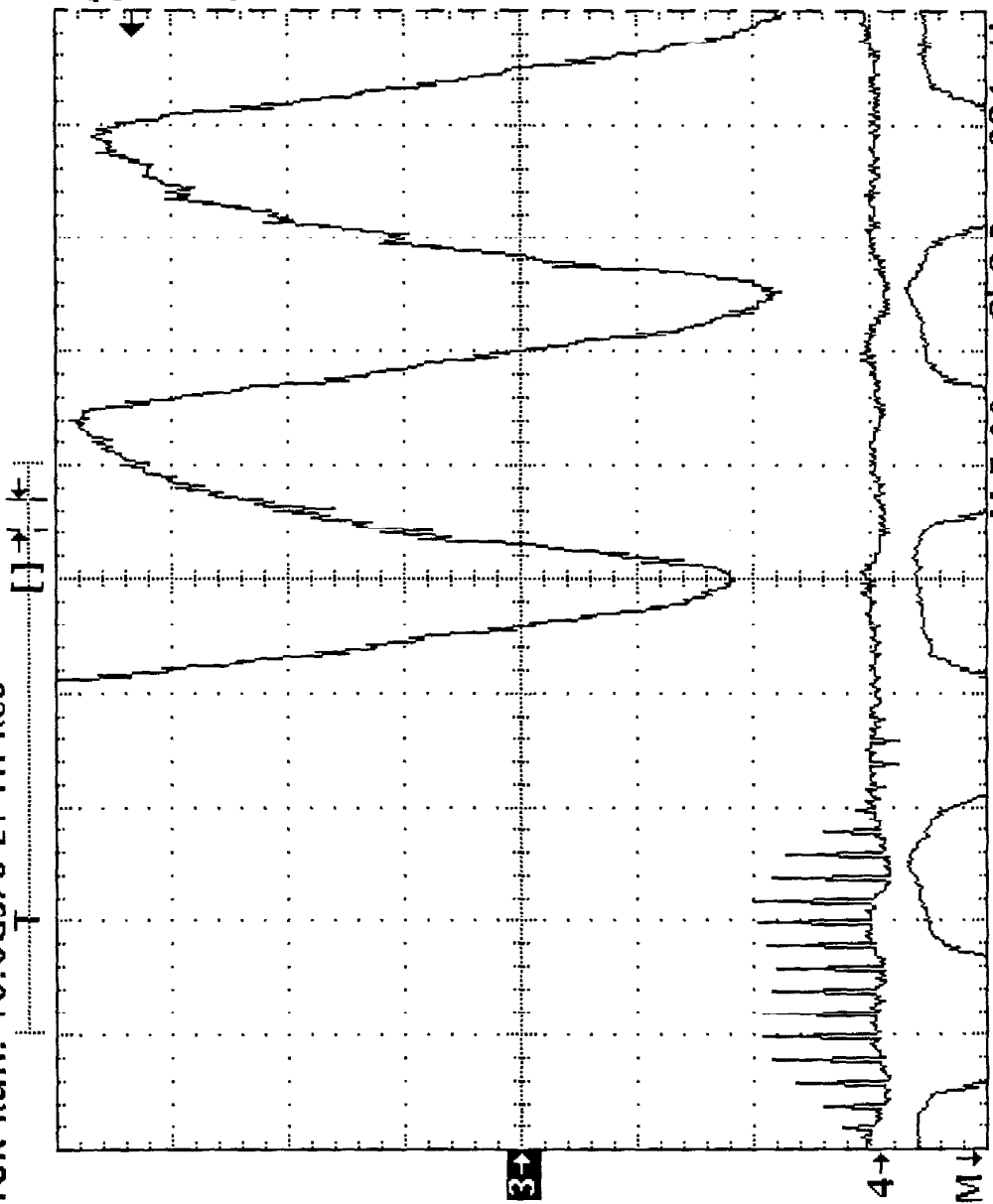
C4 +Duty  
85.513 %  
Low  
resolution

17 Apr 1997  
18:11:17

Ch3 100mV $\Omega$  Ch4 5.00 V  
Math1 1.00 V 5.00ns

1st pulse Sym NO bias  
Board # 625 meter cable

Tek Run: 10.0GS/s ET HI Res



Δ: 82.0ns  
@: 1.102μs

M1 Freq  
180.15970MHz  
Low signal  
amplitude

M1 +Duty  
57.120 %  
Low signal  
amplitude

C3 +Duty  
59.467 %

C4 +Duty  
4.087 %  
Low  
resolution

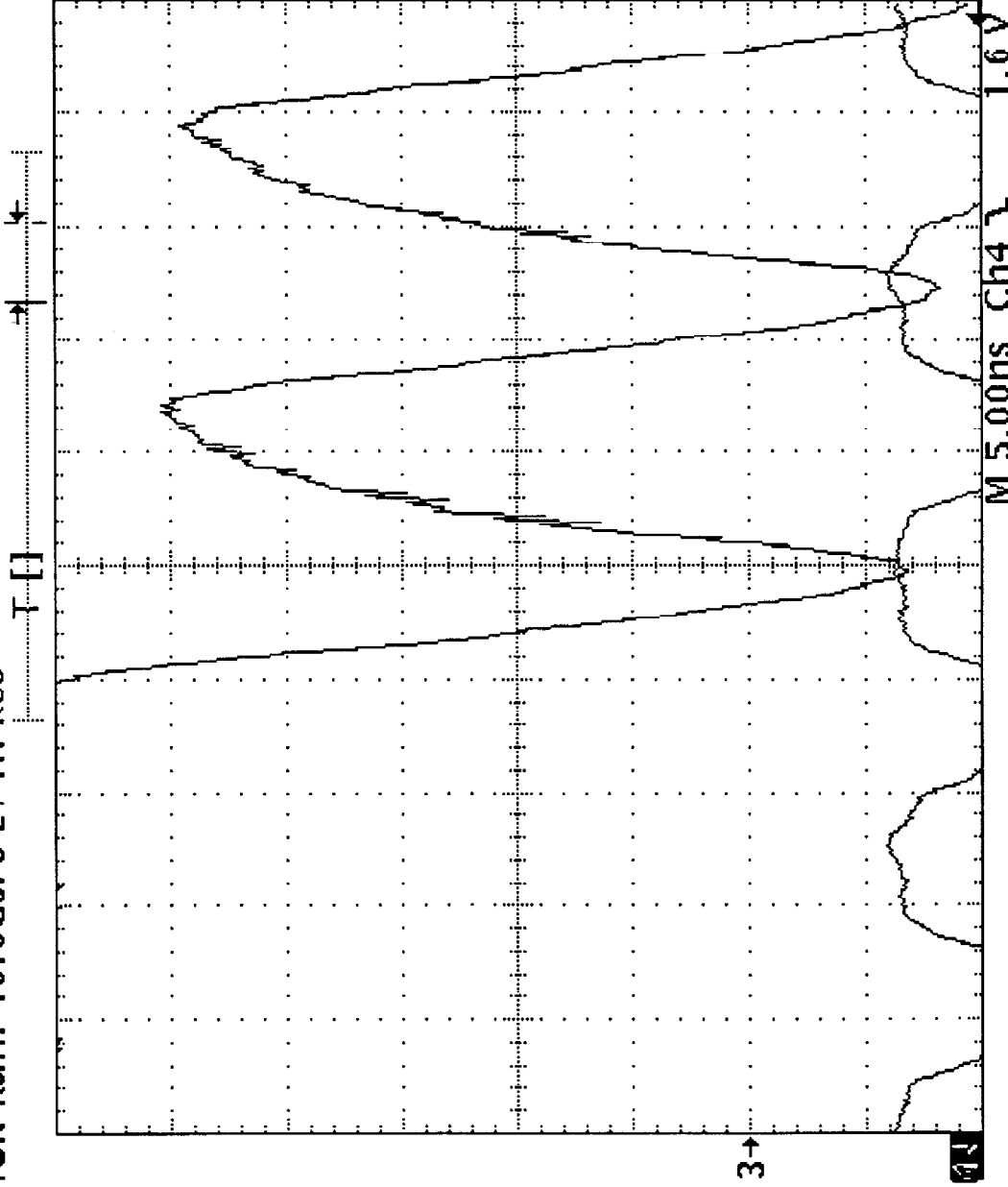
17 Apr 1997  
18:34:34

Ch3 100mVΩ Ch4 5.00 V  
Math1 1.00 V 5.00ns

M 5.00ns Ch3 334mV

1st Pulse Asyn Bics Round 16,  
80 minz 25 micro cable

Tek Run: 10.0GS/s ET Hi Res



$\Delta$ : 209.2ns  
@: 810.5ns

M1 Freq  
78.61683MHz  
Low signal  
amplitude

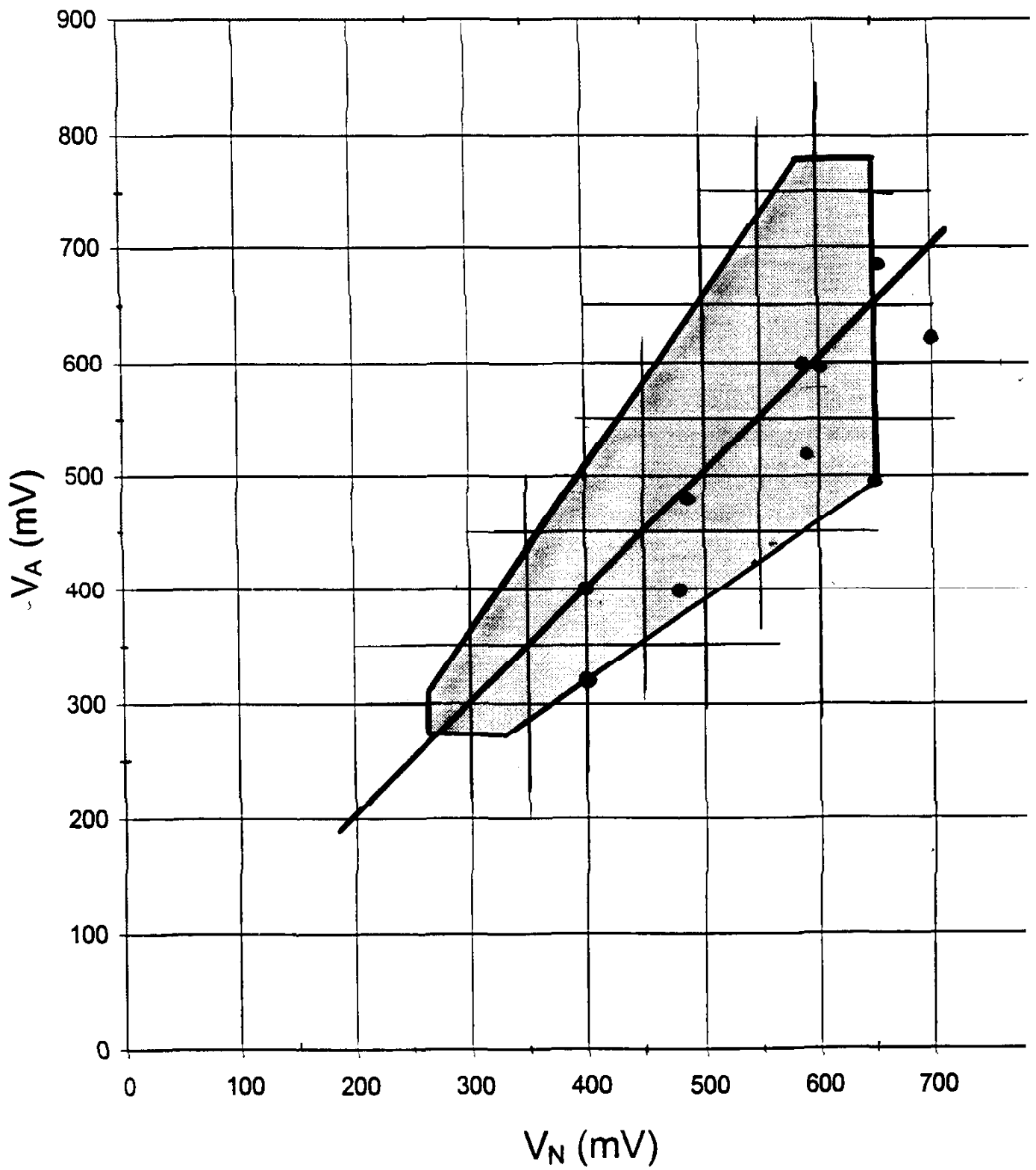
M1 +Duty  
61.233 %  
Low signal  
amplitude

C3 +Duty  
59.380 %

C4 +Duty  
4.980 %  
LOW  
resolution

17 Apr 1997  
18:28:54

Ch3 100mVΩ Ch4 5.00 V  
Math1 1.00 V 5.00ns



Domain for Driver Assertion and Negation Levels