SPI
Working Group Meeting
April 18, 1997

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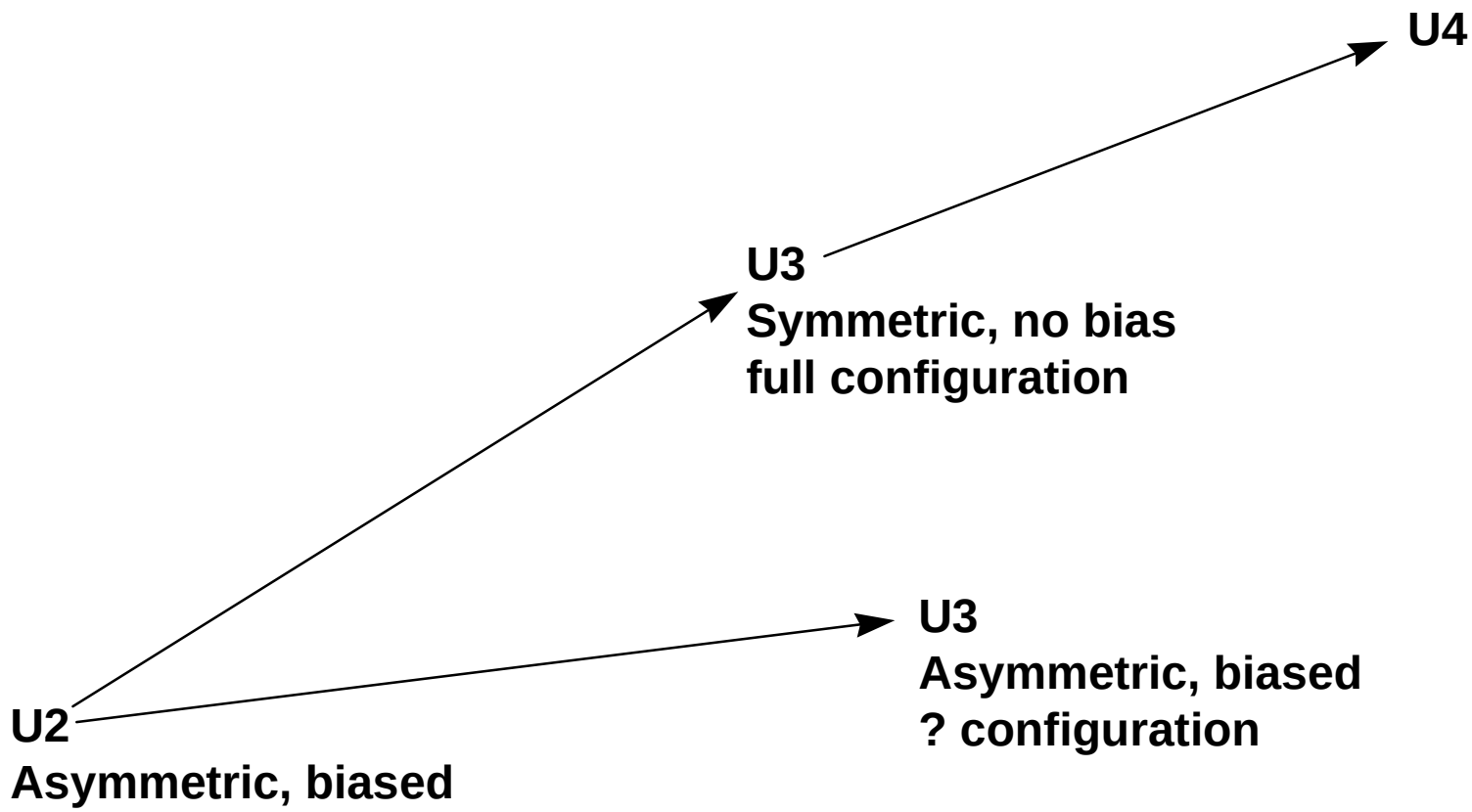
Roadmap


U4
U3
Symmetric, no bias
full configuration
U3
Asymmetric, biased
? configuration
U2
Asymmetric, biased

Agenda

- **Cable Loss @ High Frequency**
- **Simulation Study Symmetric Versus Asymmetric**
- **Measured Data**
- **Ultra 3 Alternatives**

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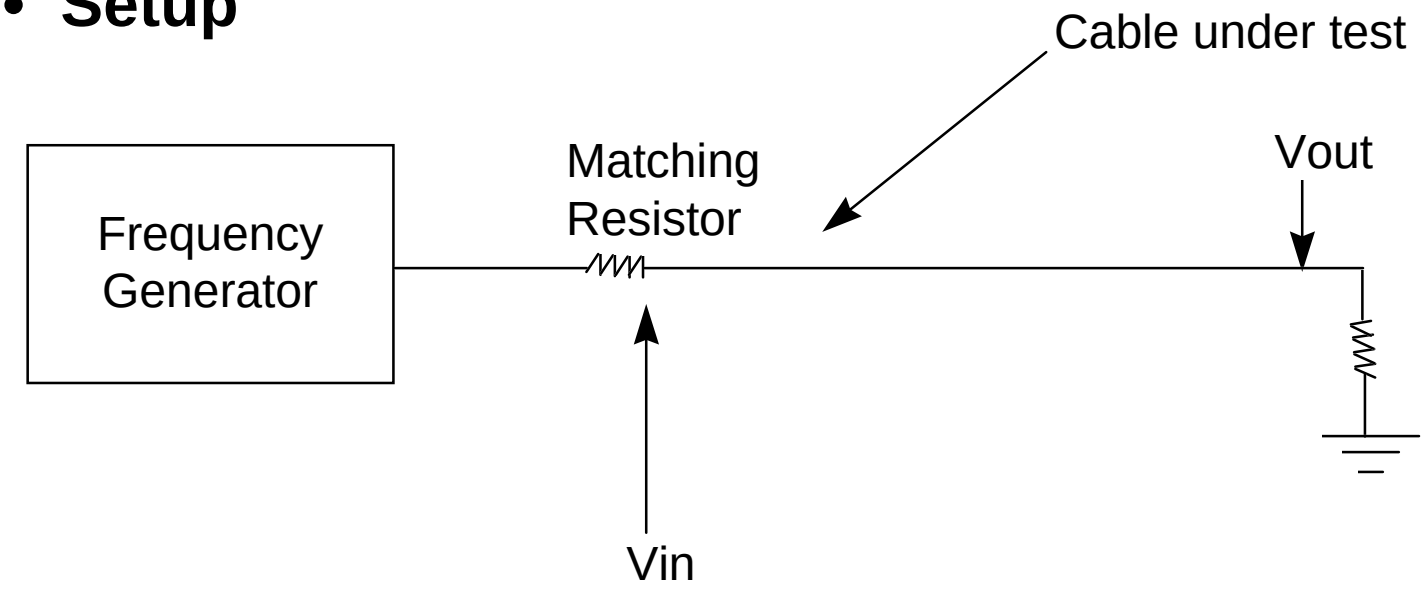
Cable Loss Test

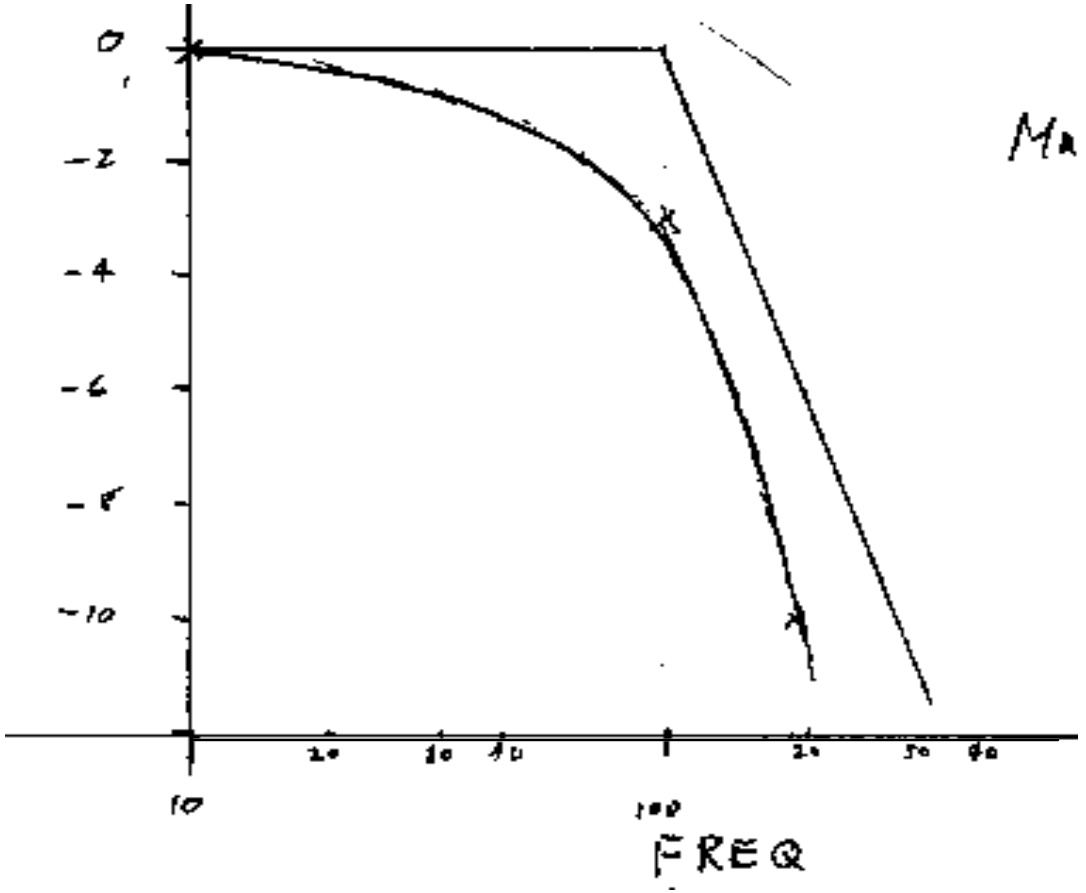
- **Motivation - Measure Standard Cable Loss As A Function Of Frequency For Later Simulations**

- **Setup**



Measured Cable Loss

Point to Point 25 Meters Standard PVC Cable



Cable Loss Conclusions

- **Rolloff Is Greater Than 6 db/oct Due To Skin Effect Dielectric Dissipation**
- **At 40 MHz ==> ~ 1 db**
- **At 100 MHz ==> 3 db**
- **At 180 MHz ==> 10 db**

Simulations

- **Goal: Compare Sym And Asym Robustness With Different Cable Attentuations And Drive Powers in**
- **Point to Point mode.**
- **Asymmetric At 500 mv With 5/8 ma Drive (Nominal)**
- **Symmetric At 350 mv With 4 ma Drive**
- **Symmetric At Min Drive Level To Produce +/- 40 mv Output**
- **Show Ratio Of Power Consumption Between Sym And Asym**

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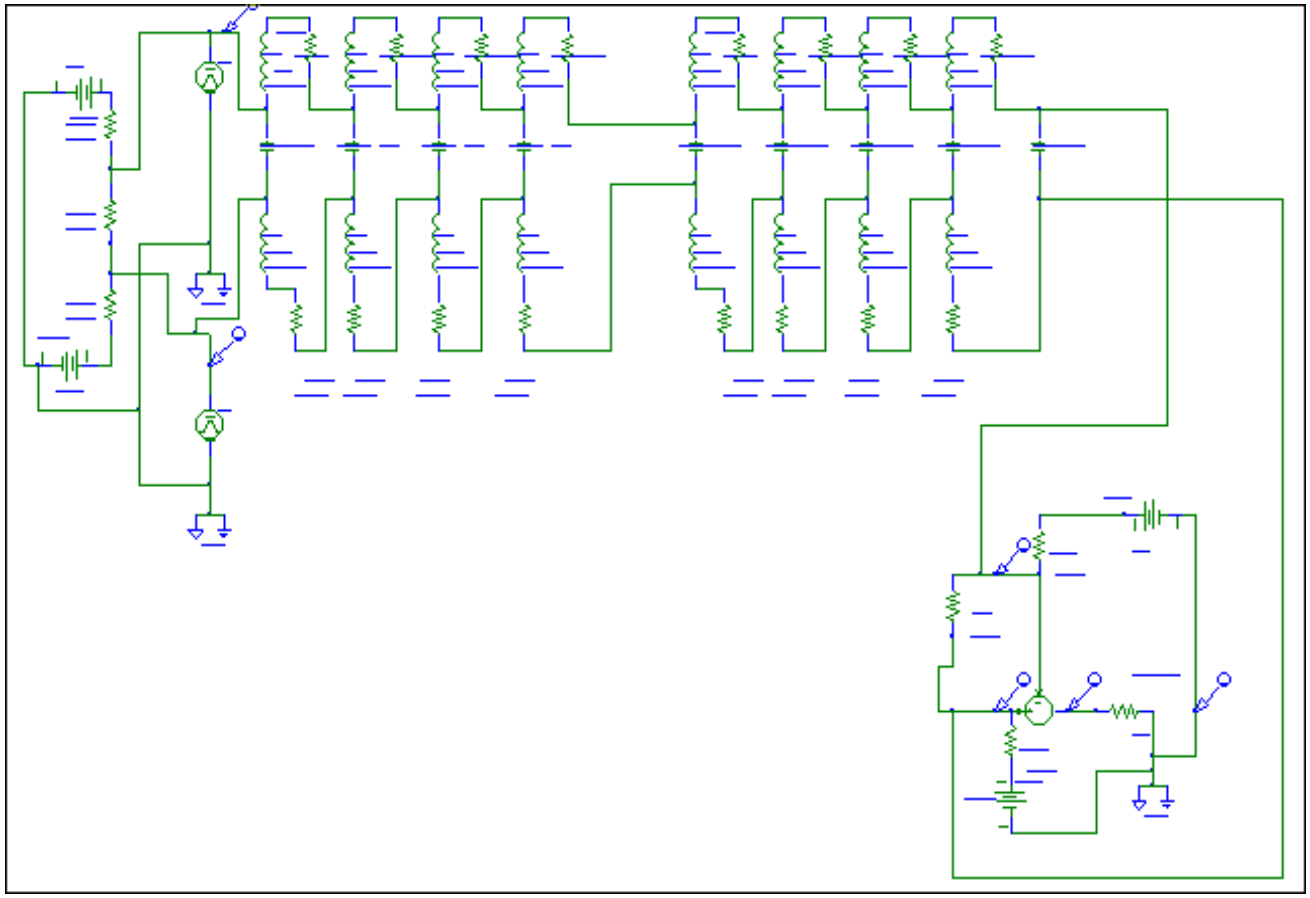
Test Configuration

Asymmetric

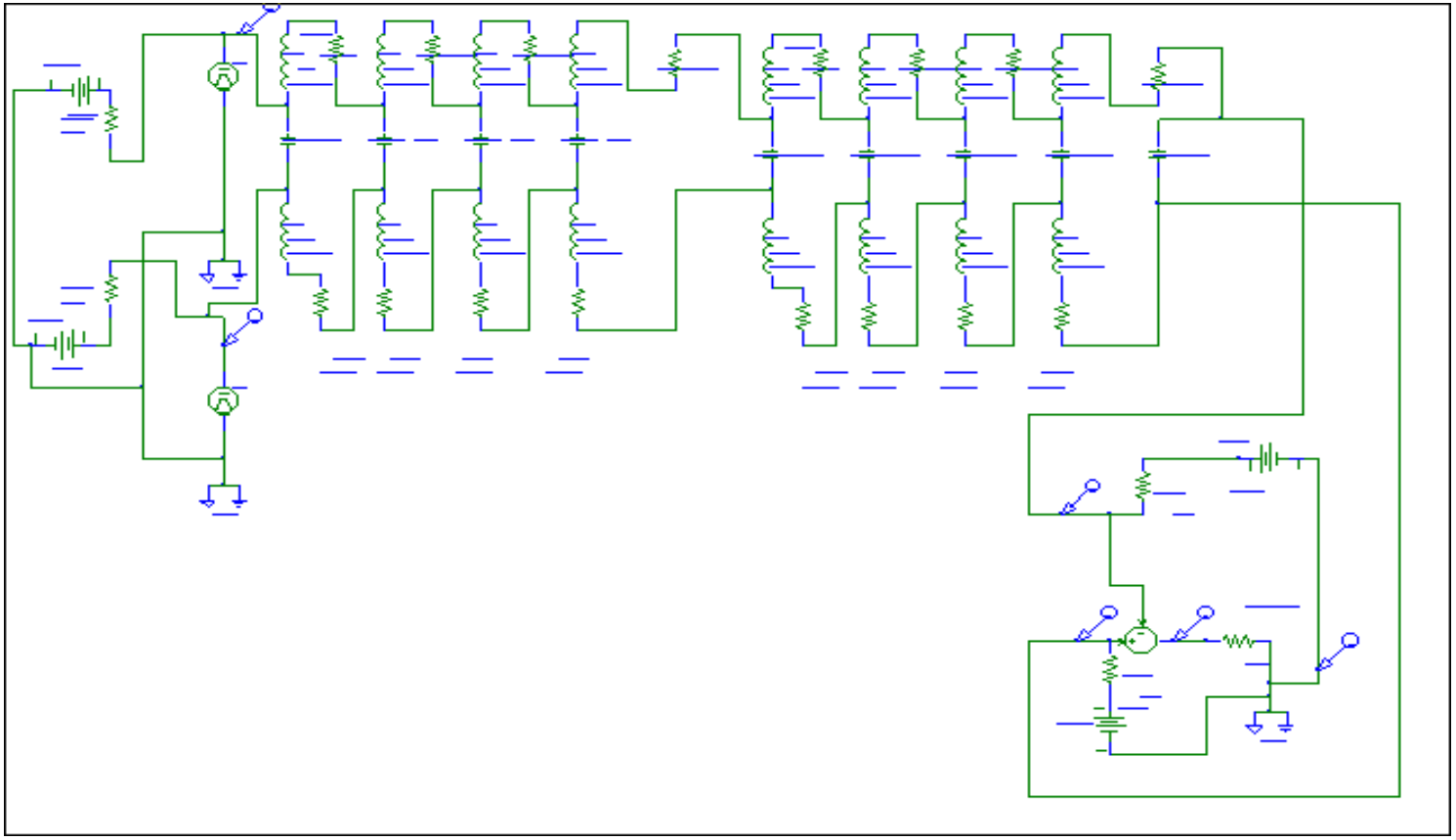


Lumped Parameter Simulation
L = .09 Microh
C = 18 pf
R = .041
all per ft.

Bias = 0.1 Volt

Test Configuration

Symmetric



Lumped Parameter Simulation
L = .09 Microh
C = 18 pf
R = .041
all per ft.

Bias = 0 Volt

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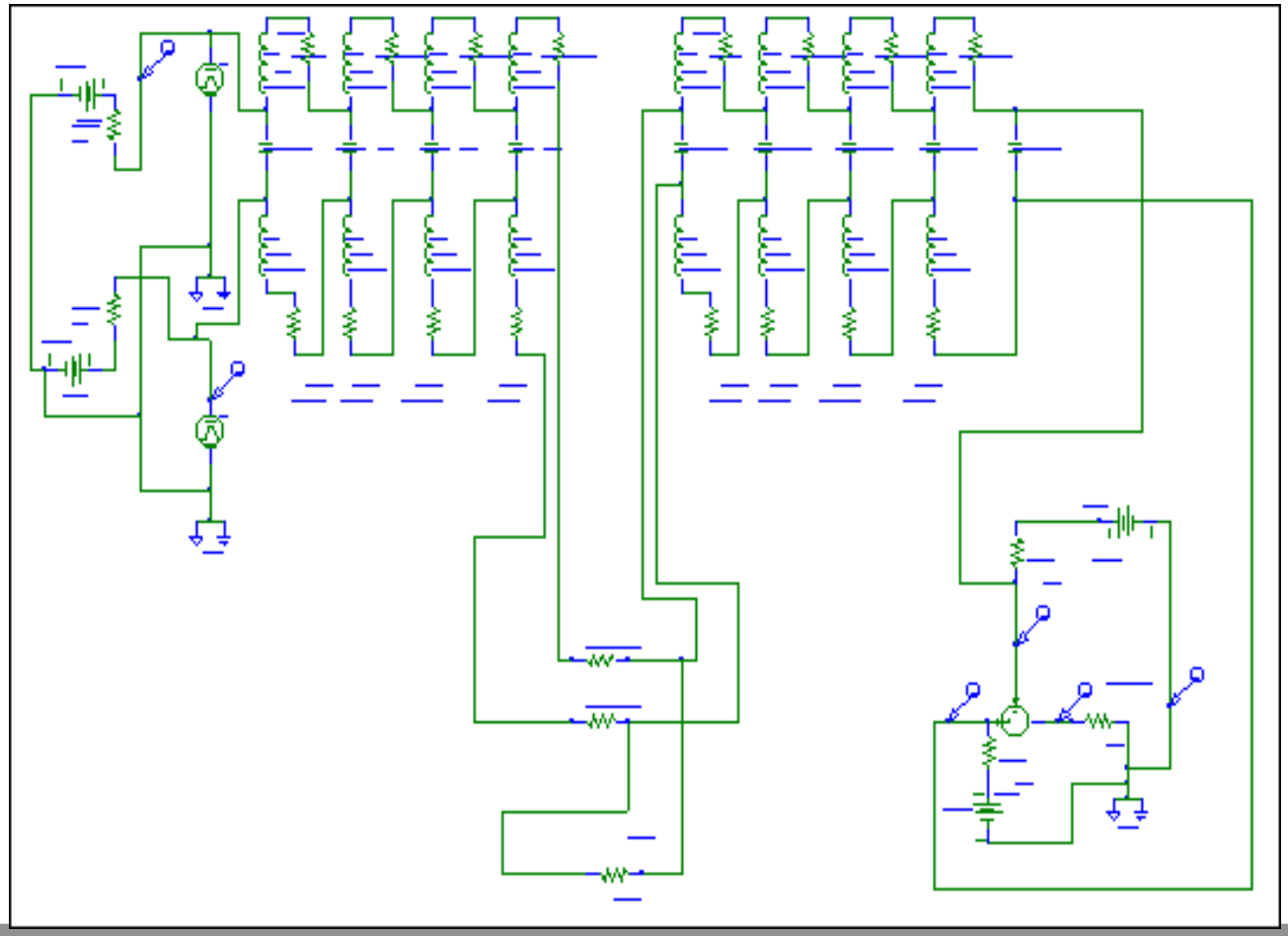
Test Configuration With Loss Symmetric



Lumped Parameter Simulation
L = .09 Microh
C = 18 pf
R = .041
all per ft.

Attenuation = 10 db

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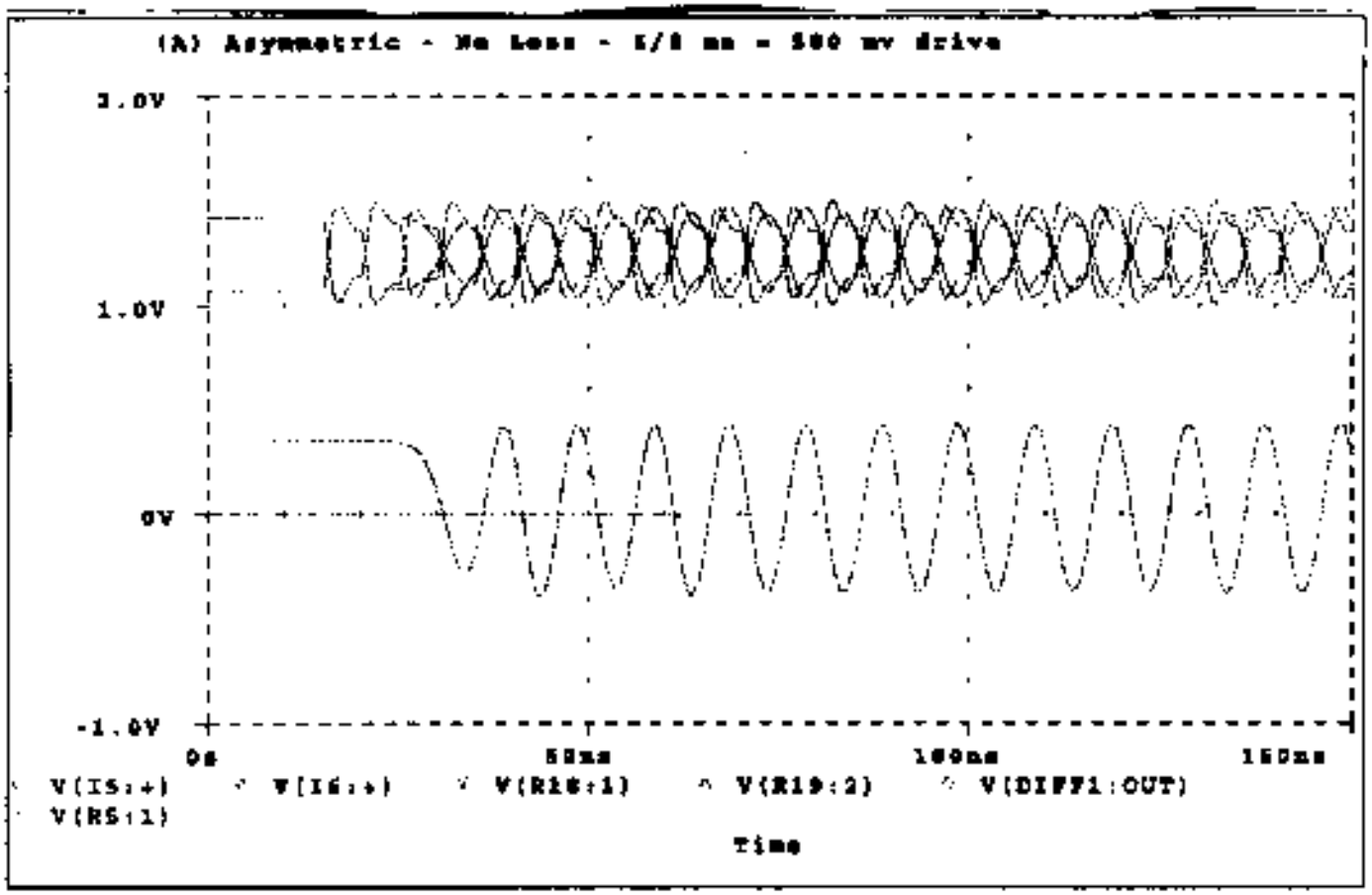
Asymmetric, No Cable Loss
5/8 ma Drive, ~500 mv drive,100 MHz



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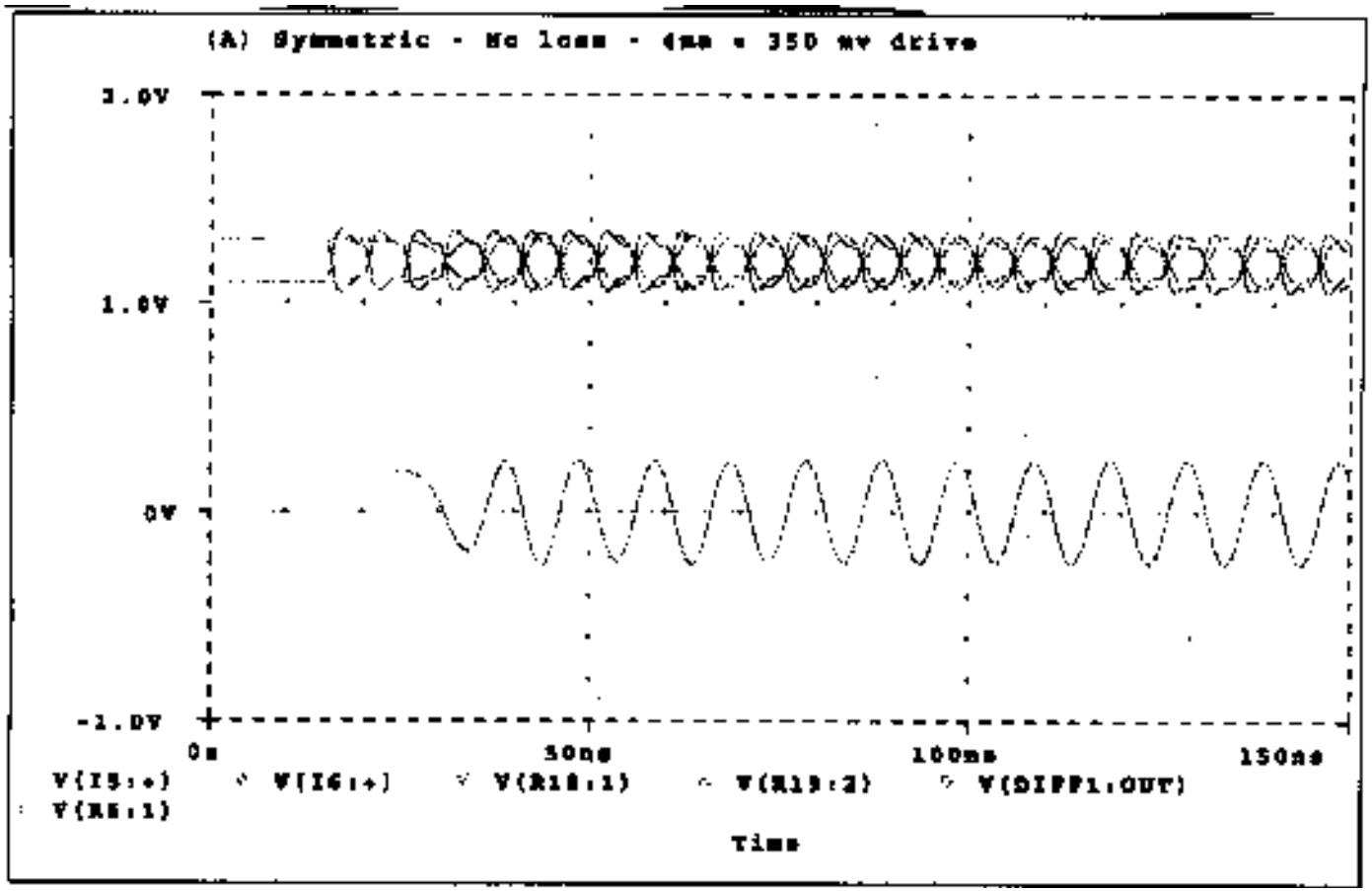
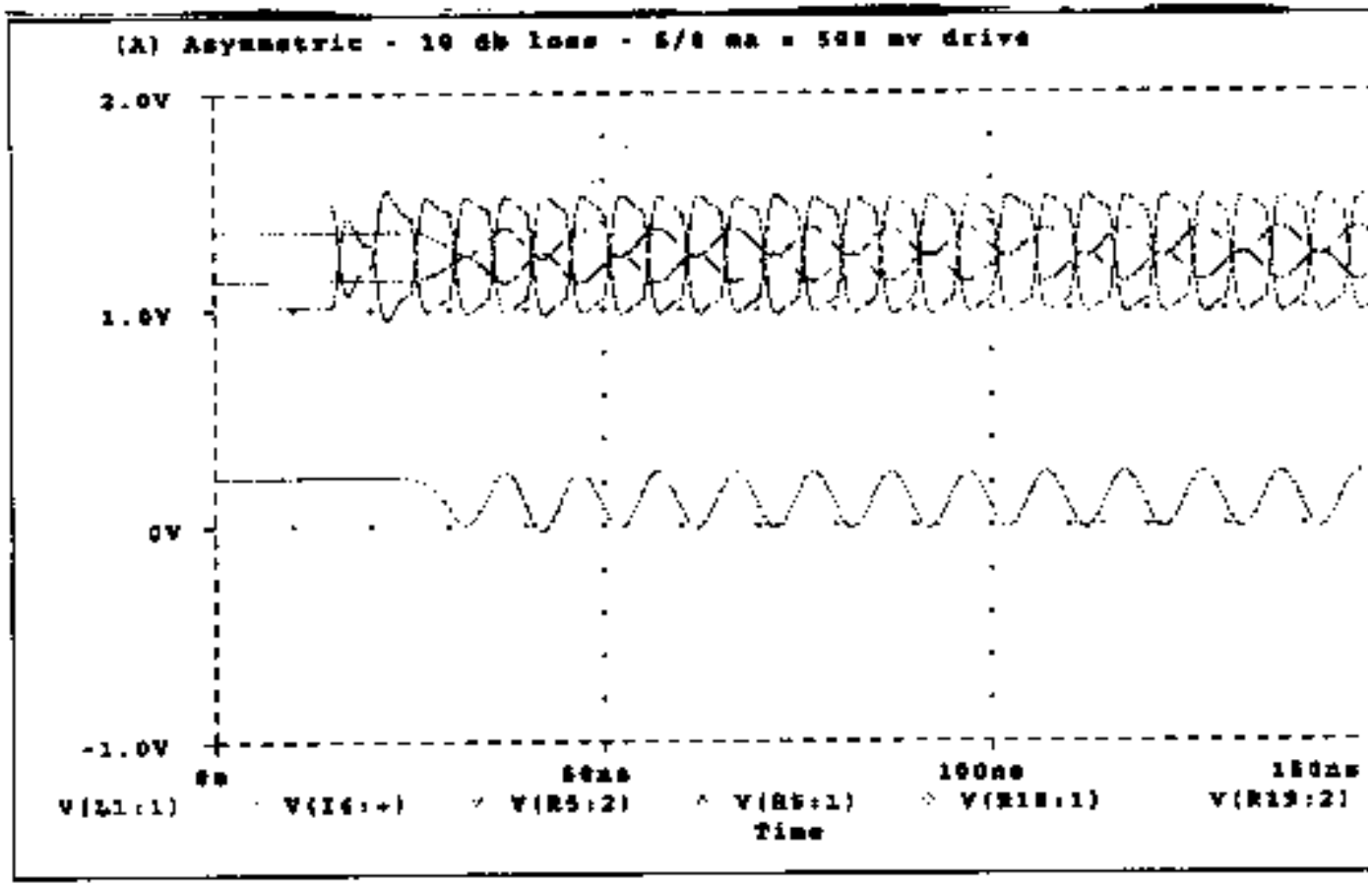
Symmetric, No Cable Loss
4 ma Drive, ~350 mv, 100 MHz



Asymmetric 10 db Cable Loss
5/8 ma Drive, ~500 mv, 100 MHz



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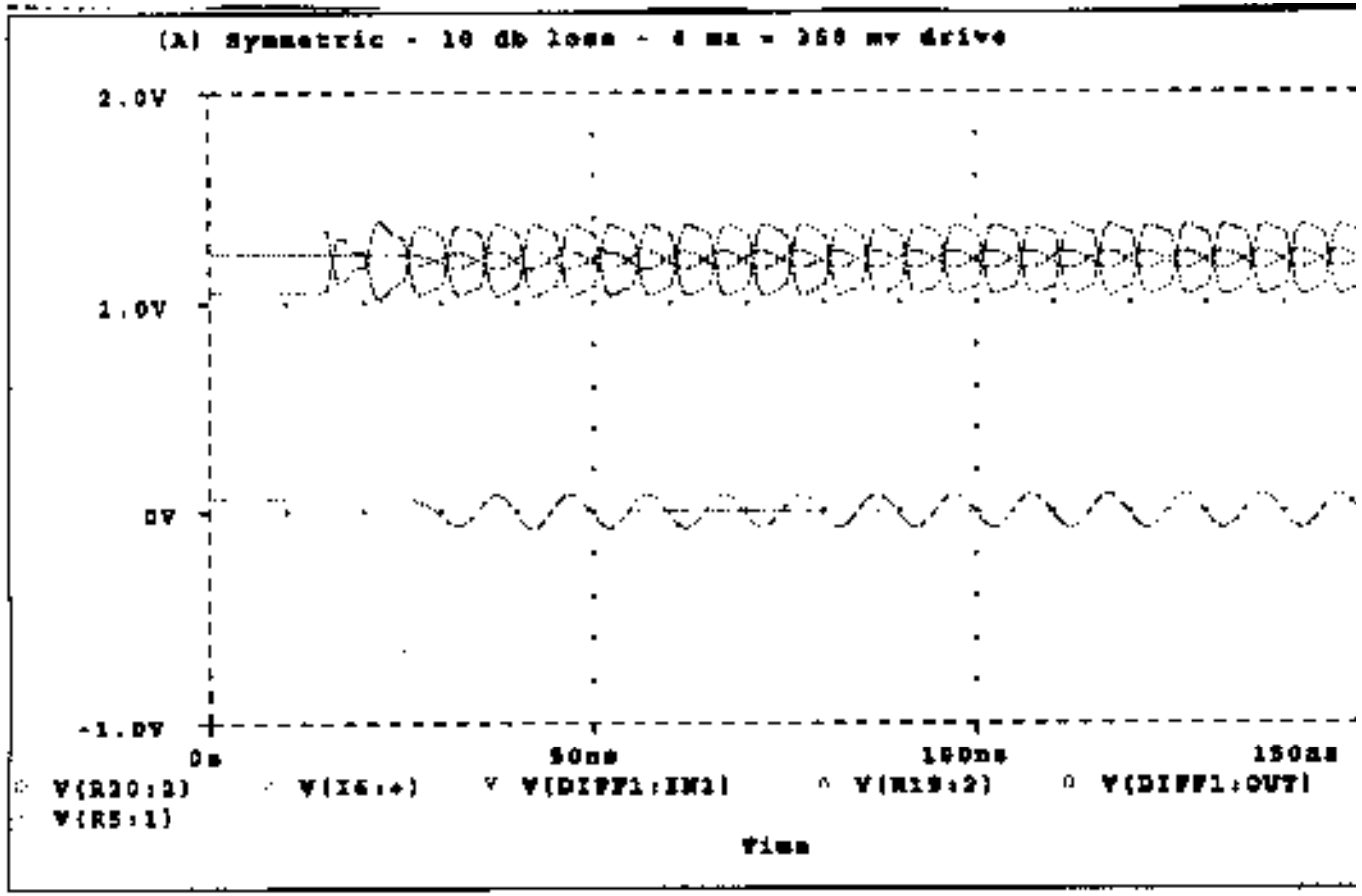
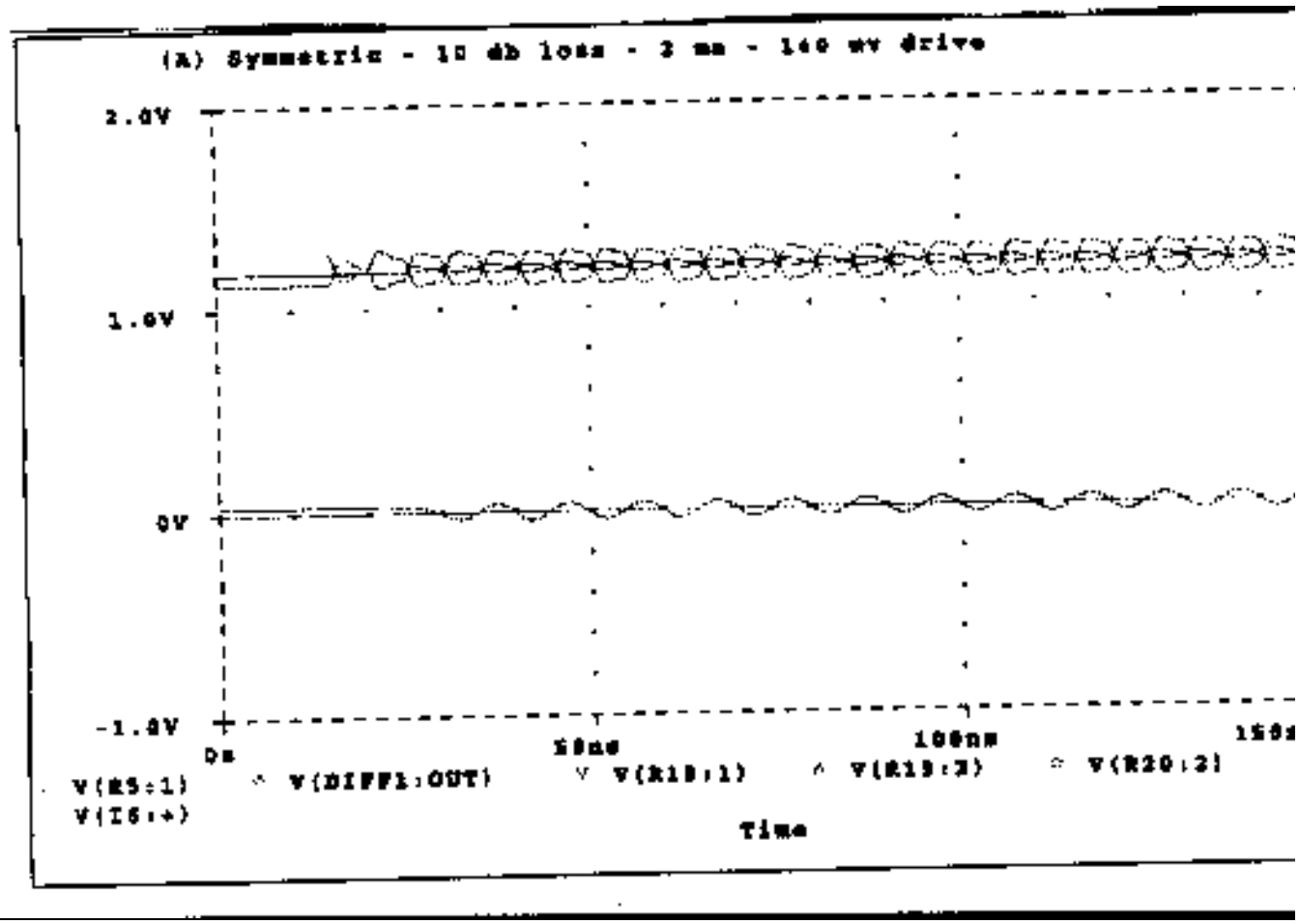
Symmetric 10 db Cable Loss
4 ma Drive, ~350 mv, 100 MHz



Symmetric, 10 db Cable Loss 2ma Drive, ~140 mv, 100 MHz

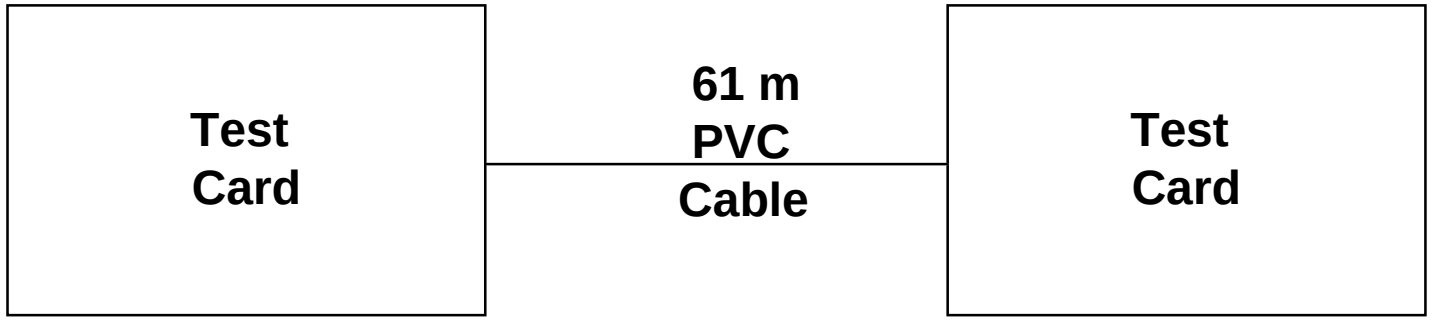


Conclusions From Simulations

- **With 10 db Cable Loss**
  - Asymmetric fails at 500 mv nominal drive level
    - -- Worse at 250 mv minimum drive level
  - Symmetric works well below 250 mv drive level
    - -- Simulation shows proper operation down to 140 mv

Measured Results

Goal: Quantify Operational Margin



- Done For 3 Bias Cases
- Done for Symmetric And Asymmetric
- Done For High Drive, Nominal Drive

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Assertion/Negation Levels With Different Drive Values

	REGULAR AND HIGH DRIVE WITH AND WITHOUT 100 MV BIAS				
SYMMETRIC			ASYMMETRIC		POWER DIFFER %
LOW DRIVE			LOW DRIVE		
BIAS = 0 MV			BIAS = 0 MV		
Current (ma)	126.953		Current (ma)	148.242	36.351
Assertion	Negation		Assertion	Negation	
1.473	1.468		1.538	1.467	
1.062	1.059		1.062	0.982	
0.415	0.406		0.556	0.404	
BIAS = 100 MV			BIAS = 100 MV		
Current (ma)	126.660		Current (ma)	149.561	39.429
Assertion	Negation		Assertion	Negation	
1.434	1.510		1.501	1.509	
1.018	1.100		1.019	1.021	
0.333	0.490		0.480	0.489	
HIGH DRIVE			HIGH DRIVE		
BIAS = 0 MV			BIAS = 0 MV		
Current (ma)	175.000		Current (ma)	196.162	25.648
Assertion	Negation		Assertion	Negation	
1.538	1.527		1.601	1.526	
0.944	0.937		0.945	0.861	
0.601	0.583		0.740	0.582	
BIAS = 100 MV			BIAS = 100 MV		
Current (ma)	175.801		Current (ma)	197.852	26.659
Assertion	Negation		Assertion	Negation	
1.502	1.565		1.567	1.564	
0.905	0.975		0.905	0.895	
0.526	0.660		0.672	0.658	

Boards 1/2

100 mv Bias (lower limit)

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Assertion/Negation Levels With Different Drive Values

	REGULAR AND HIGH DRIVE WITH AND WITHOUT 125 MV BIAS				
SYMMETRIC			ASYMMETRIC		POWER DIFFER %
LOW DRIVE			LOW DRIVE		
BIAS = 0 MV			BIAS = 0 MV		
Current (ma)	124.993		Current (ma)	149.164	42.415
Assertion	Negation		Assertion	Negation	
1.447	1.444		1.509	1.443	
1.077	1.076		1.077	1.007	
0.371	0.366		0.502	0.365	
BIAS = 125 MV			BIAS = 125 MV		
Current (ma)	124.691		Current (ma)	149.164	43.107
Assertion	Negation		Assertion	Negation	
1.397	1.500		1.462	1.496	
1.022	1.129		1.022	1.057	
0.267	0.474		0.403	0.472	
HIGH DRIVE			HIGH DRIVE		
BIAS = 0 MV			BIAS = 0 MV		
Current (ma)	163.433		Current (ma)	183.337	25.840
Assertion	Negation		Assertion	Negation	
1.505	1.498		1.564	1.496	
1.016	1.012		1.016	0.947	
0.493	0.482		0.617	0.481	
BIAS = 125 MV			BIAS = 125 MV		
Current (ma)	158.913		Current (ma)	185.096	35.667
Assertion	Negation		Assertion	Negation	
1.457	1.547		1.519	1.546	
0.964	1.063		0.964	0.994	
0.394	0.583		0.525	0.582	

Boards 3/4

125 mv Bias (upper limit)

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Assertion/Negation Levels With Different Drive Values

	REGULAR AND HIGH DRIVE WITH AND WITHOUT 160 MV BIAS			
SYMMETRIC		ASYMMETRIC		POWER DIFFER %
LOW DRIVE		LOW DRIVE		
BIAS = 0 MV		BIAS = 0 MV		
Current (ma)	121.093	Current (ma)	142.474	38.430
Assertion	Negation	Assertion	Negation	
1.468	1.462	1.534	1.461	
1.057	1.055	1.058	0.980	
0.413	0.405	0.553	0.403	
BIAS = 160 MV		BIAS = 160 MV		
Current (ma)	121.572	Current (ma)	143.979	40.258
Assertion	Negation	Assertion	Negation	
1.402	1.529	1.477	1.575	
0.988	1.123	0.989	1.044	
0.279	0.541	0.429	0.539	
HIGH DRIVE		HIGH DRIVE		
BIAS = 0 MV		BIAS = 0 MV		
Current (ma)	172.144	Current (ma)	193.096	25.824
Assertion	Negation	Assertion	Negation	
1.554	1.542	1.613	1.540	
0.963	0.957	0.963	0.884	
0.597	0.581	0.743	0.583	
BIAS = 160 MV		BIAS = 160 MV		
Current (ma)	173.298	Current (ma)	194.740	26.277
Assertion	Negation	Assertion	Negation	
1.497	1.604	1.564	1.602	
0.900	1.017	0.897	0.938	
0.476	0.704	0.626	0.702	

Boards 5/6

160 mv Bias (excessive Bias, but signals with-in spec)

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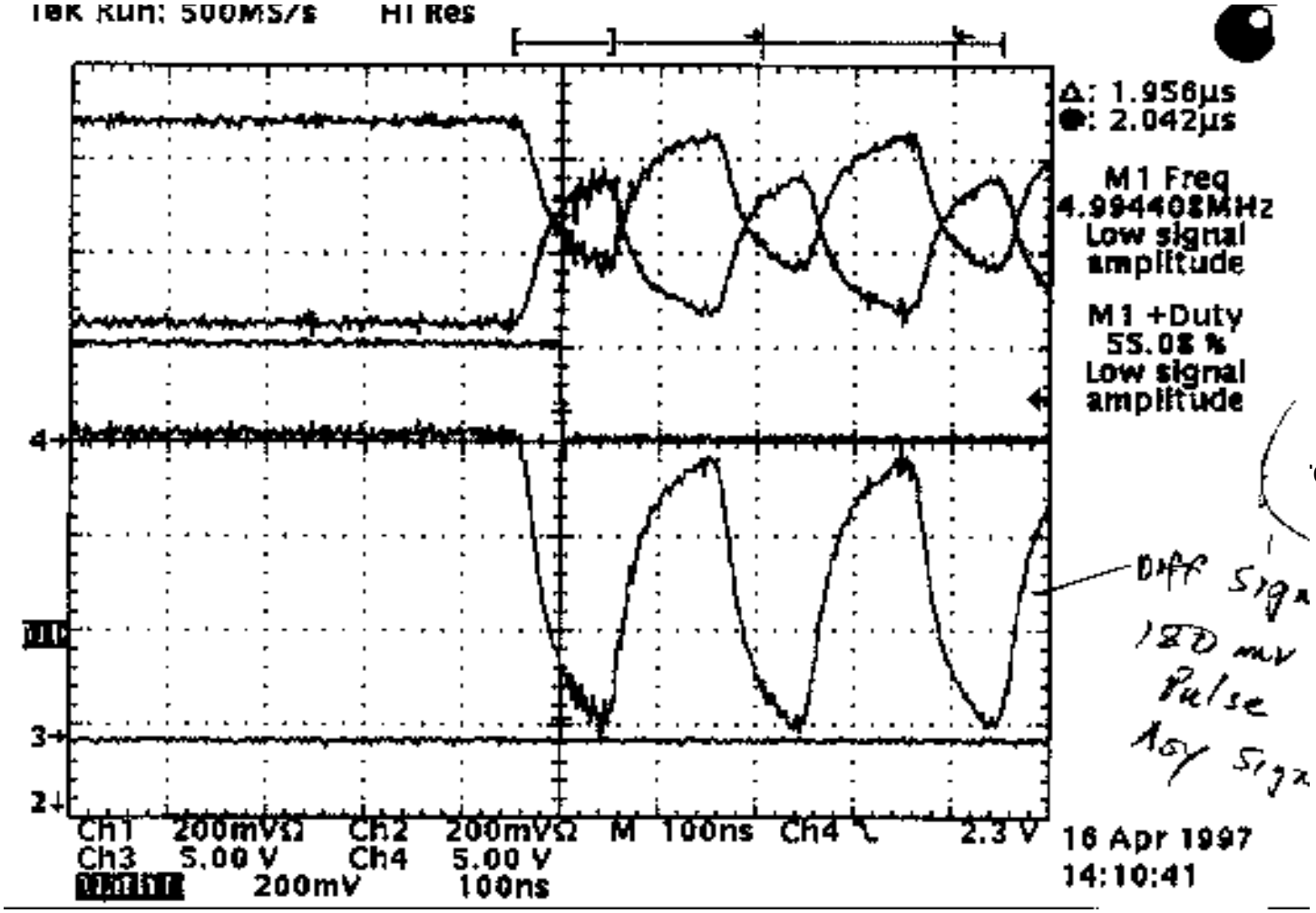
Conclusions On Power

- **Asymmetric Uses More Power Than Symmetric To Overcome Bias By About 25 - 40%**
- **All Signals Shown Are Within SPI 2 Envelope**

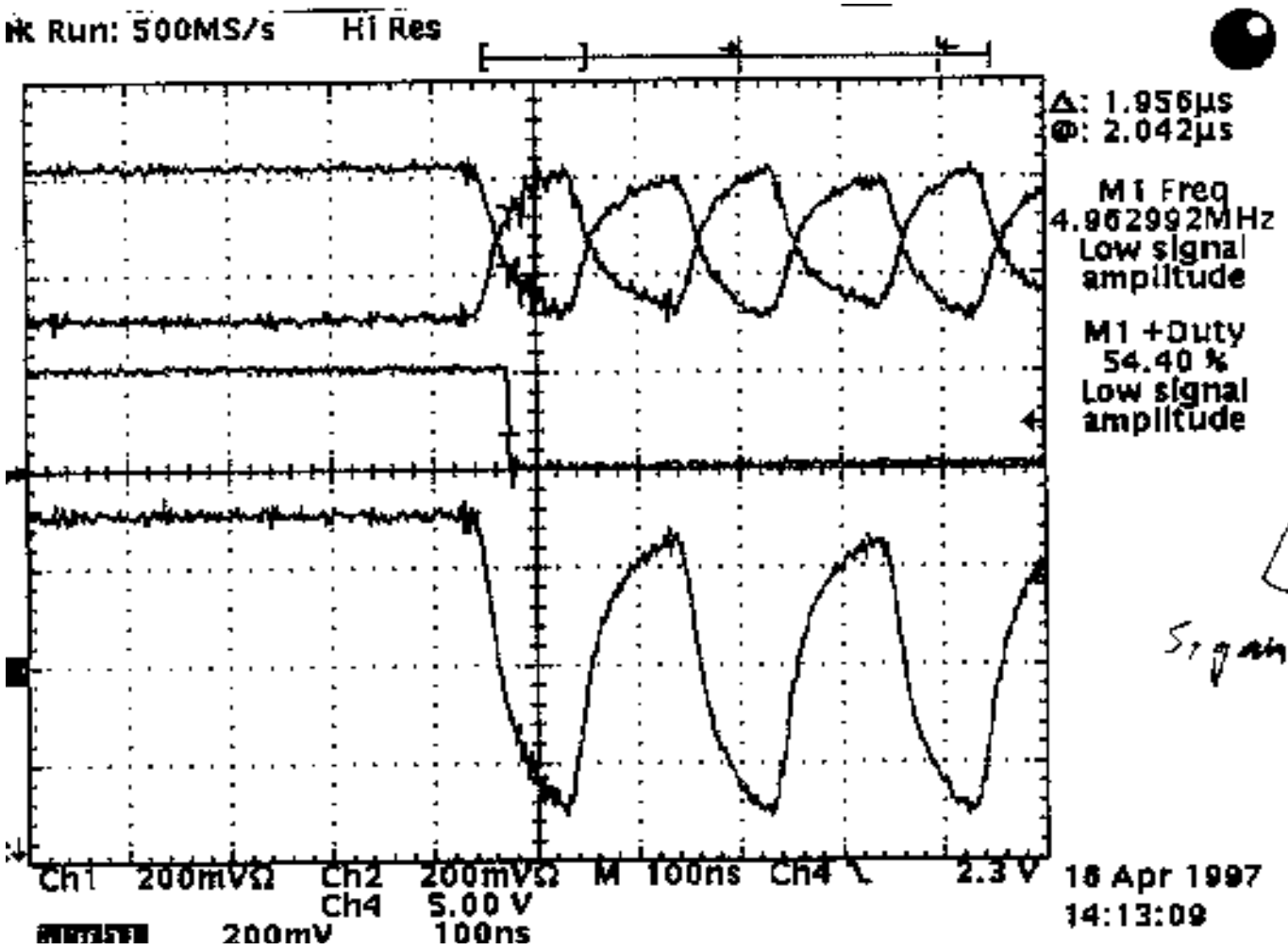
Asymmetric With 125 mv , Bias Nominal Drive



ent = 193

Diff Sig
180 mv
Pulse
Neg Sig

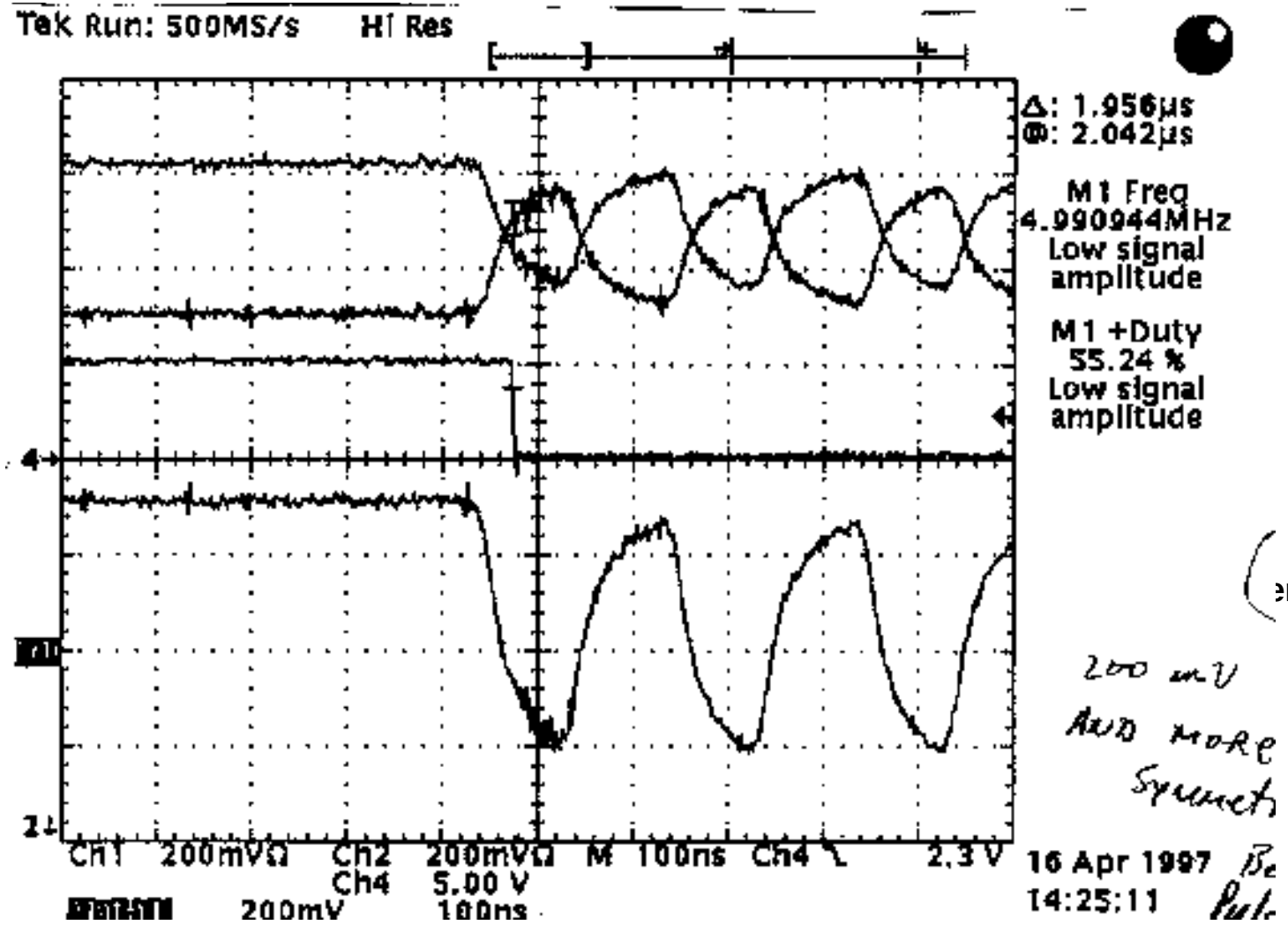
Asymmetric No Bias, Nominal Drive



Cu = 192

Signal 2

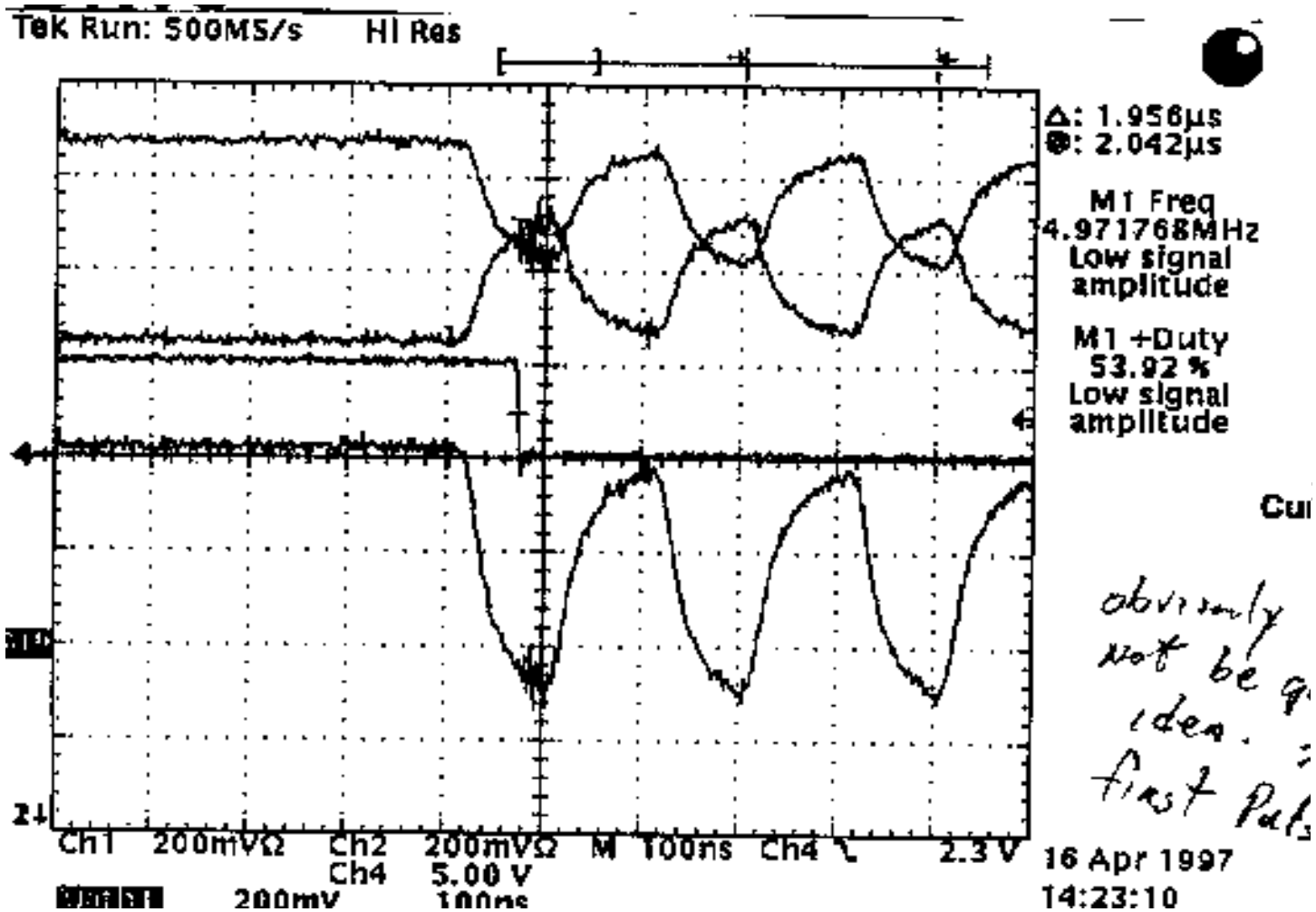
Symmetric With No Bias, Nominal Drive



ent = 171

200 mV
AND more
Symmetry

Symmetric With 125 mv Bias, Nominal Drive



Cu = 171.63

obviously not be g
idea.
first Pul

First Pulse Response Board #6

5 MHz	**First Pulse (mv)**	**Current (ma)**
Symmetrical No Bias	**340**	**207**
Symmetrical Bias	100	207
Asymmetrical No Bias	440	225
Asymmetrical Bias	**100**	**225**
10 MHz		
Symmetrical No Bias	**160**	**207**
Symmetrical Bias	30	207
Asymmetrical No Bias	260	225
Asymmetrical Bias	**100**	**225**
15 MHz		
Symmetrical No Bias	**30**	**207**
Symmetrical Bias	- 90	207
Asymmetrical No Bias	90	225
Asymmetrical Bias	**- 30**	**225**

Max. Frequency For First Pulse Detection

Board #3 125mv Bias

Symmetrical	**No Bias**	**20.6 MHz**
Symmetrical	**Bias**	**13.4 MHz**
Asymmetrical	**No Bias**	**21.5 MHz**
Asymmetrical	**Bias**	**17.9 MHz**

15% Frequency Improvement Using Symmetric With No Bias At Lower Power

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Max. Frequency For First Pulse Detection

Board #5 160 mv Bias

Symmetrical	**No Bias**	**21.27 MHz**
Symmetrical	**Bias**	**21.90 MHz**
Asymmetrical	**No Bias**	**21.90 MHz**
Asymmetrical	**Bias**	**17.33 MHz**

22% Frequency Improvement Using Symmetric With No Bias At Lower Power

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Summary Of Conclusions On Symmetric Unbiased VS Asymmetric Biased

- **Asymmetric Uses 25-40% More Power**
- **Symmetric At Less Power Operates At 15-22% Higher Frequency**
- **Symmetric With Today's Power Levels Provides 30-40% More Margin In Frequency**
- **With Typical Cable Loss At 100 MHz**
  - Asymmetric fails to operate
  - Symmetric works, and even below mini drive spec
- **Provides Headroom For Ultra 4**

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Compatibility Proposal

- **Use Dual Receiver For Ultra 3 Device**
  - One with offset, one without

- **Use Switchable Terminator For Ultra 3**
  - Switchable terminator => Ultra 3 bus
  - Switch removes bias on data, req, ack
  - Other (slow speed) control signals remain biased
  - Terminator gets switch information over bus. Done with input pin or decode of phase and device id. (invention required)

Backward Compatibility

- **Definition: Have 80 MHz Ultra 3 Device Work On Ultra 2 Bus @ 40 MHz**
- **Ultra 2 Bus Is Biased So Dual Mode Ultra 3 Device Has No Problem Operating On Biased Bus**

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Forward Compatibility

- **Definition: Have 40 MHz Ultra 2 Device Work On Ultra 3 Bus @ 40 MHz**
- **Ultra 3 Bus Is Biased During All Phases Except Data Transfer Phases**
- **Ultra 2 Device Operates As Normal @ 40 MHz**
- **For Ultra 3 Device At Data Transfer Time Ultra 3 Device Asserts Line To Remove Bias From Bus**

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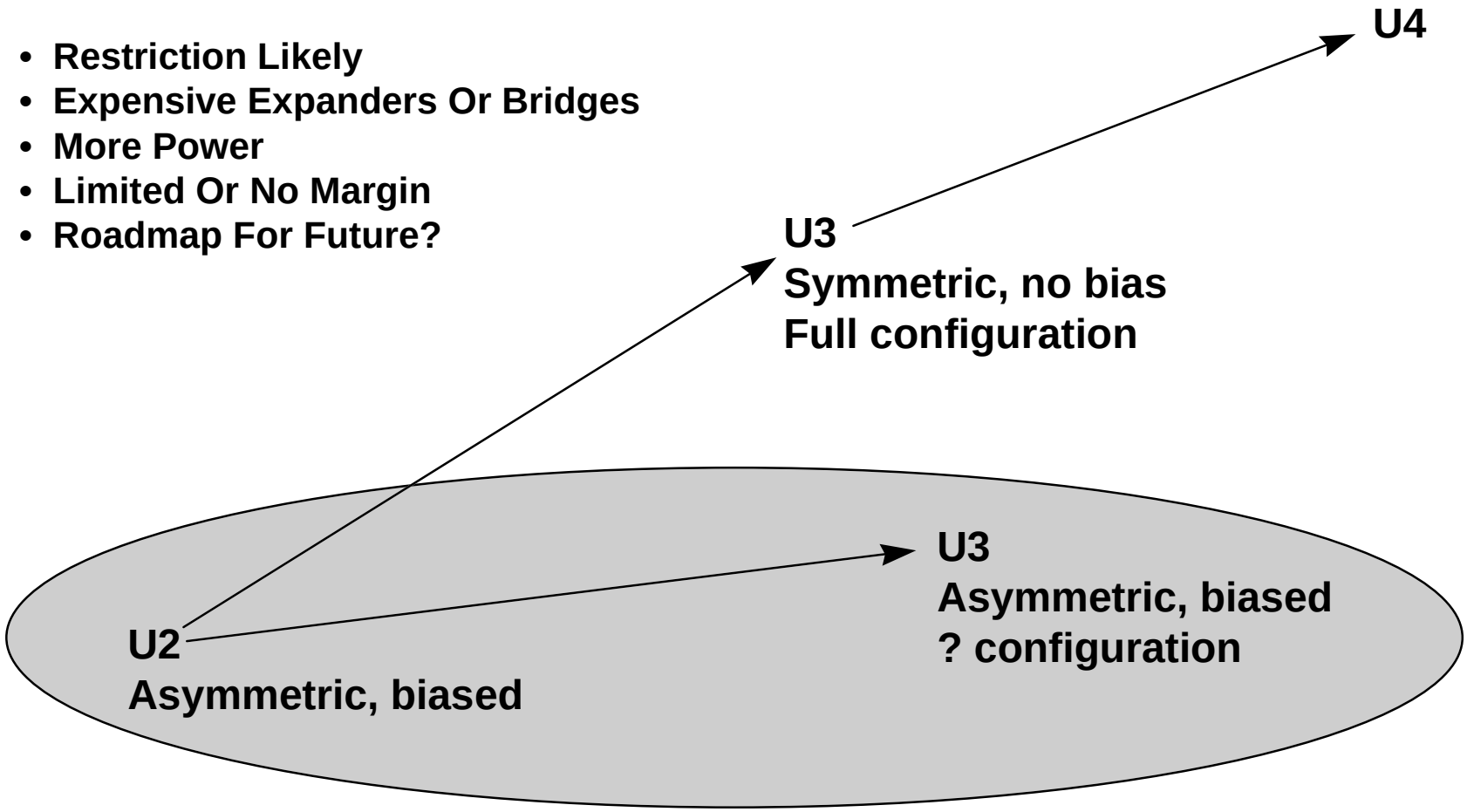
Possible Roadmap 1

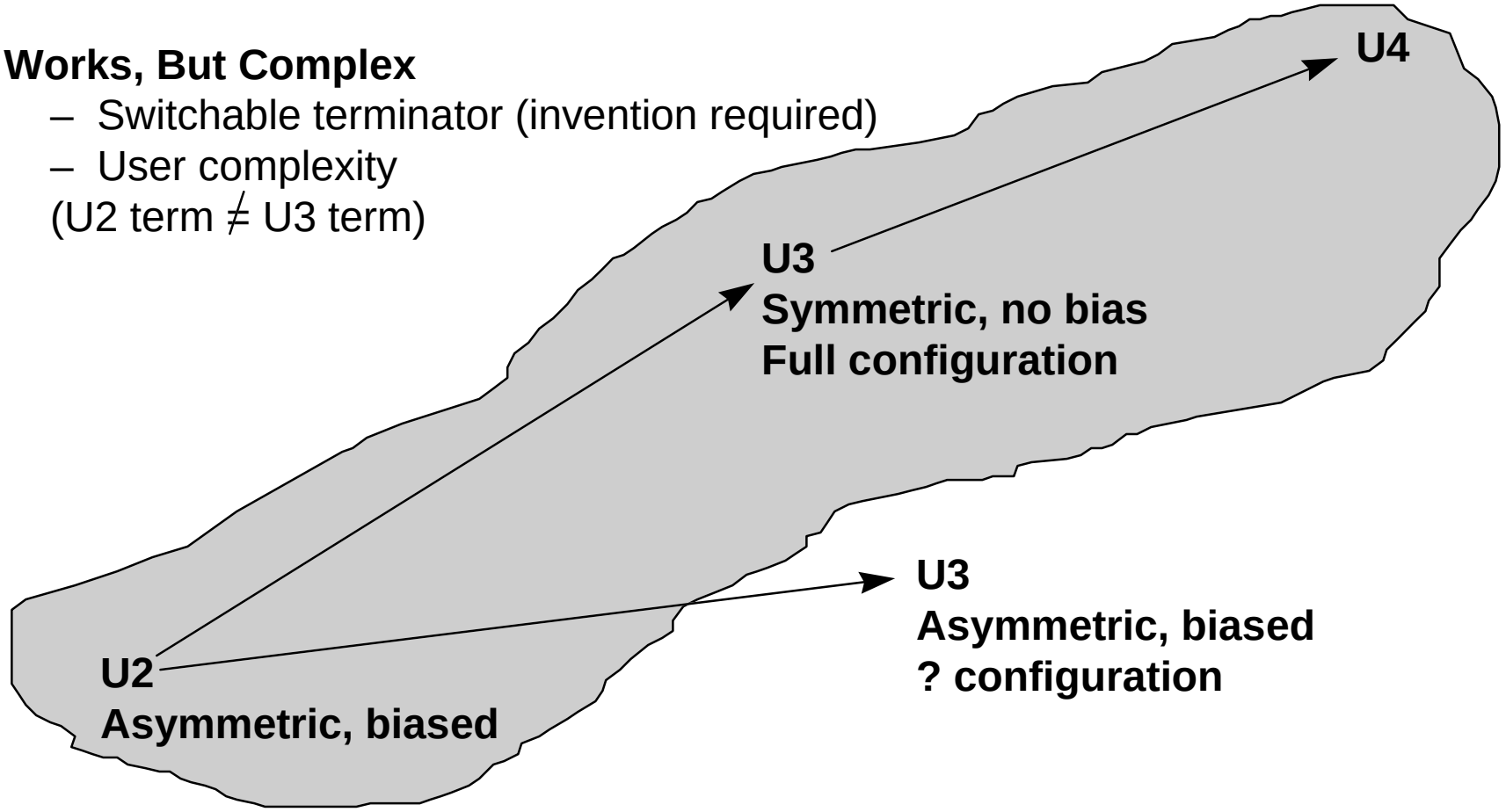
- Restriction Likely
- Expensive Expanders Or Bridges
- More Power
- Limited Or No Margin
- Roadmap For Future?



Possible Roadmap 2

- **Works, But Complex**
  - Switchable terminator (invention required)
  - User complexity

  (U2 term ≠ U3 term)



Possible Roadmap 3

- Simplest Migration For Implementors & Users
- Lower Power
- Must Decide Now To Avoid Chaos