Fast Forward to the Future

- *Ultra 2/LVD is the first major change to the mainstream SCSI physical interface since SCSI was introduced. It s a technological leap!*
- *Market expectations: SCSI is a desirable technology because it has built in backward compatibility. My investment is protected.*
- *Question: If I adopt this technology, does this stuff have headroom?*
- *First Order response: LVD technology is an excellent platform on which to build for the future. It appears to cure many of the ills of a single ended interface.*

Is LVD SCSI Scaleable Beyond Ultra-2?

- *Adaptec believes that the present LVD SCSI works at 40MHz*
- *Question: Do the tradeoffs made to produce Ultra 2 promote an easily scaleable technology?*
  - *Studies presented here a year ago and in November indicate adverse effects at higher speeds*
    - **DC imbalance on symmetry of the signal.**
    - **first pulse symmetry distortion**
    - **adverse effects of asymmetry on timing margins.**
  - *Multidrop studies have not been presented!*
  - *Characterization is not complete!*

What Will Be Presented Today

- *Adaptec has developed a test chip and conducted measurements in an Ultra 2 multidrop environment.*
- *A discussion of the test environment and the measurements made in an Ultra 2 compliant setup is offered*
- *Supporting analysis will also be shared*
- *A discussion of approaches to symmetric design and the practicality of their implementation.*
- *Review and comment on possible methods to extend current Ultra 2.*
- *A strawman proposal for Ultra-3*
- *Compatibility considerations*

SCSI LVDS Testing

- Test Chip/Test Setup
- Empirical Results
- Analysis
- Conclusions on extensibility to higher frequency
- Ideas to obtain better margins at higher rates

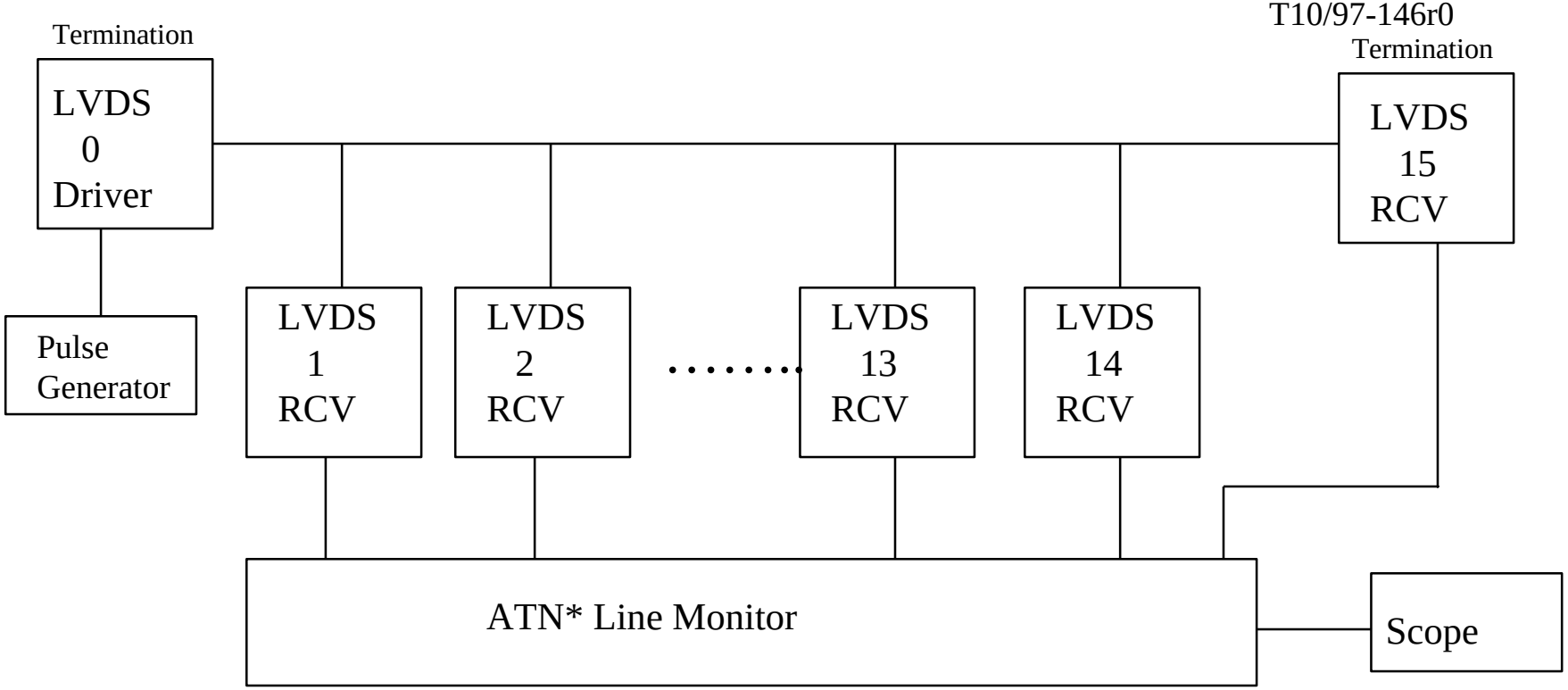
Test Process

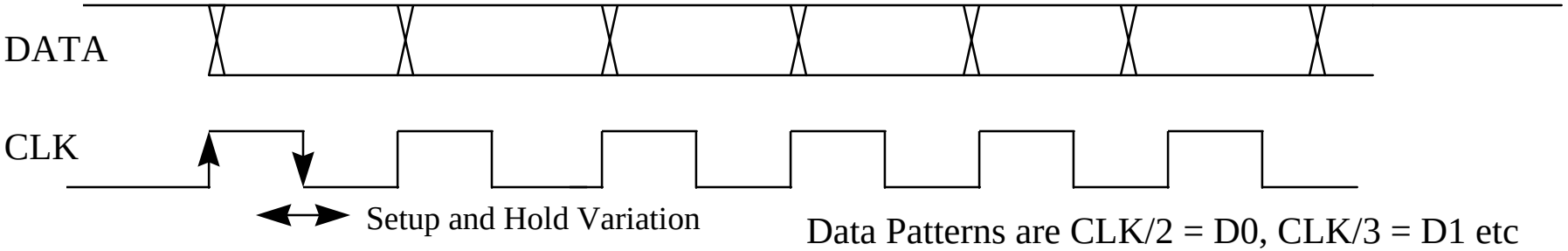
- Used test chip developed to verify Ultra 2 Design.
- Test chip provided way to evaluate margin of the REQ/ACK pulse in clocking data.
- Testing done at 80 Mtransfer and beyond to understand the extensibility of the current specification.

Test Chip/Board

Implements current Ultra 2 specification, but certain parameters can be varied.

- Can switch to symmetric or asymmetric drivers.
- Can be used with biased or non-biased terminator.
- Test setup allows clocking of data lines as well as REQ/ACK so the ability to strobe data successfully can be determined.
- Setup and hold time control allows detection of faults when sampling data.
- Test chip allows first pulse experiment to determine if a loaded line will cause errors.





Data Patterns are CLK/2 = D0, CLK/3 = D1 etc
Can do bursts or continuous clocking

Testing done for:

- Different Cable lengths and speeds.
- Configurations run with symmetric/asymmetric drivers at 40 and higher.

Monitored:

- Level of first pulse amplitude after long period of constan
- Determination of the range of Setup/Hold times where no dat

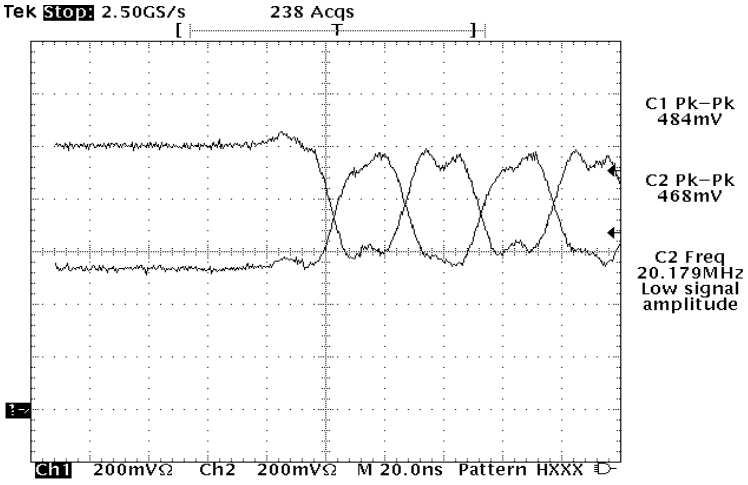
First Pulse Testing

First pulse Vs second pulse voltage swings

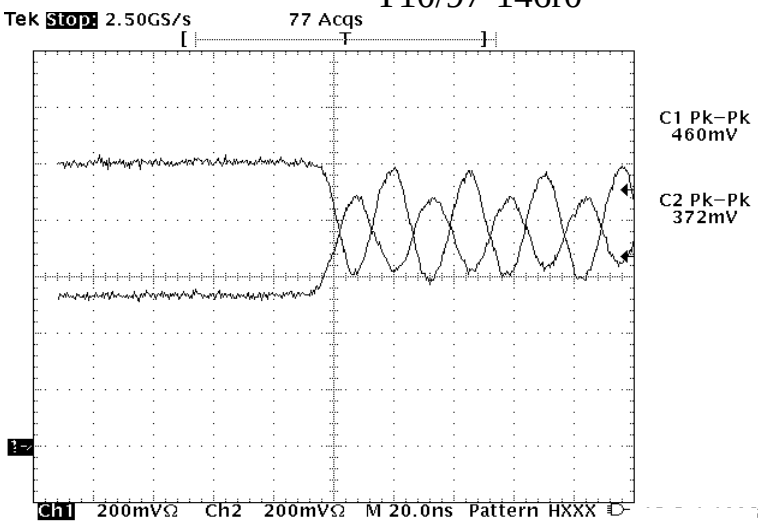
Cable Length	# of Loads	Clock Frequency	First pulse swing	Second pulse swing
8m	16	20 MHz	400 mV pp	468 mV pp
8m	16	40 MHz	295 mV pp	372 mV pp
8m	16	60 MHz	210 mV pp	240 mV pp
8m	16	80 MHz	65 mV pp	196 mV pp
12m	16	20 MHz	370 mV pp	428 mV pp
12m	16	40 MHz	240 mV pp	376 mV pp
12m	16	60 MHz	80 mV pp	225 mV pp
12m	16	80 MHz	Fail	Fail

Shows problem at 80 Mtransfers for first pulse detection.

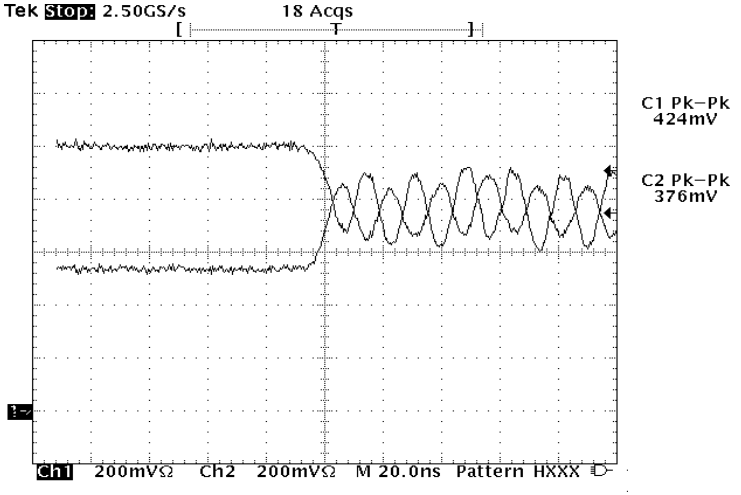
20 MHZ



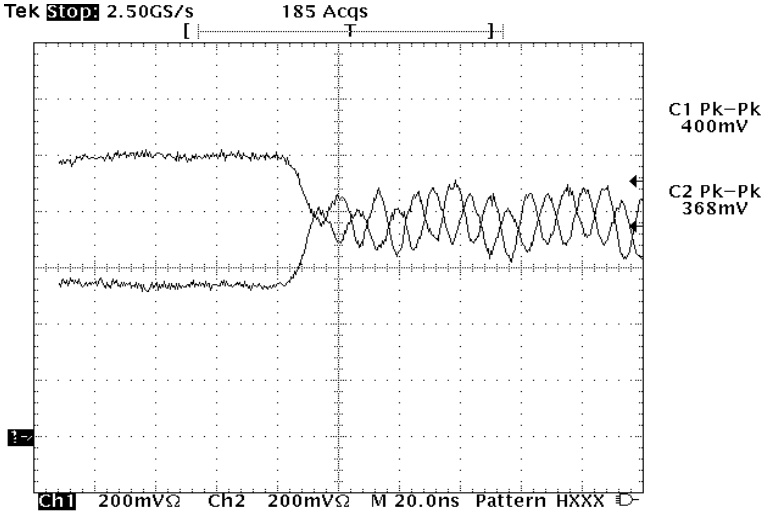
40 MHZ



60 MHZ



80 MHZ

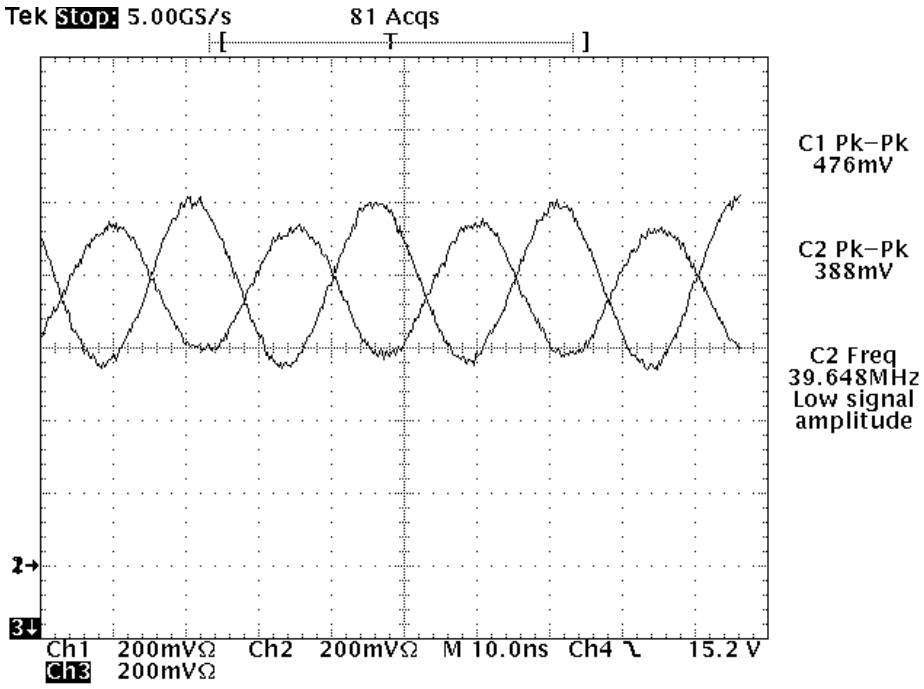


Setup and Hold Time Margins with driver in different cable p

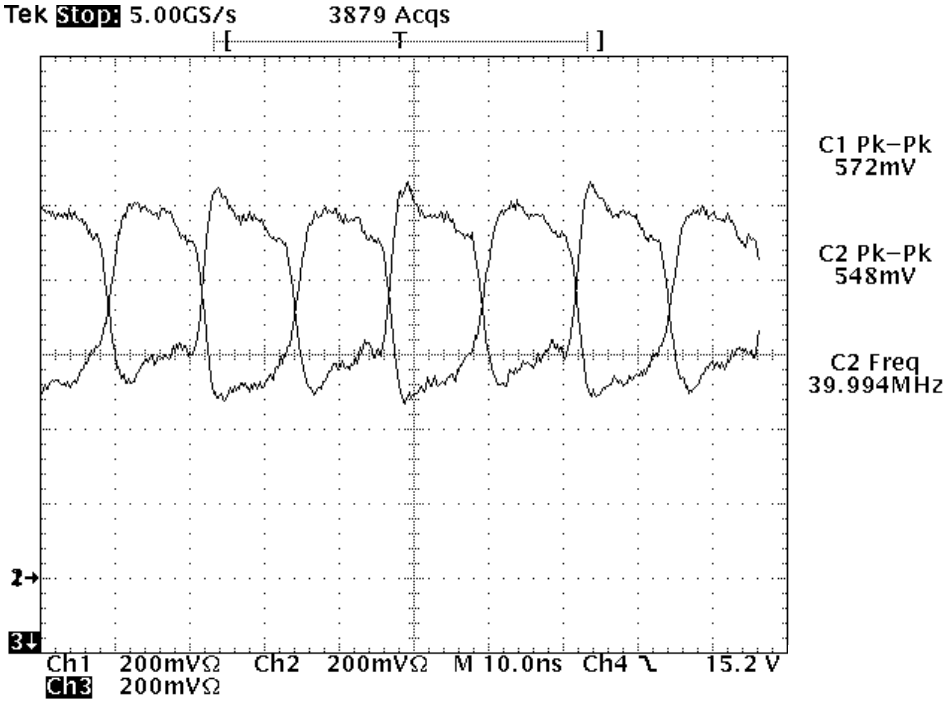
Driver position	UDT Receiver position	Cable length	frequency	Max. duty cycle	Min. duty cycle	Setup/Hold
1	16	12m	40 MHz	74%	24%	12.5
2	16	12m	40 MHz	70%	39%	9.75
3	16	12m	40 MHz	65%	42%	5.75
4	16	12m	40 MHz	56%	41%	3.75
5	16	12m	40 MHz	39%	36%	0.75
6	16	12m	40 MHz	78%	63%	3.75
7	16	12m	40 MHz	78%	58%	7.5 n
8	16	12m	40 MHz	65%	57%	2.0 n
9	16	12m	40 MHz	79%	49%	7.5 n
10	16	12m	40 MHz	73%	60%	3.25
11	16	12m	40 MHz	77%	64%	3.25
12	16	12m	40 MHz	79%	64%	3.75
13	16	12m	40 MHz	68%	57%	2.75
14	16	12m	40 MHz	64%	36%	7.0 n
15	16	12m	40 MHz	77%	39%	9.5 n

Duty cycles not consistent.

Position 5 Signal Quality



Position 15 Signal Quality



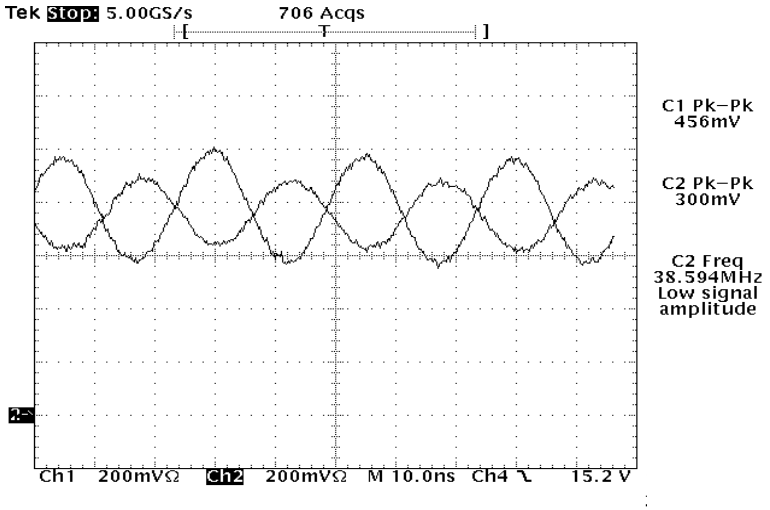
Setup and Hold Time Margins at Increased Speed

Cable Length	# of Loads	Clock Frequency	Max. Duty Cycle	Min. Duty Cycle	Duty Cycle Range	Setup/Hold Margin	LVD signal-swing
8m	16	40 MHz	74%	29%	45%	11.25 ns	456 mV p
8m	16	60 MHz	see note 1	see note 1	see note 1	see note 1	240 mV p
8m	16	80 MHz	failed	failed	failed	failed	208 mV p
12m	16	40 MHz	74%	24%	50%	12.5 ns	456 mV p
12m	16	60 MHz	58%	47%	11%	1.82 ns	252 mV p
12m	16	80 MHz	49%	40%	9%	1.12 ns	200 mV p

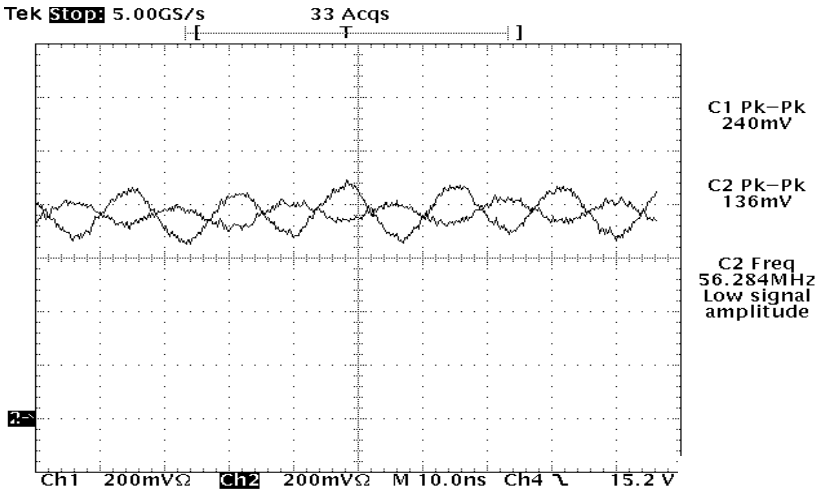
Table 1. Setup/Hold Time Data, fully-loaded configuration, asymmetrical outputs

Note 1: Data miscompare occurs at one point over the range of duty cycle adjustment.
38% to 45% : passed
46% to 53% : failed
54% to 64% : passed

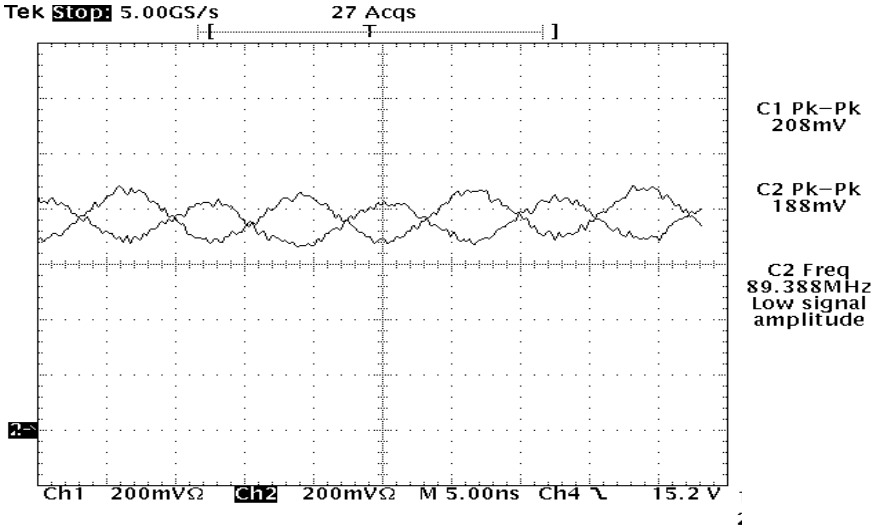
LVD Signals 40 MHZ, 8 Meter Cable, Asymmetrical Driver



LVD Signals 60 MHZ, 8 Meter Cable, Asymmetrical Driver



LVD Signals 80 MHZ, 8 Meter Cable, Asymmetrical Driver



Bias Terminator and Asymmetrical Drivers

- From testing it would appear asymmetric drivers may not be s compensate for bias in the terminator at higher speeds. This caused by the cable and capacitance.

- An investigation into the effect bias has on the terminator this represents a noise source which causes distortion of th resulting in mis-clocking of the data (REQ/ACK).

- Different current sources required for asymmetrical drive re variations and bias in terminator also result in large tolera These errors will affect timing margin.

Determination of Setup and Hold Time Margins.

0.5 Meter cable in continuous run mode

Measurement Mode	80 MHz duty cycle	120 MHz duty cycle	160 MHz duty cycle	200 MHz duty cycle	Comments
no bias/ symmetrical	19 to 73% 54	26 to 63% 37	29 to 58% 29	35 to 47% 12	Proposed LVD Spec
no bias/ asymmetrical	19 to 73% 54	27 to 64% 37	29 to 59% 30	36 to 49% 13	
0.1 V bias/ symmetrical	18 to 70% 52	24 to 58% 34	26 to 50% 24	30 to 37% 7	Early LVD Spec
0.1 V bias asymmetrical	18 to 72% 54	24 to 60% 36	26 to 52% 26	30 to 40% 10	Current LVD Spec

Non-Biased Terminator and Symmetrical Drivers

- From testing, symmetric drivers with no bias can do as well a
  at lower power. Could get more margin for same power.
- There is no tolerance problem with this setup since there is
  and no bias.
- Could more easily build a driver that provided an increased
  overcome any problems with sensing the first pulse after a d
- Symmetric drives with no bias is the way everyone else handl
- Symmetric drivers will make future speed extensions easier.

Summary Of Predictions For Higher Speeds

Loss Of Signal Amplitude And Asymmetry As Shown In Test Data

Major Effects Contributing To Losses

- Capacitive loading of bus
- Conductor skin effect
- Lossy dielectric

Quantification Of Losses (40 to 80MT)

- 50% loss of asymmetry at receiver (short bus)
- Additional 50% loss; with a long bus - 25M (both symmetry and signal)

Evaluation Of PH Layer Improvement Alternatives

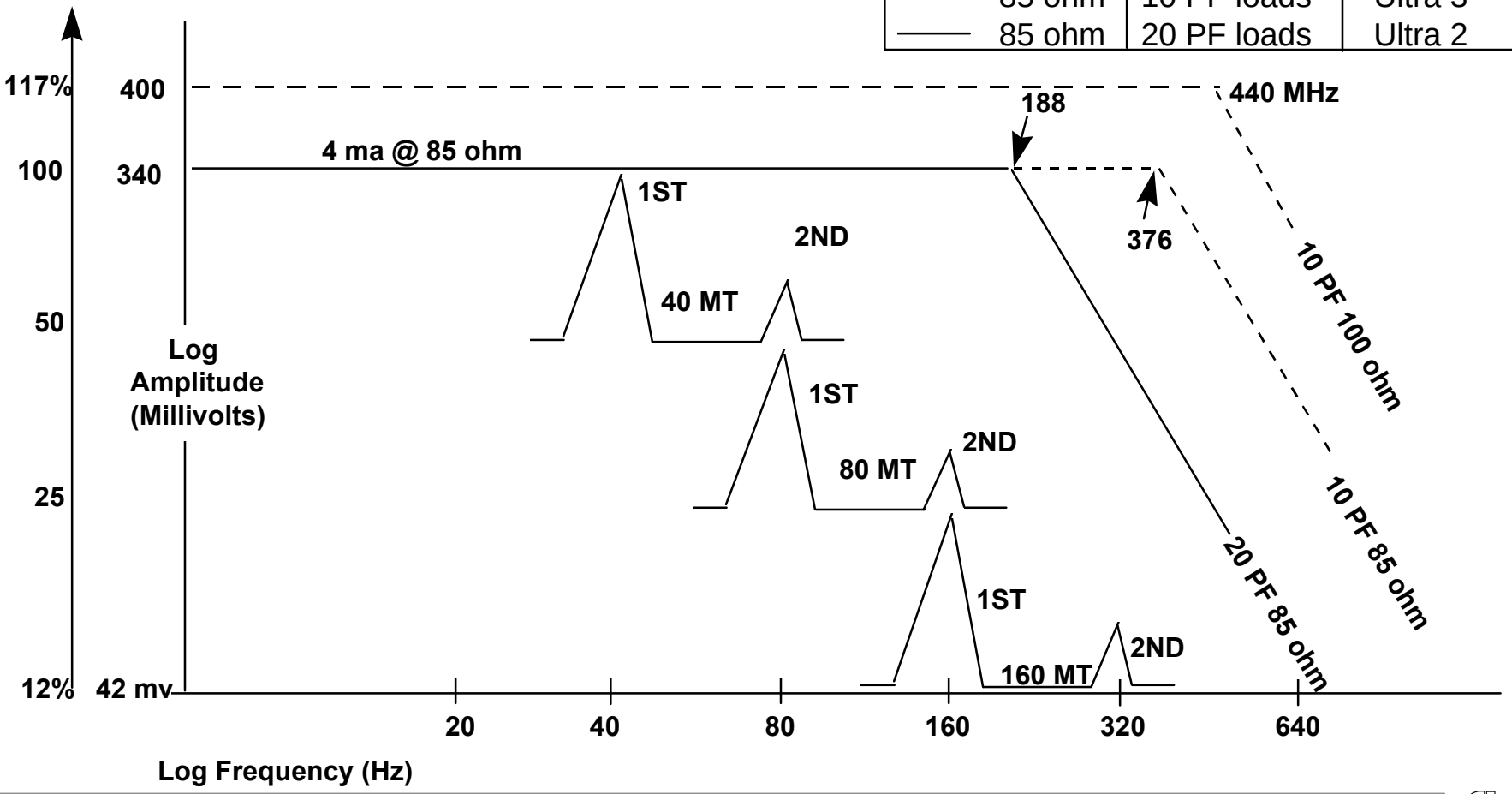
More Signal	Results	Issues
Increase Drive Current 50%	More Power; Asymmetry % Same	Higher Power
Increase Load Spacing	2X Yields 140% Bandwidth	Legacy & Backplanes
Lower CIN	Cin< 10PF Yield 200% Bandwidth	Evolution of ASIC Design

Less Noise	Results	Issues
Delete Asymmetry At Drivers	Greater Margin; Must Change Receivers & Terminators	New Receiver Design
Improve Termination	Reduced Reflections; Must Change Spacing Rules And/ Or Terminators	Legacy

T10/97-146r0

LVD Bus - Amplitude vs Frequency

Impedance	Load	Uses
100 ohm	10 PF loads	Ultra 3 pp
85 ohm	10 PF loads	Ultra 3
85 ohm	20 PF loads	Ultra 2



Bus Current Waveforms

Fundamental @ 40 MHz

Amplitude vs Time

Amplitude vs Frequency

(a) Asymmetrical Waveforms

(b) Symmetrical Waveforms

Notes:

(1) Current Probe Differential; 120 MHz

(2) Change in 80 & 160 MHz (Even Harmonics)

Issue: Ultra 2 uses a bias voltage on terminator
has been found to be detrimental to hig
operation.

But: Bias is required to assure the receivers wi
a non asserted state if bus is not drive

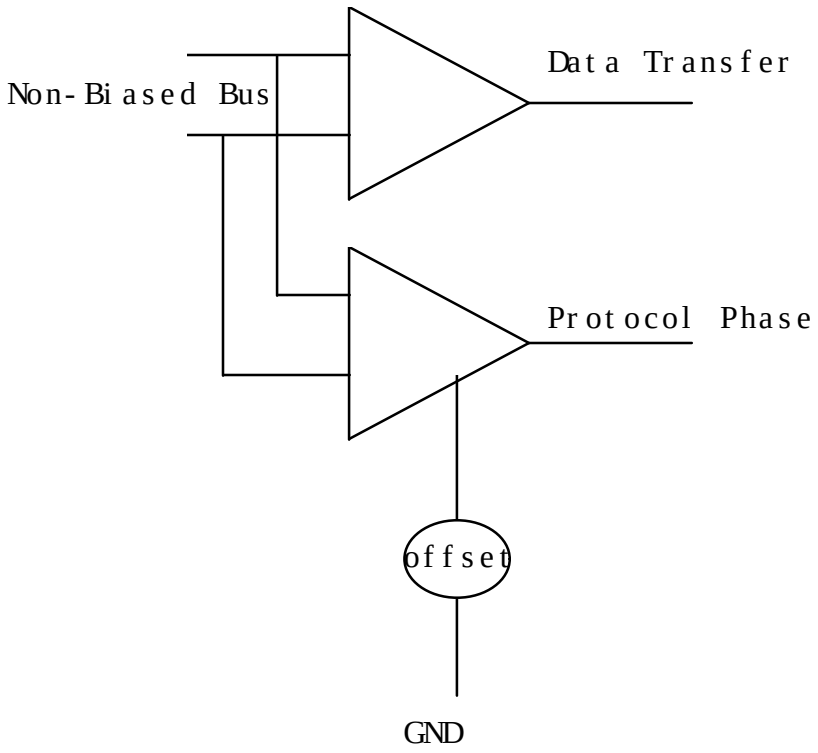
And: We need to keep backwards compatibility betw
Ultra 2 and Ultra 3.

Ultra 3 Strawman Definition

- 80 Mtransfers per Second
- 12 Meter max length
- 16 Loads
- 25 Meter max length point to point
- Load Capacitance 10/10/5
- Terminator unbiased
- Drivers are symmetrical

Ultra 3 Proposed Receiver

To use no bias at high speed must assure undriven is detected as non-asserted.



Receiver with offset was proposed for Ultra 2 but de no better than biased termi

In this case offset receive only for protocol not data t Therefore, have non-asserte state for arbitration and b possible situation for data

Dual Receiver Design Considerations

Primary Data Receiver, High Speed, Low Offset

Secondary Protocol Phase Receiver

- ~130mV +/- 20% built-in offset
- Low speed, ~50ns delay time will be fine
- A very low power design still has good speed with a multiple stage design
- Small area, Vt offset design can be ~3200 square micron in 0.6µ process. This is ~1-3% of pad area.
- Low input capacitance. Small input transistors can be used, they would add ~0.05pf to the pin capacitance

Design Examples

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Compatibility Goal

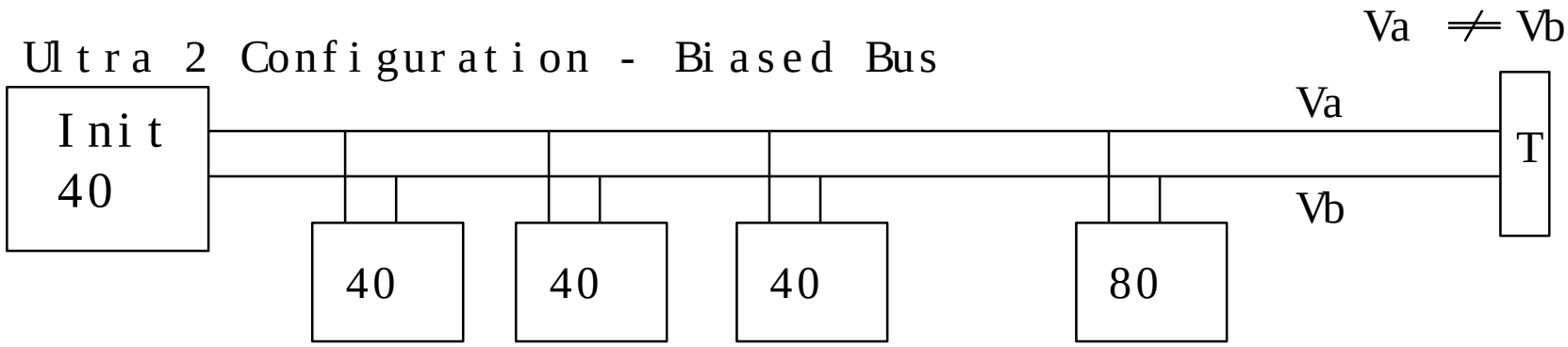
Want to have compatibility between Ultra 2 and Ult

Compatibility is defined as being able to have Ult device work on Ultra 3 and vice versa.

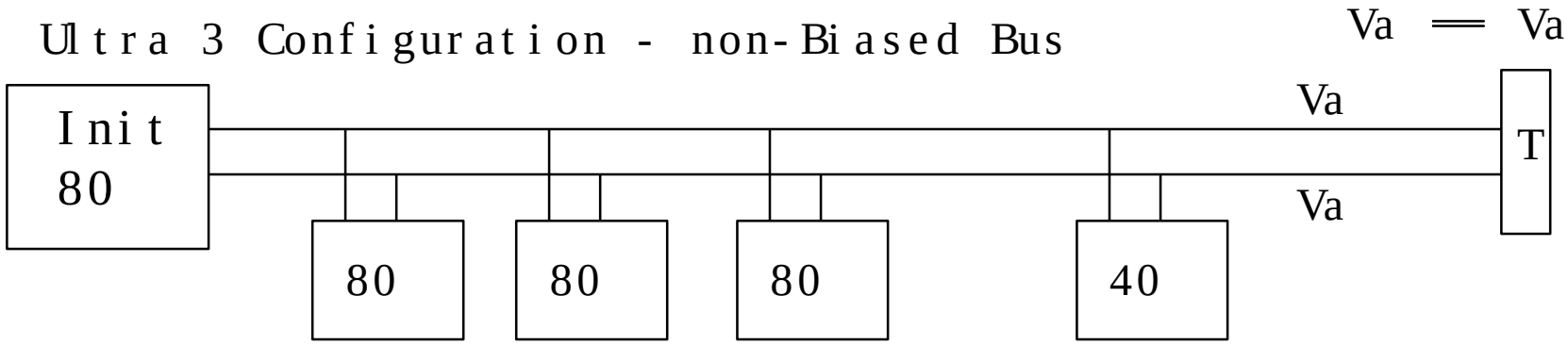
Compatibility Goal

Backward Compatibility - 2 Cases

Ultra 2 Configuration - Biased Bus



Ultra 3 Configuration - non-Biased Bus



Compatibility Goal

Three Approaches:

A

- Keep Ultra 2 as is.
- Have Ultra 3 require a Ultra 2 mode.
- Use a Ultra 2 to Ultra 3 adapter.

B

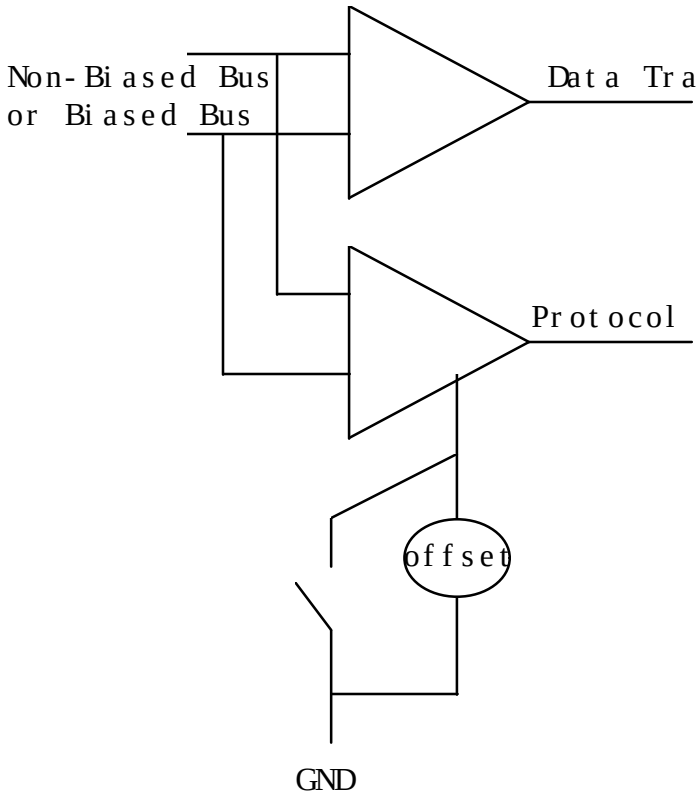
- Define an Ultra 2A receiver design.
- Build Ultra 3 and Ultra 2A with support for b non-biased bus.

C

- Change Ultra 2 to an non-biased bus

Approach A

Ultra 3/2 Receiver Design



In Ultra 3 mode the switch is

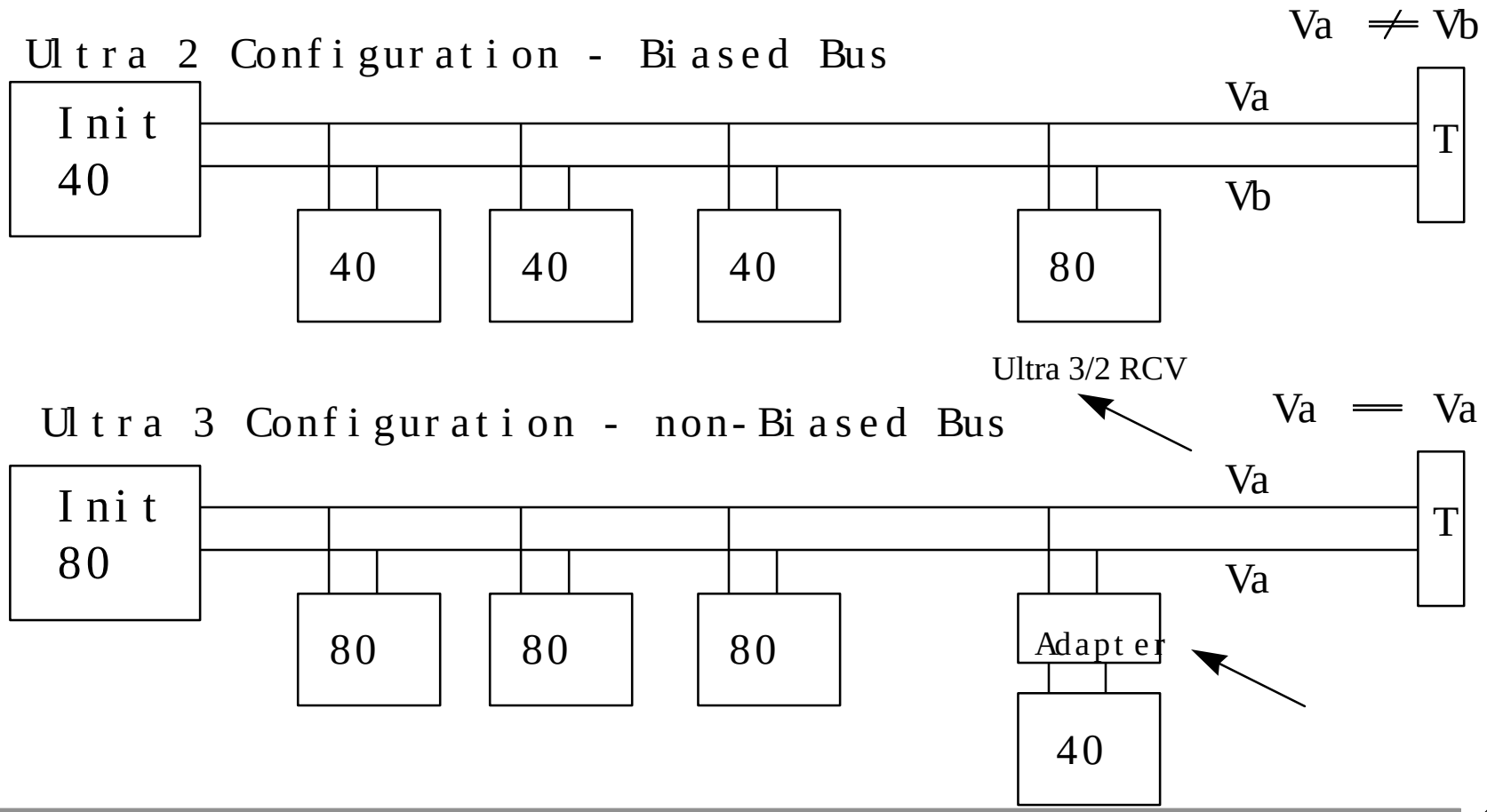
In Ultra 2 mode the switch is use is made of the biased bus.

This receiver will work on cur (biased bus) system as well as Ultra 3 system.

Current Ultra 2 defined receiv need an adapter on a non-biase

Approach A

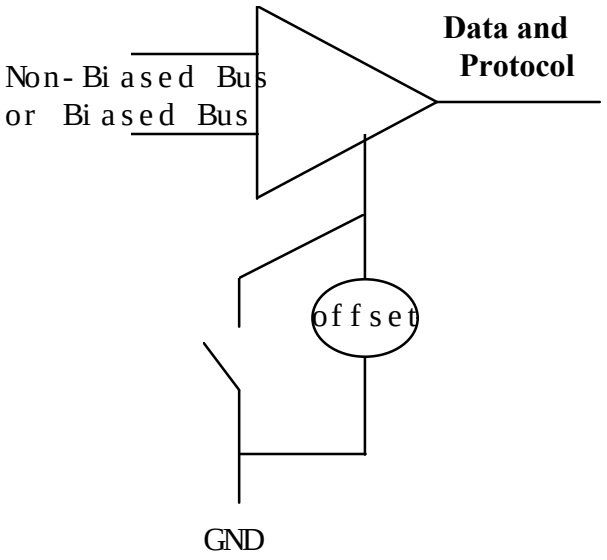
Backward Compatibility - 2 Cases



Approach **B**

Ultra 2A Receiver Design

To make Ultra 2 device work on a non-Biased bus the Ultra 2 receiver to be as follows.

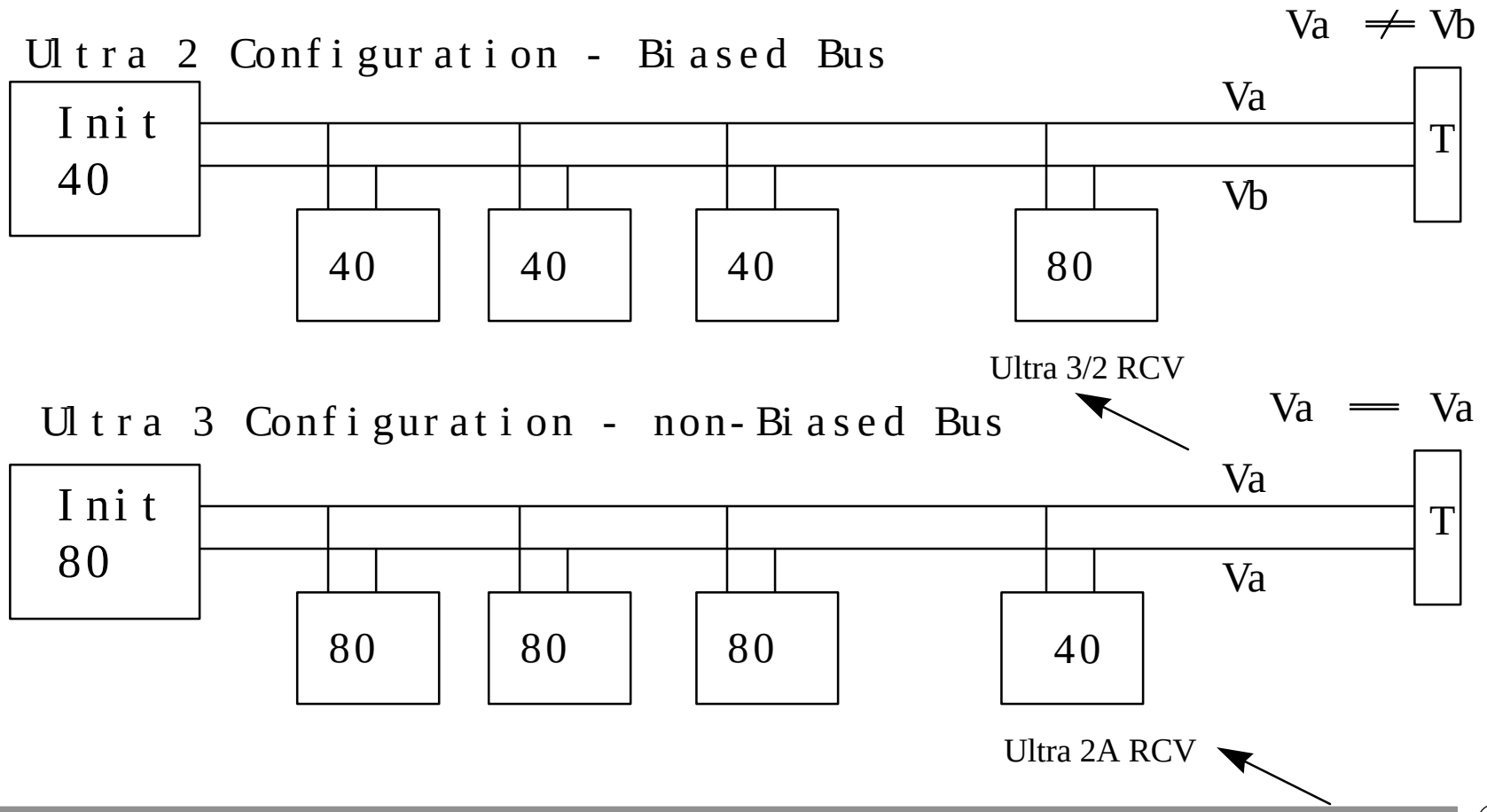


In this configuration operating o bus (with bias) switch is closed terminator bias is used.

When operated on Ultra 3 bus with the switch is open, the offset as receiver sees a non-asserted stat bus is not driven. Note the recei at a maximum of 40 Mtransfers.

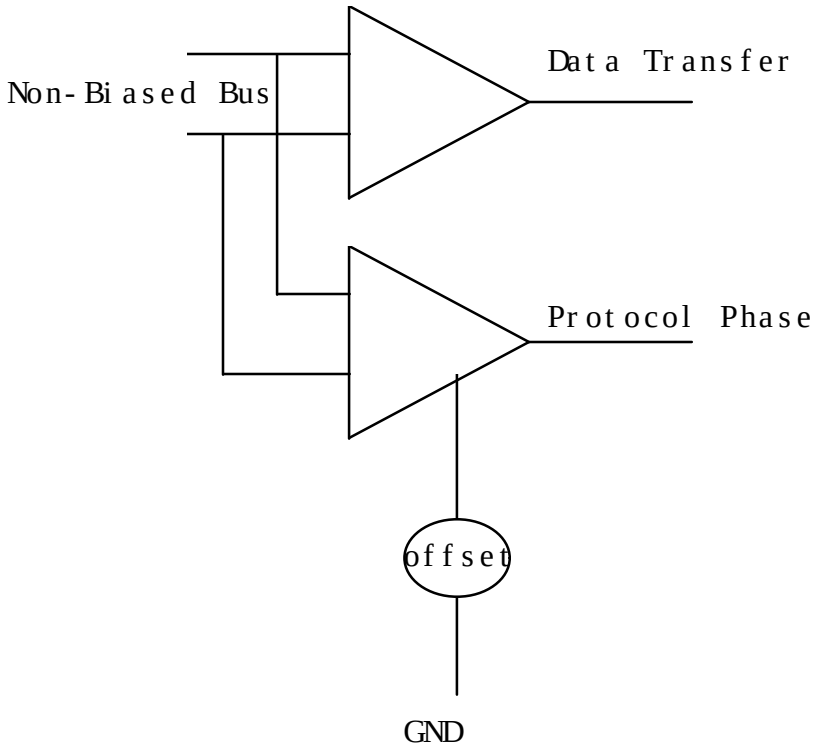
Approach B

Backward Compatibility - 2 Cases



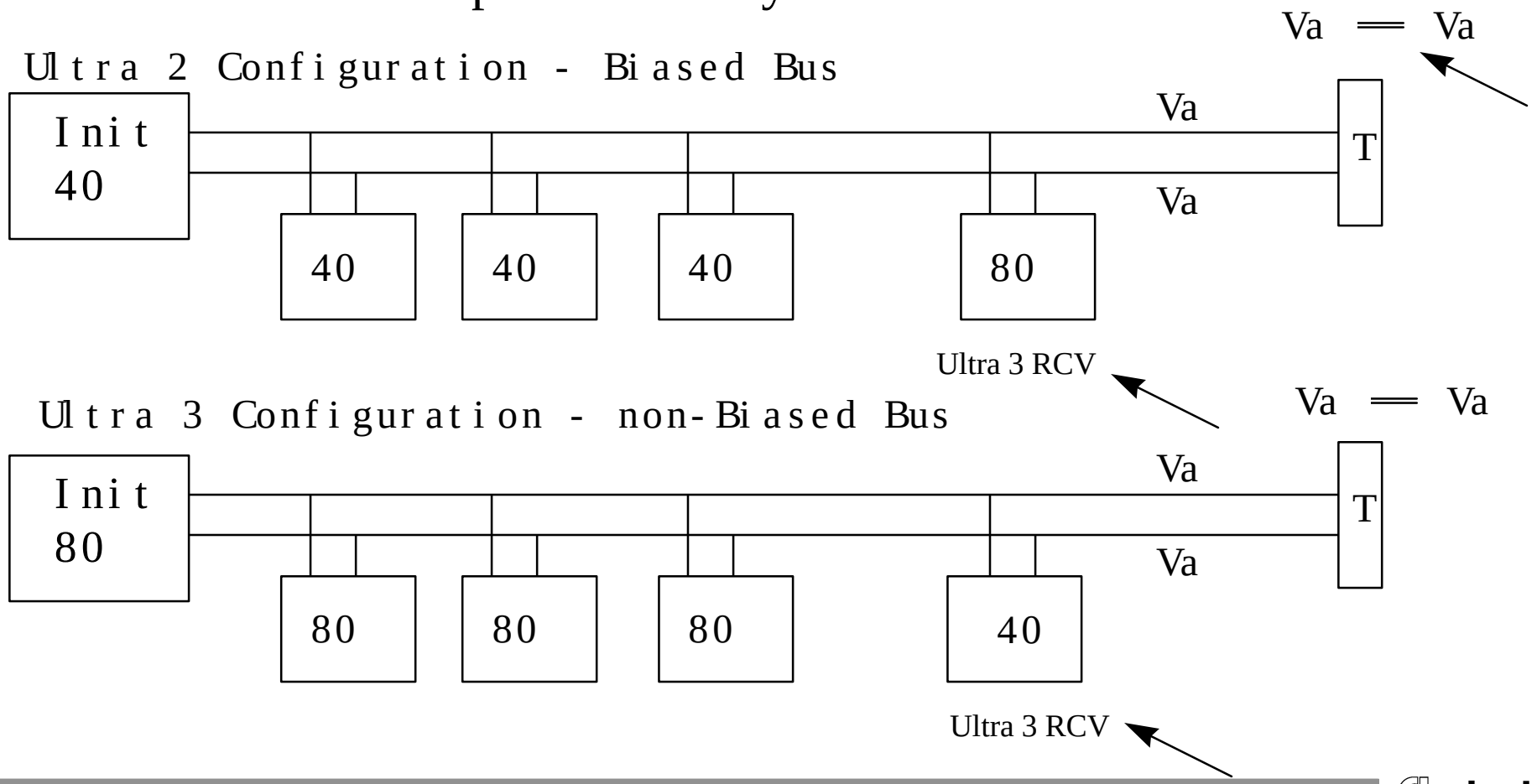
Approach C

Change Ultra 2 to an non-biased bus. The new rece both becomes as shown for Ultra 3 receiver.



Approach C

Backward Compatibility - 2 Cases



Summary

Changing LVDS to a non-biased bus provides additional margin for extending the bus more easily to higher speed operation.

Backward compatibility can be achieved using one of several different ideas presented.