Fast Forward to the Future

- Ultra 2/LVD is the first major change to the mainstream SCSI physical interface since SCSI was introduced. It's a technological leap!

- Market expectations: SCSI is a desirable technology because it has built in backward compatibility. My investment is protected.

- Question: If I adopt this technology, does this stuff have headroom?

- First Order response: LVD technology is an excellent platform on which to build for the future. It appears to cure many of the ills of a single ended interface.
Is LVD SCSI Scaleable Beyond Ultra-2?

Adaptec believes that the present LVD SCSI works at 40MHz

Question: Do the tradeoffs made to produce Ultra 2 promote an easily scaleable technology?

Studies presented here a year ago and in November indicate adverse effects at higher speeds

- DC imbalance on symmetry of the signal.

- First pulse symmetry distortion

- Adverse effects of asymmetry on timing margins.

Multidrop studies have not been presented!

Characterization is not complete!
What Will Be Presented Today

- Adaptec has developed a test chip and conducted measurements in an Ultra 2 multidrop environment.

- A discussion of the test environment and the measurements made in an Ultra 2 compliant setup is offered.

- Supporting analysis will also be shared.

- A discussion of approaches to symmetric design and the practicality of their implementation.

- Review and comment on possible methods to extend current Ultra 2.

- A strawman proposal for Ultra-3.

- Compatibility considerations.
SCSI LVDS Testing

• Test Chip/Test Setup
• Empirical Results
• Analysis
• Conclusions on extensibility to higher frequency
• Ideas to obtain better margins at higher rates
Test Process

• Used test chip developed to verify Ultra 2 Design.

• Test chip provided way to evaluate margin of the REQ/ACK pulse in clocking data.

• Testing done at 80 Mtransfer and beyond to understand the extensibility of the current specification.
Test Chip/Board

Implements current Ultra 2 specification, but certain parameters can be varied.

• Can switch to symmetric or asymmetric drivers.

• Can be used with biased or non-biased terminator.

• Test setup allows clocking of data lines as well as REQ/ACK so the ability to strobe data successfully can be determined.

• Setup and hold time control allows detection of faults when sampling data.

• Test chip allows first pulse experiment to determine if a loaded line will cause errors.
DATA

CLK

Setup and Hold Variation

Data Patterns are CLK/2 = D0, CLK/3 = D1 etc
Can do bursts or continuous clocking

Pulse Generator

LVDS 0 Driver

LVDS 1 RCV

LVDS 2 RCV

……...

LVDS 13 RCV

LVDS 14 RCV

Termination

LVDS 15 RCV

Scope

ATN* Line Monitor

T10/97-146r0

Termination

……..
Testing done for:

- Different Cable lengths and speeds.
- Configurations run with symmetric/asymmetric drivers at 40 and higher.

Monitored:

- Level of first pulse amplitude after long period of constant
- Determination of the range of Setup/Hold times where no dat
First Pulse Testing

First pulse Vs second pulse voltage swings

<table>
<thead>
<tr>
<th>Cable Length</th>
<th># of Loads</th>
<th>Clock Frequency</th>
<th>First pulse swing</th>
<th>Second pulse swing</th>
</tr>
</thead>
<tbody>
<tr>
<td>8m</td>
<td>16</td>
<td>20 MHz</td>
<td>400 mV pp</td>
<td>468 mV pp</td>
</tr>
<tr>
<td>8m</td>
<td>16</td>
<td>40 MHz</td>
<td>295 mV pp</td>
<td>372 mV pp</td>
</tr>
<tr>
<td>8m</td>
<td>16</td>
<td>60 MHz</td>
<td>210 mV pp</td>
<td>240 mV pp</td>
</tr>
<tr>
<td>8m</td>
<td>16</td>
<td>80 MHz</td>
<td>65 mV pp</td>
<td>196 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>20 MHz</td>
<td>370 mV pp</td>
<td>428 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>40 MHz</td>
<td>240 mV pp</td>
<td>376 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>60 MHz</td>
<td>80 mV pp</td>
<td>225 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>80 MHz</td>
<td><strong>Fail</strong></td>
<td><strong>Fail</strong></td>
</tr>
</tbody>
</table>

Shows problem at 80 M transfers for first pulse detection.
Setup and Hold Time Margins with driver in different cable positions.

<table>
<thead>
<tr>
<th>Driver position</th>
<th>UDT Receiver position</th>
<th>Cable length</th>
<th>frequency</th>
<th>Max. duty cycle</th>
<th>Min. duty cycle</th>
<th>Setup/Hold</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>74%</td>
<td>24%</td>
<td>12.5</td>
</tr>
<tr>
<td>2</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>70%</td>
<td>39%</td>
<td>9.75</td>
</tr>
<tr>
<td>3</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>65%</td>
<td>42%</td>
<td>5.75</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>56%</td>
<td>41%</td>
<td>3.75</td>
</tr>
<tr>
<td>5</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>39%</td>
<td>36%</td>
<td>0.75</td>
</tr>
<tr>
<td>6</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>78%</td>
<td>63%</td>
<td>3.75</td>
</tr>
<tr>
<td>7</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>78%</td>
<td>58%</td>
<td>7.5</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>65%</td>
<td>57%</td>
<td>2.0</td>
</tr>
<tr>
<td>9</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>79%</td>
<td>49%</td>
<td>7.5</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>73%</td>
<td>60%</td>
<td>3.25</td>
</tr>
<tr>
<td>11</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>77%</td>
<td>64%</td>
<td>3.25</td>
</tr>
<tr>
<td>12</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>79%</td>
<td>64%</td>
<td>3.75</td>
</tr>
<tr>
<td>13</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>68%</td>
<td>57%</td>
<td>2.75</td>
</tr>
<tr>
<td>14</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>64%</td>
<td>36%</td>
<td>7.0</td>
</tr>
<tr>
<td>15</td>
<td>16</td>
<td>12m</td>
<td>40 MHz</td>
<td>77%</td>
<td>39%</td>
<td>9.5</td>
</tr>
</tbody>
</table>

Duty cycles not consistent.
**Setup and Hold Time Margins at Increased Speed**

<table>
<thead>
<tr>
<th>Cable Length</th>
<th># of Loads</th>
<th>Clock Frequency</th>
<th>Max. Duty Cycle</th>
<th>Min. Duty Cycle</th>
<th>Duty Cycle Range</th>
<th>Setup/Hold Margin</th>
<th>LVD signal-swing</th>
</tr>
</thead>
<tbody>
<tr>
<td>8m</td>
<td>16</td>
<td>40 MHz</td>
<td>74%</td>
<td>29%</td>
<td>45%</td>
<td>11.25 ns</td>
<td>456 mV pp</td>
</tr>
<tr>
<td>8m</td>
<td>16</td>
<td>60 MHz</td>
<td>see note 1</td>
<td>see note 1</td>
<td>see note 1</td>
<td>see note 1</td>
<td>240 mV pp</td>
</tr>
<tr>
<td>8m</td>
<td>16</td>
<td>80 MHz</td>
<td>failed</td>
<td>failed</td>
<td>failed</td>
<td>failed</td>
<td>208 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>40 MHz</td>
<td>74%</td>
<td>24%</td>
<td>50%</td>
<td>12.5 ns</td>
<td>456 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>60 MHz</td>
<td>58%</td>
<td>47%</td>
<td>11%</td>
<td>1.82 ns</td>
<td>252 mV pp</td>
</tr>
<tr>
<td>12m</td>
<td>16</td>
<td>80 MHz</td>
<td>49%</td>
<td>40%</td>
<td>9%</td>
<td>1.12 ns</td>
<td>200 mV pp</td>
</tr>
</tbody>
</table>

Table 1. Setup/Hold Time Data, fully-loaded configuration, asymmetrical outputs

**Note 1:** Data miscompare occurs at one point over the range of duty cycle adjustment.

- 38% to 45% : passed
- **46% to 53% : failed**
- 54% to 64% : passed
LVD Signals 40 MHZ, 8 Meter Cable, Asymmetrical Driver

LVD Signals 60 MHZ, 8 Meter Cable, Asymmetrical Driver

LVD Signals 80 MHZ, 8 Meter Cable, Asymmetrical Driver
Bias Terminator and Asymmetrical Drivers

- From testing it would appear asymmetric drivers may not be sufficient to compensate for bias in the terminator at higher speeds. This is caused by the cable and capacitance.

- An investigation into the effect bias has on the terminator shows this represents a noise source which causes distortion of the waveform, resulting in mis-clocking of the data (REQ/ACK).

- Different current sources required for asymmetrical drive result in large tolerances and bias in terminator also result in large tolerances. These errors will affect timing margin.
## Determination of Setup and Hold Time Margins.

**0.5 Meter cable in continuous run mode**

<table>
<thead>
<tr>
<th>Measurement Mode</th>
<th>80 MHz duty cycle</th>
<th>120 MHz duty cycle</th>
<th>160 MHz duty cycle</th>
<th>200 MHz duty cycle</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>no bias/ symmetrical</td>
<td>19 to 73%</td>
<td>26 to 63%</td>
<td>29 to 58%</td>
<td>35 to 47%</td>
<td>Proposed LVD Spec</td>
</tr>
<tr>
<td>no bias/ asymmetrical</td>
<td>19 to 73%</td>
<td>27 to 64%</td>
<td>29 to 59%</td>
<td>36 to 49%</td>
<td>0.1 V bias/ symmetrical</td>
</tr>
<tr>
<td>0.1 V bias/ asymmetrical</td>
<td>18 to 72%</td>
<td>24 to 60%</td>
<td>26 to 52%</td>
<td>30 to 40%</td>
<td>Current LVD Spec</td>
</tr>
</tbody>
</table>
Non-Biased Terminator and Symmetrical Drivers

- From testing, symmetric drivers with no bias can do as well at lower power. Could get more margin for same power.

- There is no tolerance problem with this setup since there is and no bias.

- Could more easily build a driver that provided an increased drive on the first transition to overcome any problems with sensing the first pulse after a delay.

- Symmetric drives with no bias is the way everyone else handles high speed line driving.

- Symmetric drivers will make future speed extensions easier.
Summary Of Predictions For Higher Speeds

Loss Of Signal Amplitude And Asymmetry As Shown In Test Data

Major Effects Contributing To Losses
- Capacitive loading of bus
- Conductor skin effect
- Lossy dielectric

Quantification Of Losses (40 to 80MT)
- 50% loss of asymmetry at receiver (short bus)
- Additional 50% loss; with a long bus - 25M (both symmetry and signal)
## Evaluation Of PH Layer Improvement Alternatives

<table>
<thead>
<tr>
<th>More Signal</th>
<th>Results</th>
<th>Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increase Drive Current 50%</td>
<td>More Power; Asymmetry % Same</td>
<td>Higher Power</td>
</tr>
<tr>
<td>Increase Load Spacing</td>
<td>2X Yields 140% Bandwidth</td>
<td>Legacy &amp; Backplanes</td>
</tr>
<tr>
<td>Lower CIN</td>
<td>Cin&lt; 10PF Yield 200% Bandwidth</td>
<td>Evolution of ASIC Design</td>
</tr>
</tbody>
</table>

### Less Noise

<table>
<thead>
<tr>
<th>Less Noise</th>
<th>Results</th>
<th>Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delete Asymmetry At Drivers</td>
<td>Greater Margin; Must Change Receivers &amp; Terminators</td>
<td>New Receiver Design</td>
</tr>
<tr>
<td>Improve Termination</td>
<td>Reduced Reflections; Must Change Spacing Rules And/Or Terminators</td>
<td>Legacy</td>
</tr>
</tbody>
</table>
# LVD Bus - Amplitude vs Frequency

## Graph Details

- **Log Amplitude (Millivolts)**: Ranges from 12% to 117% with peaks at 400 and 42 mV.
- **Log Frequency (Hz)**: Ranges from 20 to 640 Hz with peaks at 400 MHz.
- **4 ma @ 85 ohm**: Indicated at 4 mA.
- **1ST and 2ND Harmonics**: Marked at 10 PF loads.
- **10 PF 100 ohm**: Uses Ultra 3 pp.
- **10 PF 85 ohm**: Uses Ultra 3.
- **10 PF 20 PF loads**: Uses Ultra 2.

## Table: Impedance, Load, Uses

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Load</th>
<th>Uses</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 ohm</td>
<td>10 PF loads</td>
<td>Ultra 3 pp</td>
</tr>
<tr>
<td>85 ohm</td>
<td>10 PF loads</td>
<td>Ultra 3</td>
</tr>
<tr>
<td>85 ohm</td>
<td>20 PF loads</td>
<td>Ultra 2</td>
</tr>
</tbody>
</table>
Even Harmonics
(2) Change in 80 to 150 MHz
Differential 120 MHz
Waveforms
(1) Current Probe
Waveforms
(2) Asymmetrical
Noise

Amplitude vs Frequency
Amplitude vs Time
Fundamental @ 40 MHz
Bus Current Waveforms
Issue: Ultra 2 uses a bias voltage on terminator, which has been found to be detrimental to high operation.

But: Bias is required to assure the receivers will be in a non asserted state if bus is not driven.

And: We need to keep backwards compatibility between Ultra 2 and Ultra 3.
Ultra 3 Strawman Definition

- 80 M transfers per Second
- 12 Meter max length
- 16 Loads
- 25 Meter max length point to point
- Load Capacitance 10/10/5
- Terminator unbiased
- Drivers are symmetrical
Ultra 3 Proposed Receiver

To use no bias at high speed must assure undriven is detected as non-asserted.

Receiver with offset was proposed for Ultra 2 but deemed no better than biased terminator.

In this case offset receiver was only for protocol not data transfer. Therefore, have non-asserted state for arbitration and best possible situation for data transfer.
Dual Receiver Design Considerations

Primary Data Receiver, High Speed, Low Offset

Secondary Protocol Phase Receiver
- ~130mV +/- 20% built-in offset
- Low speed, ~50ns delay time will be fine
- A very low power design still has good speed with a multiple stage design
- Small area, Vt offset design can be ~3200 square micron in 0.6µ process. This is ~1-3% of pad area.
- Low input capacitance. Small input transistors can be used, they would add ~0.05pf to the pin capacitance
Design Examples
Compatibility Goal

Want to have compatibility between Ultra 2 and Ultra 3. Compatibility is defined as being able to have Ultra 2 device work on Ultra 3 and vice versa.
Compatibility Goal

Backward Compatibility - 2 Cases

Ultra 2 Configuration - Biased Bus

Init 40

Ultra 3 Configuration - non-Biased Bus

Init 80

T10/97-146r0
Compatibility Goal

Three Approaches:

A
• Keep Ultra 2 as is.
• Have Ultra 3 require a Ultra 2 mode.
• Use a Ultra 2 to Ultra 3 adapter.

B
• Define an Ultra 2A receiver design.
• Build Ultra 3 and Ultra 2A with support for a non-biased bus.

C
• Change Ultra 2 to an non-biased bus.
**Approach A**

**Ultra 3/2 Receiver Design**

In Ultra 3 mode the switch is open.

In Ultra 2 mode the switch is closed and use is made of the biased bus.

This receiver will work on current Ultra 2 (biased bus) system as well as Ultra 3 system.

Current Ultra 2 defined receivers would need an adapter on a non-biased bus.
Approach A

Backward Compatibility - 2 Cases

Ultra 2 Configuration - Biased Bus

Init 40

40 40 40 80

Ultra 3 Configuration - non-Biased Bus

Init 80

80 80 80 Adapter

Ultra 3/2 RCV

Va ≠ Vb

Va = Va

T10/97-146r0
Approach B

Ultra 2A Receiver Design

To make Ultra 2 device work on a non-Biased bus, the Ultra 2 receiver to be as follows.

In this configuration operating on Ultra 2 bus (with bias) switch is closed and terminator bias is used.

When operated on Ultra 3 bus with the switch is open, the offset assures the receiver sees a non-asserted state when the bus is not driven. Note the receiver at a maximum of 40 M transfers.
Approach B

Backward Compatibility - 2 Cases

Ultra 2 Configuration - Biased Bus

Init 40

40 40 40 80

Ultra 3 Configuration - non-Biased Bus

Init 80

80 80 80 40

Ultra 3/2 RCV

Ultra 2A RCV
Approach C

Change Ultra 2 to an non-biased bus. The new receiver both becomes as shown for Ultra 3 receiver.
**Approach C**

**Backward Compatibility - 2 Cases**

**Ultra 2 Configuration - Biased Bus**
- **Init 40**
  - 40
  - 40
  - 40
  - 80

**Ultra 3 Configuration - non-Biased Bus**
- **Init 80**
  - 80
  - 80
  - 80
  - 40

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Adaptec
Summary

Changing LVDS to a non-biased bus provides additional margin for extending the bus more easily to higher speed operation.

Backward compatibility can be achieved using one of several different ideas presented.