X3T10/96-278

SYMBIOS LOGIC

Date: November 26, 1996

To: Dr. Bill Ham, Digital Equipment
Richard Moore, Adaptec
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cc: Kevin Bruno, Symbios Logic
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From: Frank Gasparik

Subject: SPI-2 Rev. 11
Timing Specifications

Here is my response to your recent Email from Richard More regarding the SPI-2 timing specification. First let me clarify where the 60mV comes from.

1. Input offset voltage

Please refer to Figure 20A below. This is a modified Figure 20 from the SPI-2 document. If the receiver is implemented with either N or P-channel differential pair, there is an inherent input offset voltage, V_{io}. This input offset voltage is caused by a number of physical factors such as threshold mismatch and thermal gradient between the MN_1 and MN_2 devices, layout symmetry, masking photo-lithographic process variations, load mismatch, etc. Under ideal layout conditions, the input offset voltage has the Gaussian distribution, i.e. it has both +/- polarities. Depending upon the process control the three sigma V_{io} can be of the order of a few 10's of mV.

The receiver's minimum differential input signal has to overcome this input offset voltage and also to provide some overdrive, depending upon the gain of the receiver. As a reference point let's use for the V_{io} effect +/- 20mV. The overdrive depends upon the design implementation and the desired speed of the receiver. We can use any number from say 10 to 20mV. This will give us a minimum differential input signal of approximately 40mV.

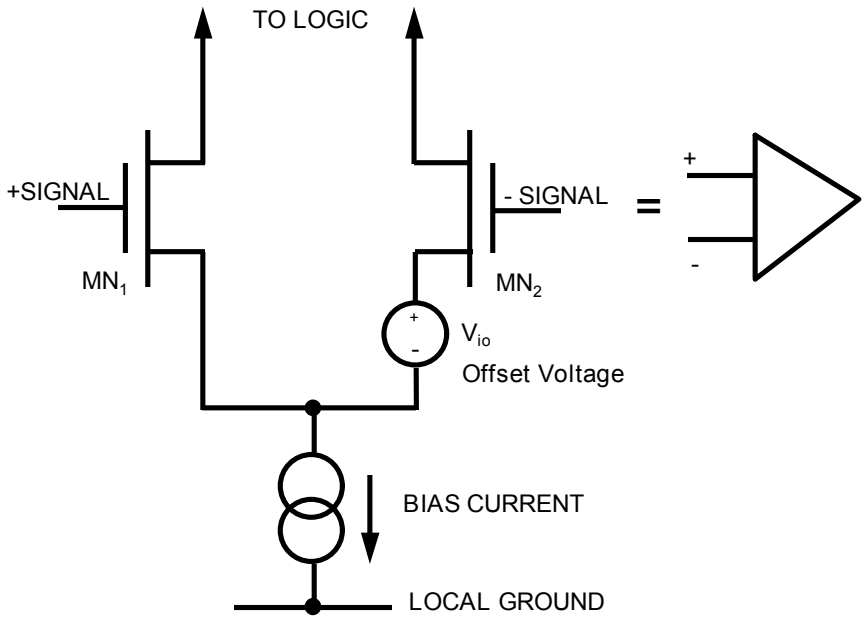


Figure 20A - LVD Receiver Example

2. Attenuation of the SCSI cable

I will use the SCSI cable listed in Fast-20 document. The 28 AWG cable has the characteristic impedance Z_o=110Ω and an attenuation of 0.28dB/m. For 25m cable it's 25 * (-0.28) = -7dB. That's an attenuation factor of 0.447.

From Table 15 the $|V_A| = |V_N|$ = 115mV. Even without the effect of maximum 16 loads, the signal at the end of the cable will be 115mV * 0.447 = 51mV. So the 60mV differential input signal for the receiver is in the ball park.

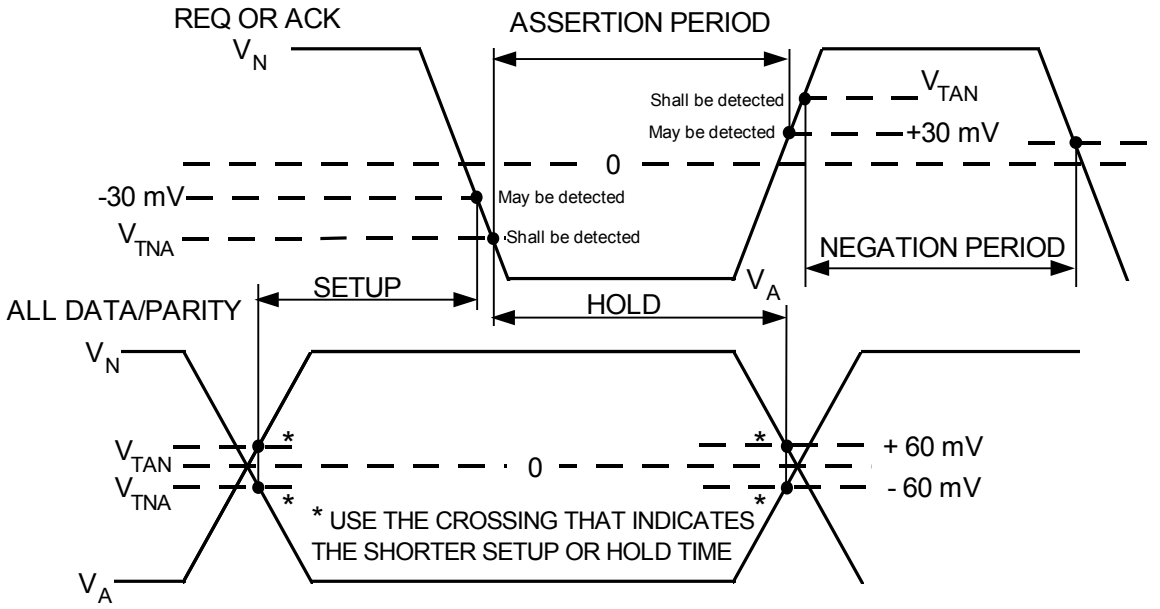
The maximum attenuation listed in Table 15 is 15% (measured from the driver to the farthest receiver.) This is in conflict with the specification for the cable even for a maximum 12 meter long cable.

3. Timing Specification

Figure 24 need slight modification as indicated below. Then it will agree with the definitions of the Fast-20 document Figure 1B which is also included below.

Table I - System level Requirements

Parameter	min	max	notes	reference
V_A (mV)	- 115		1	this table
V_N (mV)		115	1	this table
receiver input (mV) differential	- V_N * 0.25	- V_A * 0.25		
attenuation (%)		15	2	this table
loaded media impedance (ohms)	85	135	3	this table
unloaded media impedance (ohms)	110	135		section
terminator bias (mV)	100	125		section
terminator impedance (ohms)	100	110		section
device leakage (μA)	-20	20		section
number of devices	2	16	4	
ground offset level (mV)	-355	355	5	this table



V_{TNA} = - max [60 mV, 0.25 * V_N]

V_{TAN} = max [60 mV, - 0.25 * V_A]

1.0 V ≥ V_N ≥ 60 mV

- 1.0 V ≤ V_A ≤ - 60 mV

DIFFERENTIAL VOLTAGE SIGNALS IN ALL CASES

Figure 24 - Definition of timing measurement points

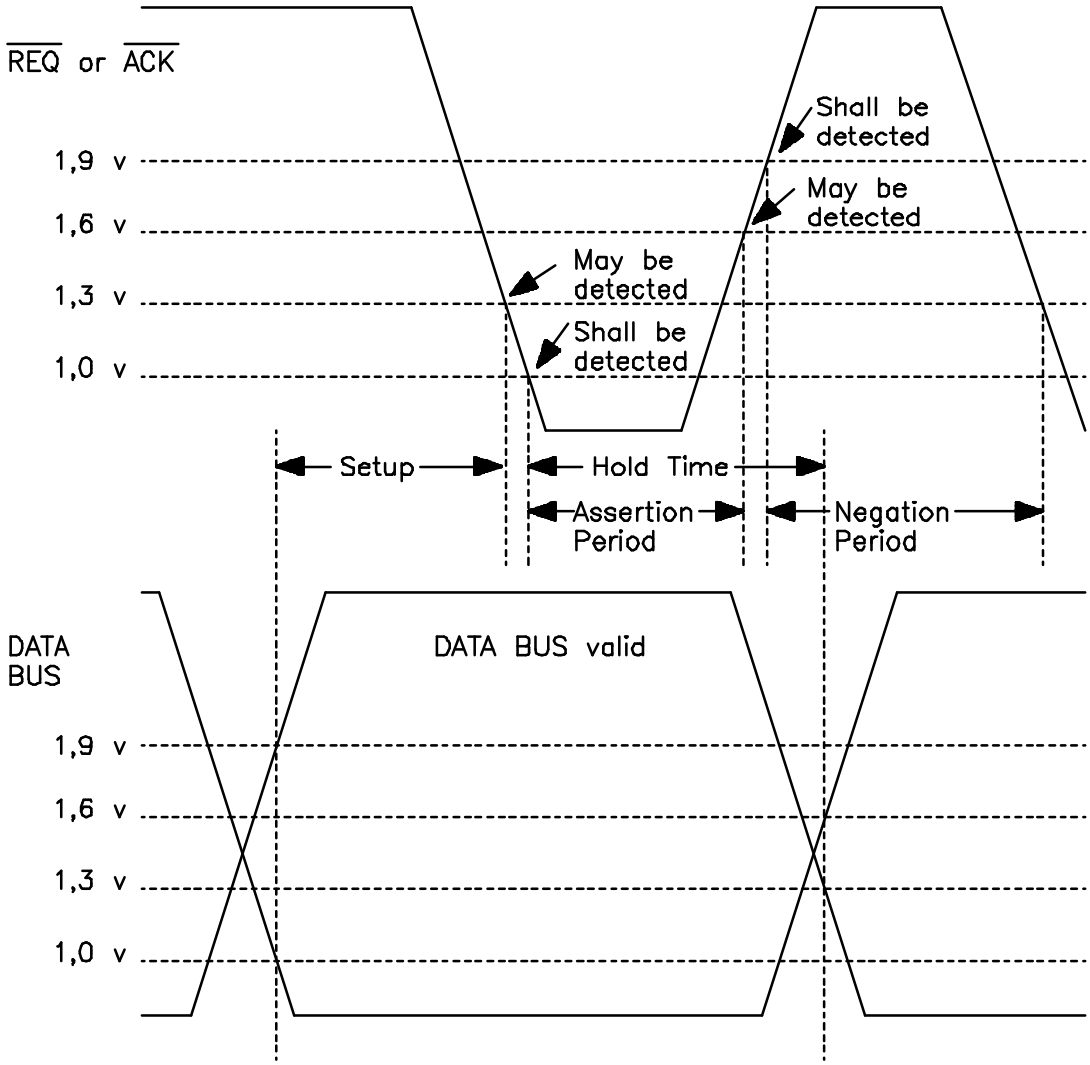


Figure 1.B - Definition of timing measurement points