Date: Jan. 3, 1997 X3T10/96-195R1
To: X3T10 Committee
From: Gerry Houlder, Seagate Technology
Sub: Add Mode Page for fibre channel features

With Fibre Channel - Arbitrated Loop (FC-AL) interface, there are characteristics implementors desire to customize. This proposal includes control bits for interface characteristics of Fibre Channel Private Loop that implementors desire to control.

These controls are for characteristics that must be known when the device is powered on. They cannot be set during login or a later command. This behavior can be met by use of a Mode page with saved values. In fact the parameters will have to be saved in flash memory, so there is no wait for device spinup before the parameters are available.

As of Jan. 3 there are still several places in FC-PH that require loop initialization. This requirement conflicts with many of the functions defined here, so this proposal can not be accepted for inclusion in SCSI-3 until the X3T11 committee resolves the wording in FC-PH to allow these functions. I expect X3T11 will allow these functions with in the next few months, however, so it is time for us to review this proposal.

The characteristics below will be proposed for inclusion in the Disconnect-reconnect mode page (page 2). The proposed text will need to be added to SPC-2 (since this is where mode page 2 is described) and FCP-2 (since this must describe how these bit settings control the behavior of the Fibre Channel interface). Changes to the table are in byte 13, the text is additional explanation that is needed.

Table 100 - Disconnect-reconnect

Bit Byte	7	6	5	4	3	2	1	0
0	PS	Reserved	PAGE CODE (02h)					
1	PAGE LENGTH (0Eh)							
2	BUFFER FULL RATIO							
3	BUFFER EMPTY RATIO							
4	(MSB)	BUS INACTIVITY LIMIT						
5								(LSB)
6	(MSB)	DISCONNECT TIME LIMIT						
7								(LSB)
8	(MSB)	CONNECT TIME LIMIT						
9								(LSB)
10	(MSB)	MAXIMUM BURST SIZE						
11								(LSB)
12	EMPD	FARD	FAWRT	FASAT	DIMM	DTDC		
13	RESERVED	RESERVED	DDIS	DDLM	DSA	ALWLI	DTIPE	DTOLI
14	(MSB)	FIRST BURST SIZE						
15								(LSB)

When Disable Target Originated Loop Initialization (DTOLI) bit is one, the target does not generate the Initializing LIP following insertion into the loop. The target will respond to an Initializing LIP when it is received. The target shall generate the Loop Failure LIP if it detects loop failure at its input and the Initializing LIP when the loop failure is corrected. When DTOLI bit is zero, the Target generates the Initializing LIP after it enables a port into a loop.

When Disable Target Initiated Port Enable (DTIPE) bit is one, the target waits for an Initiator to send the Loop Port Enable primitive before inserting itself into the loop. The target uses the hard address available in the SCA connector (or device address jumpers) to determine if primitives are addressed to it. When DTIPE bit is zero, the target enables its port into the loop without waiting for a Loop Port Enable primitive.

When Allow Login Without Loop Initialization (ALWLI) bit is one, the target shall use the hard address available in the SCA connector (or device address jumpers) and accept logins without verifying the address with loop initialization. When ALWLI bit is zero, the target is required to verify its address through the Loop Initialization process before a login is accepted.
When Disable Soft Address (DSA) bit is one, the target does not select a soft address if there is a conflict for the hard address selection during Loop Initialization. In this case the target enters the non-participating state. If the Target detects loop initialization while in the non-participating state, the target will again attempt to get its hard address. When DSA bit is zero, the Target attempts to obtain a soft address during the Loop Initialization process.

When Disable Loop Master (DLM) bit is one, the target does not become loop master. The target only repeats LISM frames it receives. This allows the initiator to be loop master during loop initialization. When DLM bit is zero, the Target may become loop master during in the Loop Initialization process.
When Disable Discovery (DDIS) bit is one, the target does not require receipt of Address or Port Discovery following loop initialization. The target resumes processing of tasks on completion of loop initialization. When DDIS bit is zero, the target must wait to receive an Address or Port Discovery before it resumes processing tasks for that initiator.