LVD SCSI Driver Proposal

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Adaptec

Existing Boundaries

- Test circuit (SPI-2 10.1.1):

  9.7 mA < Ia < 15.0 mA

  4.9 mA < In < 15.8 mA

  -0.9 mA < Ia - In < 7.5 mA

  This describes a diagonal band across a rectangular region.

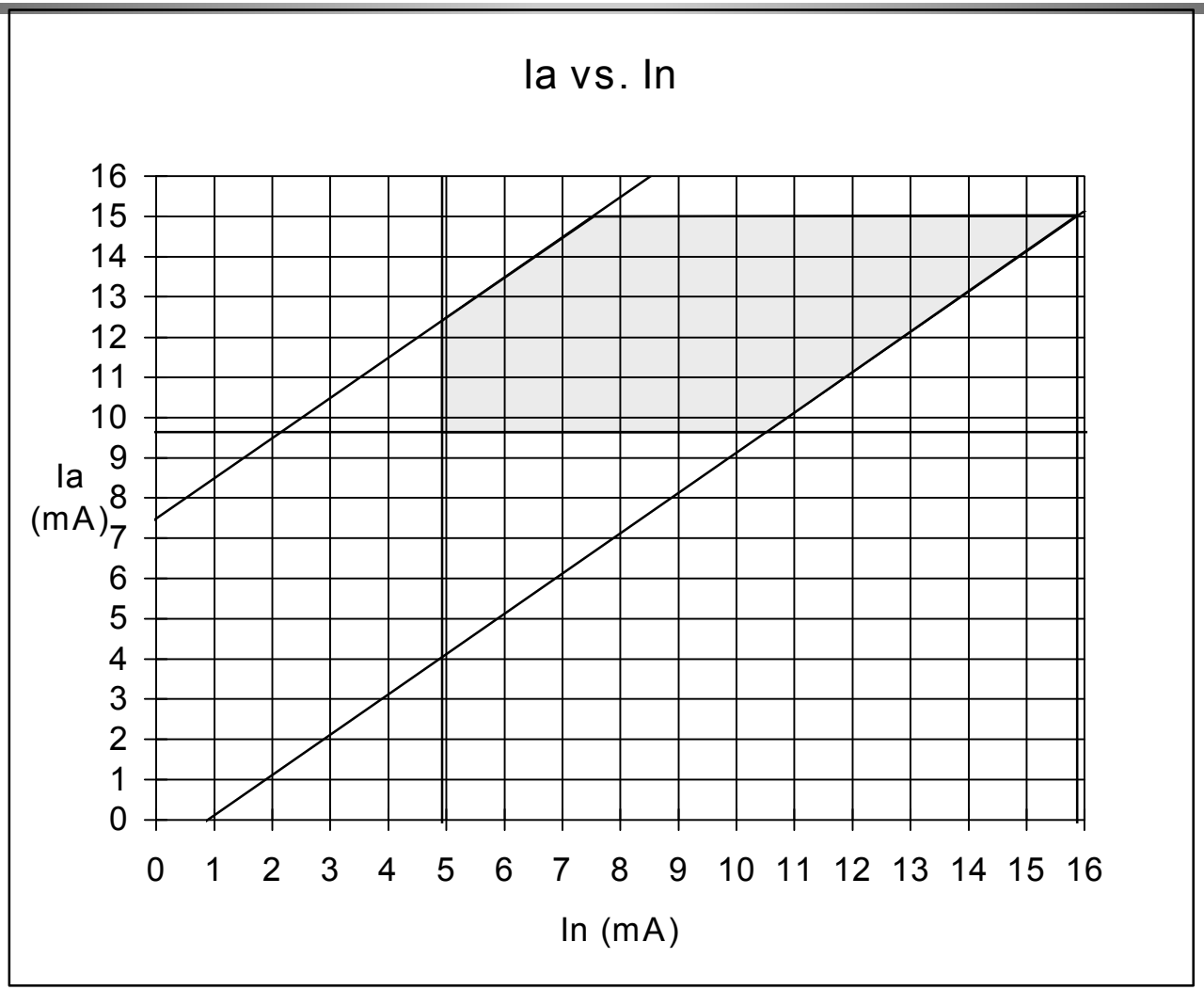
- Algebraically derived minimum requirements:

  Ia >= 7.02 mA + .353 * In

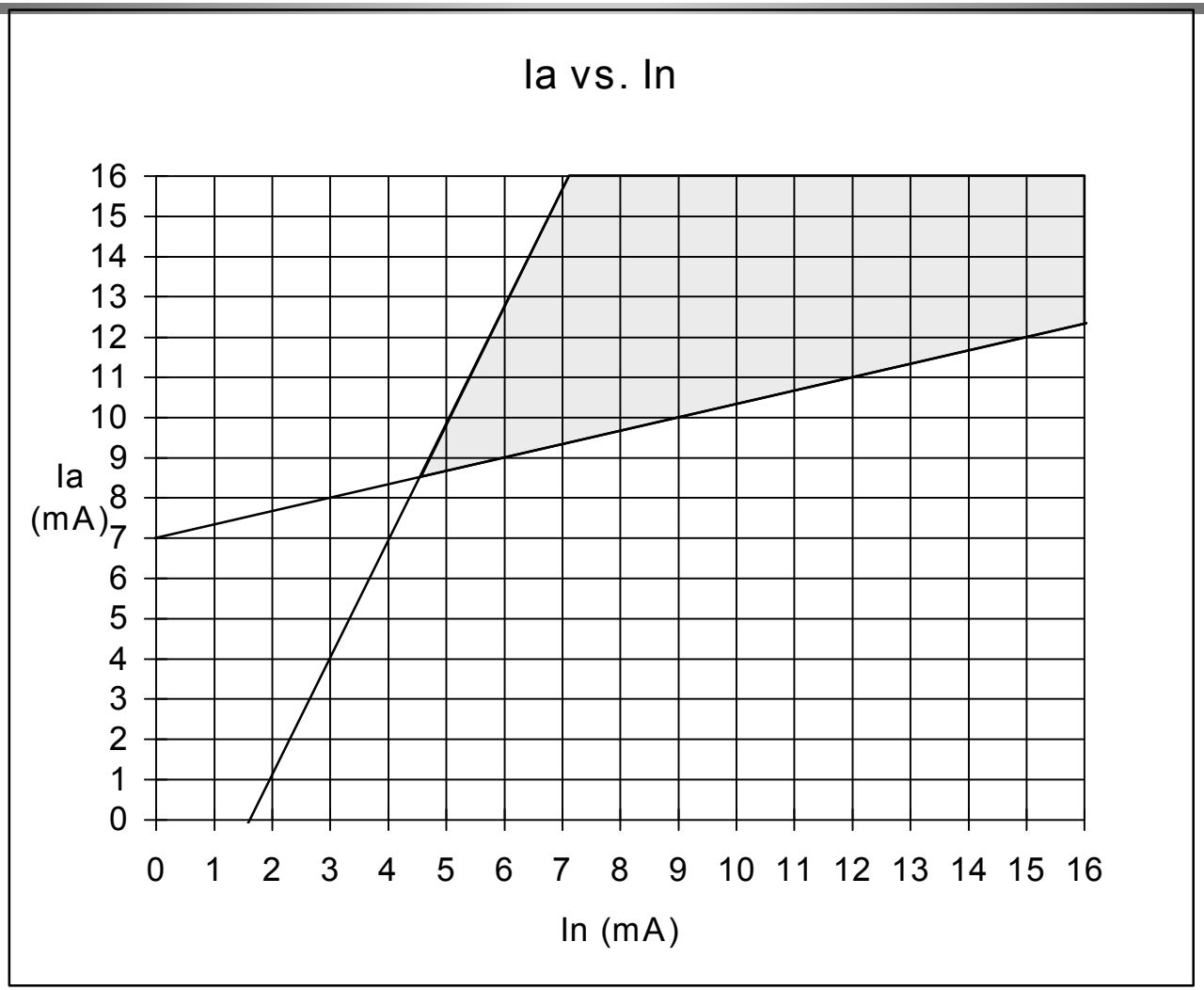
  In >= 1.61 mA + .353 * Ia

  This describes a wedge-shaped region.

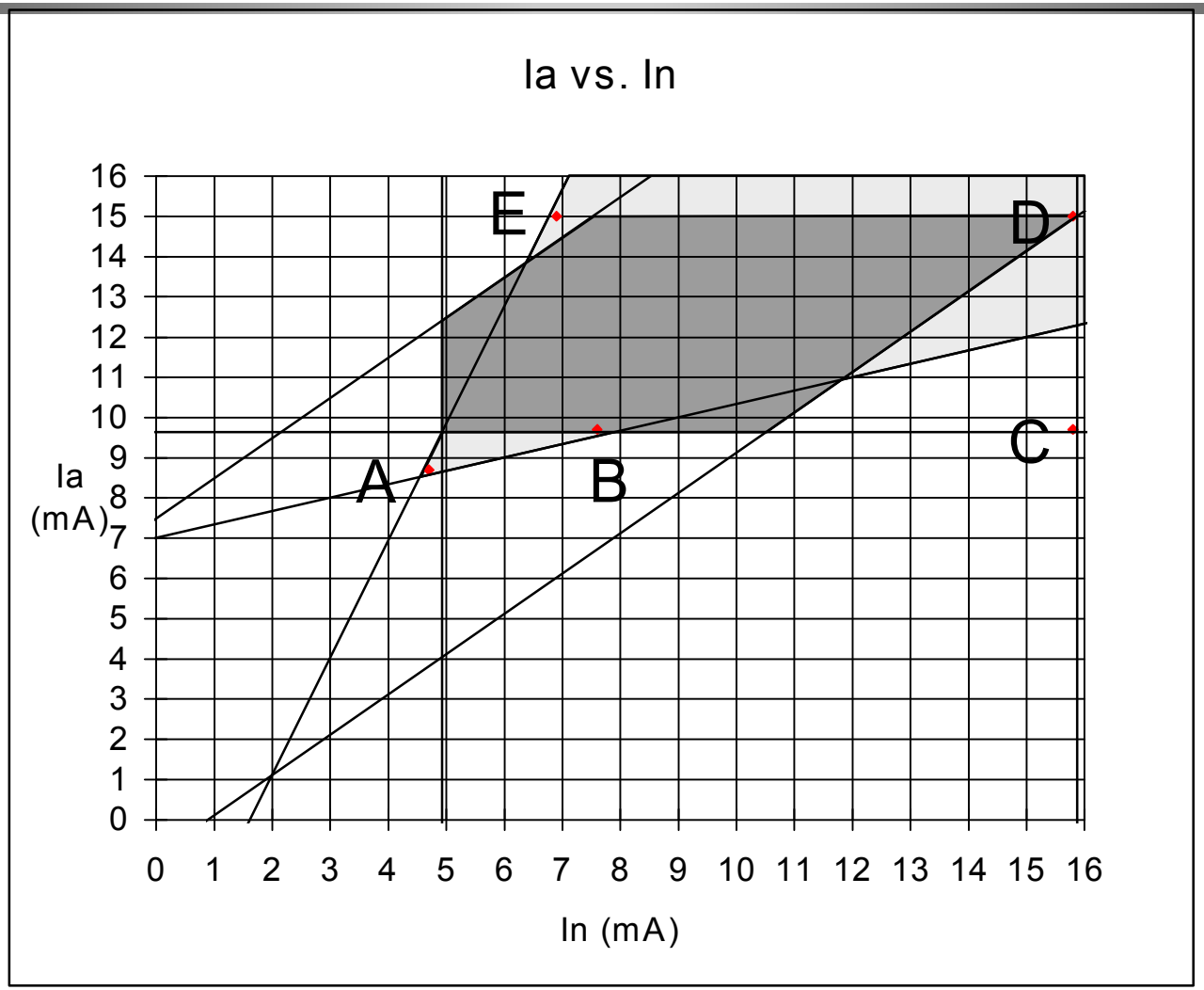
SPI-2 Test Circuit (10.1.1)



Algebraic Solution



Overlay of Both Regions



Points of Interest

Label	In (mA)	Ia (mA)	Significance
A	4.7	8.7	Tip of wedge
B	7.6	9.7	Intersection of wedge and bottom edge of rectangle
C	15.8	9.7	Lower right-hand corner of rectangle
D	15.8	15.0	Upper right-hand corner of rectangle
E	6.9	15.0	Intersection of wedge and top edge of rectangle

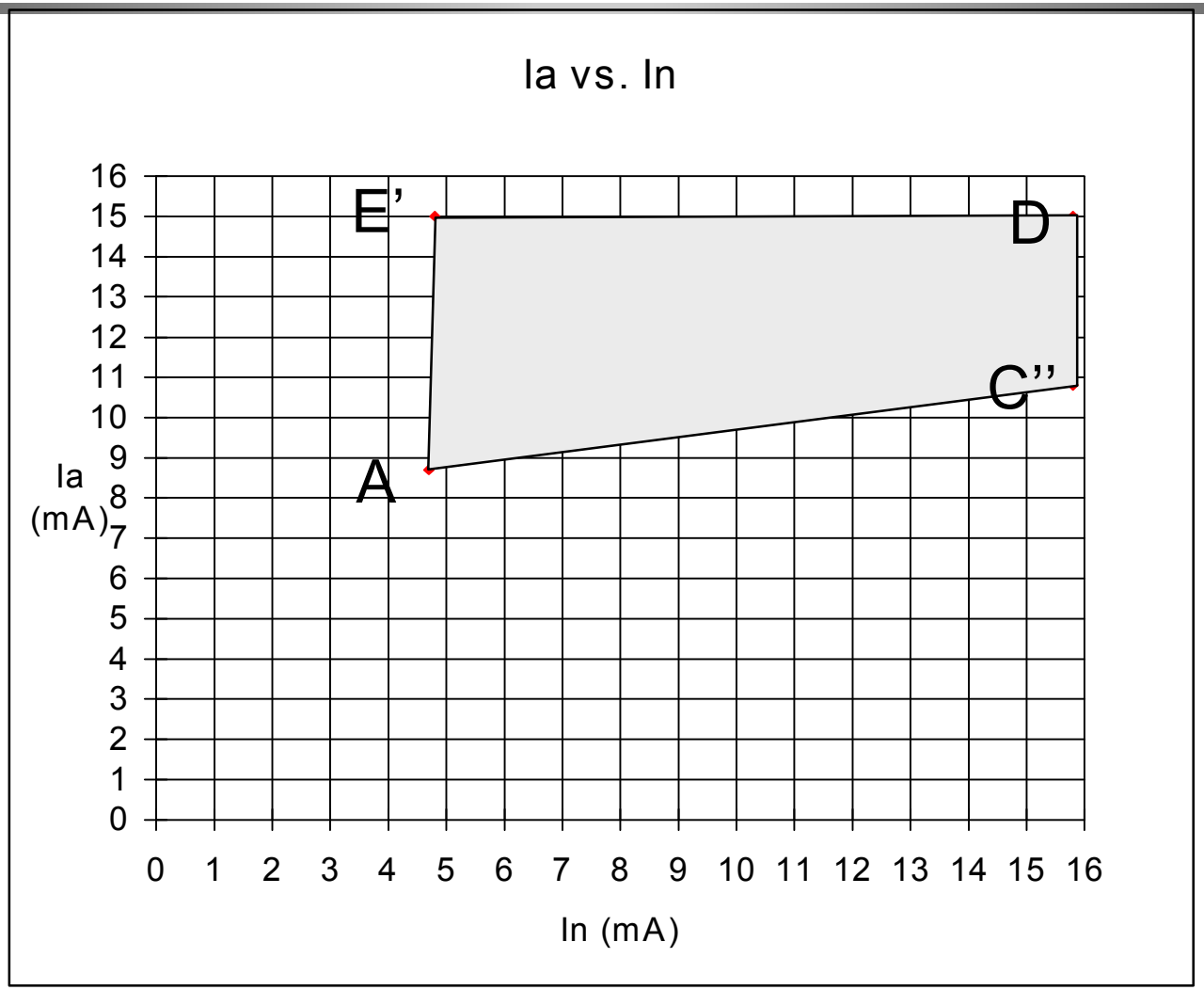
- Consider region ABCDE.
- Point C fails in Kevin Gingerich's spreadsheet model. Either move up or move left.
- Points B and E are unnecessarily strict. Eliminate B and move E to the left.

Points of Interest

Label	In (mA)	Ia (mA)	Significance
A	4.7	8.7	Tip of wedge
C'	10.1	9.7	Rightmost working point on bottom edge of rectangle
C''	15.8	10.8	Lowest working point on right-hand edge of rectangle
D	15.8	15.0	Upper right-hand corner of rectangle
E'	4.8	15.0	Leftmost working point on top edge of rectangle

- Consider AC'DE'. Boundary includes 3 diagonals and one horizontal segment.
- AC''DE' requires one less diagonal segment and is therefore easier to specify.
- The spreadsheet model shows that all four corners of AC'DE' or AC''DE' give sufficient assertion-to-negation and negation-to-assertion transitions under worst case conditions.

Modified Region of Operation



Objection: 4:1 Voltage Ratio

- Need to meet receiver input balance requirements.
- Derive an additional boundary condition:

  $|V_N| <= 4*|V_+|$

  $-V_N <= 4*(V_N + (I_A + I_N)*Z_L/2)$

  $5* V_N + 2*(I_A + I_N)*Z_L >= 0$

  $5*(I_N*R_T/2 + V_B) <= 2*(I_A + I_N)*Z_L$

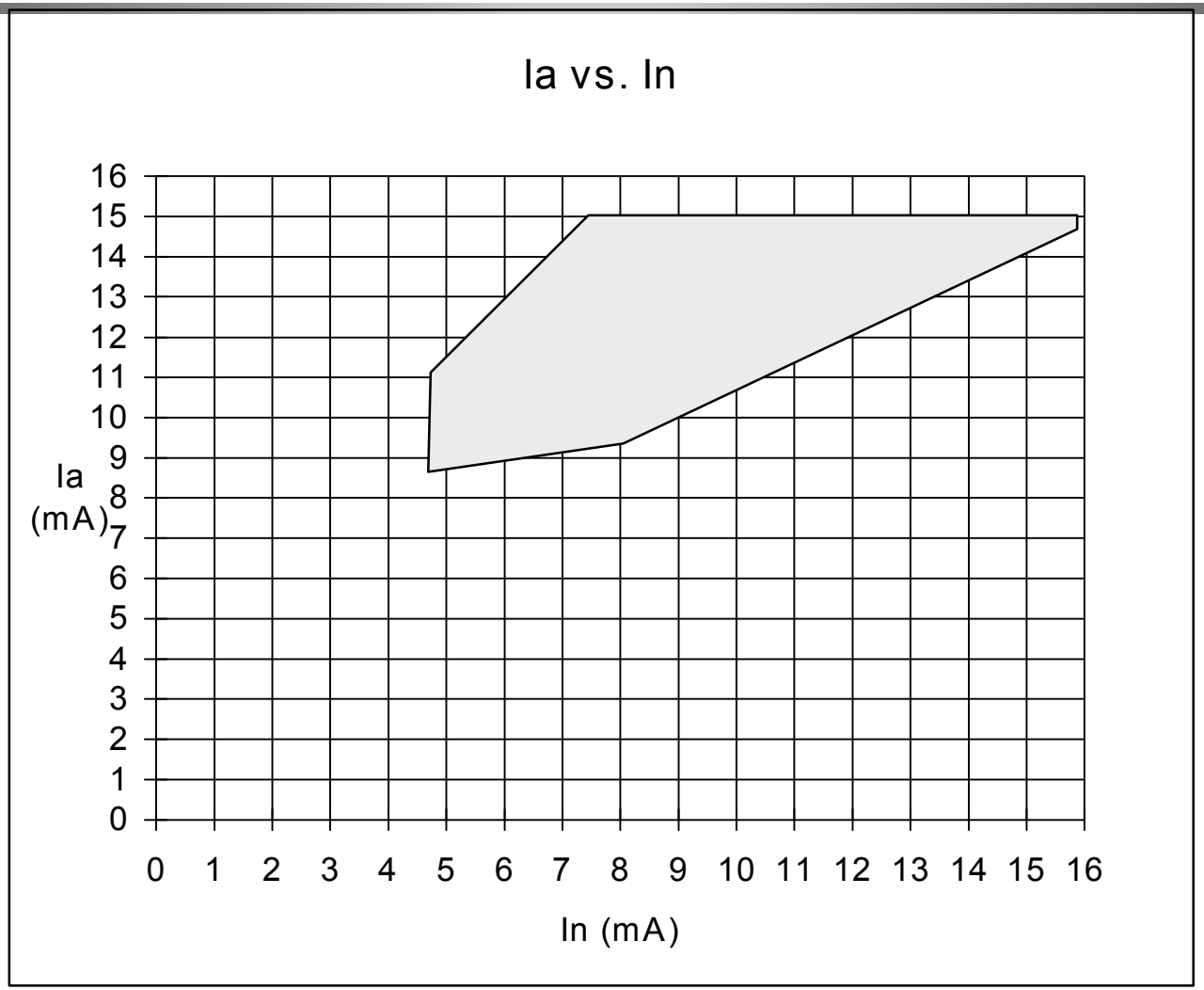
  $I_A >= 3.8\ mA + .69*I_N$
- Similar derivation to ensure $|V_A| <= 4*|V_-|$ gives:

  $I_N >= -2.9\ mA + .69*I_A$

  or,

  $I_A <= 4.2\ mA + 1.45*I_N$

Revised Region of Operation



New Boundaries

$I_A >= 7.8\ mA + 0.19 * I_N$	(AC'')
$I_N <= 15.8\ mA$	(C''D)
$I_A <= 15.0\ mA$	(DE')
$I_N >= 4.5\ mA + 0.02 * I_A$	(E'A)
$I_A >= 3.8\ mA + 0.69 * I_N$	(receiver
$I_N >= -2.9\ mA + 0.69 * I_A$	balance)

Proposed Test Conditions

- Replace:

  416 mV <= V_A <= 706 mV

  with:

  309 mV + 0.19 * |V_N| <= V_A <= 706 mV
- Replace:

  381 mV <= |V_N| <= 977 mV

  with:

  361 mV + 0.02 * V_A <= |V_N| <= 977 mV
- Replace:

  -277 mV < |V_A| - |V_N| < 181 mV

  with:

  91 mV + 0.69 * |V_N| <= V_A <= 113 mV + 1.45 * |V_N|

Further Improvements?

- Lowering the maximum termination resistance or the maximum bias voltage reduces the drive current requirement by about 0.5 to 1.0 mA. Minimum values for these parameters should not be changed.
- How much tightening of these parameters (if any) can be tolerated by terminator designers?