LVD SCSI Release Glitches

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Overview

◆ Release glitches can occur when a signal transitions from actively negated to released state

◆ Glitches can be suppressed via prevention and/or masking

- Restrictions at transmitting device to prevent release glitches from occurring

- Mask out signals at receiving device to ignore potential release glitches

◆ Propose to use combination of prevention and masking for least overall complexity at transmitter and receiver

Proposed LVD SCSI Rules

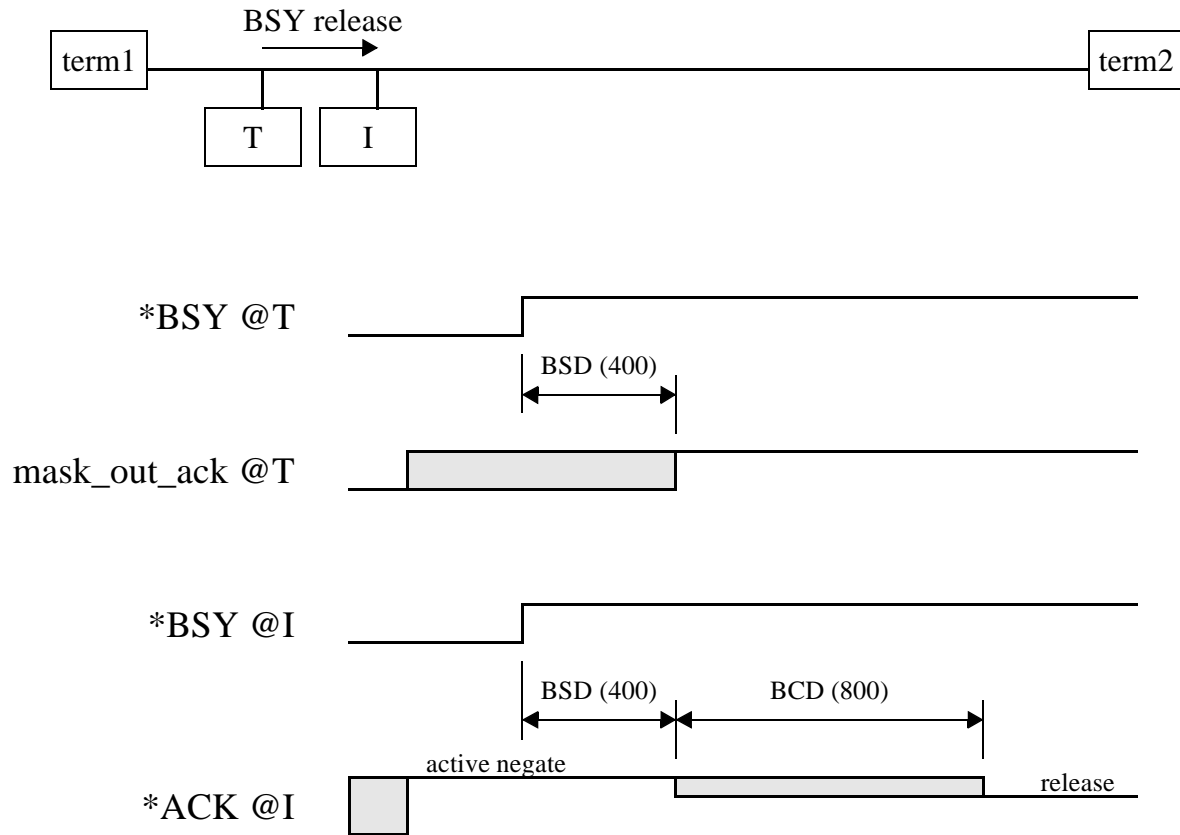| Signals	Source	Active Neg	Transmitting Device Requirements	Receiving Device Requirements
BSY, SEL, RST	I,T	P	--	--
ACK, ATN	I	R	Initiator shall wait for Bus Free phase before releasing ACK & ATN from actively negated state	Target shall mask out ACK & ATN after negation of last ACK and within BSD of releasing BSY
REQ	T	R	Target shall wait 2.5*BSD after releasing BSY before releasing REQ from actively negated state	Initiator shall mask out REQ within 1.5*BSD detecting BSY release
C/D, I/O, MSG	T	A/R/P?	--	--
Data & Parity	I,T	R	--	--

I -- initiator; T -- target
P -- prohibited; R -- required; A -- Allowed

BSD = Bus Settle Delay (400ns)
Bus Free Phase starts Bus Settle Delay after BSY & SEL are both negated
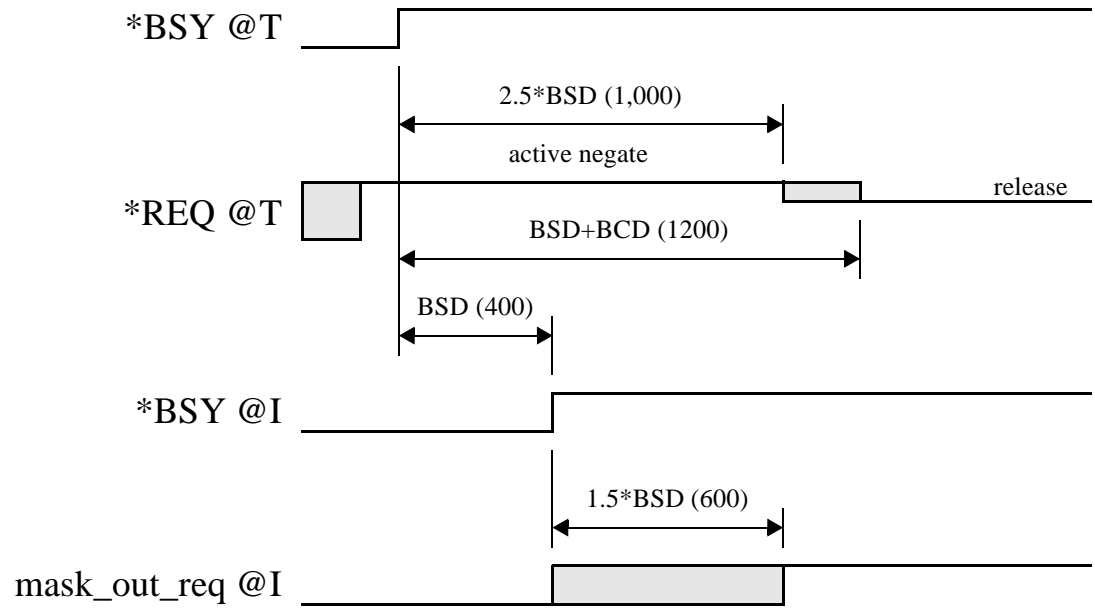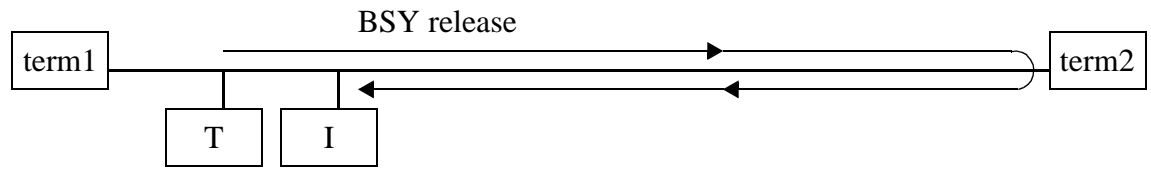
Release Glitch Suppression on ACK

Worst case scenario: Initiator immediately detects BSY release (incident wave, adjacent I & T)

BSD = Bus Settle Delay
BCD = Bus Clear Delay

Release Glitch Suppression on REQ

Worst case scenario: Initiator detects BSY release after round trip delay (reflected wave)

BSD = Bus Settle Delay
BCD = Bus Clear Delay

BSY, SEL & RST

- Active negation prohibited due to wire-or

- Protocol delays allow for reflected wave detection

ATN

- Active negation required since ATN to ACK setup time (2 Deskew delays, 90ns) requires incident wave detection on ATN.

- Use same rules as ACK

Phase Signals (C/D, I/O & MSG)

- Active negation NOT needed since protocol delays allow for reflected wave detection of phase signals and will mask out release glitches

- Decision to require, allow or prohibit active negation on phase signals is beyond the scope of this proposal

Data & Parity

- Release glitches on data & parity are inherently masked by protocol (strobed by REQ/ACK during information transfer, protocol delays during arbitration/(re)selection)

- Exception: selection time-out (see Symbios proposal)